User's Guide

LMQ66430-Q1 Buck Controller Evaluation Module User's Guide

ABSTRACT

The Texas Instruments LMQ66430-2EVM evaluation module (EVM) helps designers evaluate the operation and performance of the LMQ66430-Q1 wide-input voltage buck converter. The LMQ66430-Q1 is an easy-to-use synchronous step-down voltage converter capable of driving up to 3 A of load current from an input voltage of up to 36 V. The LMQ66430-2EVM features an output voltage of 3.3 V and a switching frequency of 2.2 MHz. By default this EVM is populated with the LMQ66430MC3RXBRQ1. This EVM is capable of supporting the entire LMQ664x0-Q1 family of devices by exchanging the default IC with other variants in the family including the non-automotive grade devices. See the data sheet for additional features, detailed descriptions, and available options.

Table 1-1. Device and Package Configurations

EVM	U1	FREQUENCY	SPREAD SPECTRUM	CURRENT	PIN 13 TRIM
LMQ66430-2EVM	LMQ66430MC3RXBRQ1	2200 kHz	Enabled	3 A	MODE/SYNC

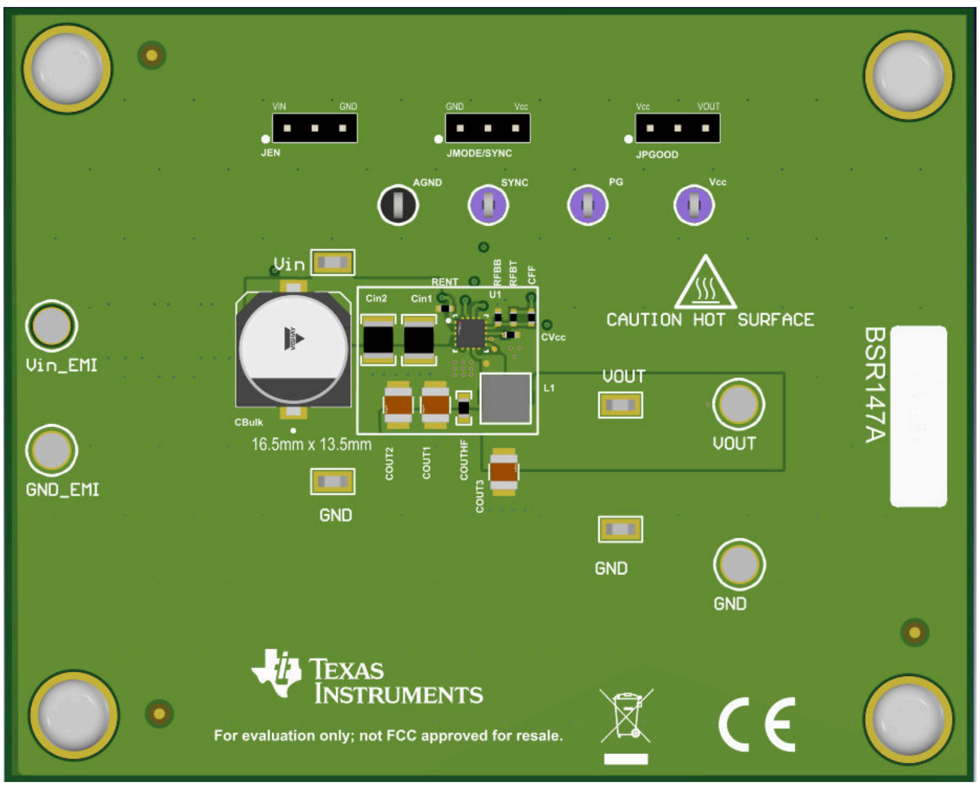

Figure 1-1. LMQ66430-2EVM Board

CAUTION

Caution Hot surface.
Contact may cause burns.
Do not touch.

Table of Contents

Trademarks

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1 Setup

This section describes the test points and connectors on the EVM and how to properly connect, set up, and use the LMQ66430-Q1 EVM.

1.1 Test Points

The test points on the board can be used to connect to the input of a power supply and output load for the EVM. See Figure 1-1 for typical test setup. The functions of the test point connections are:

- **Vin_EMI —** Input supply to EVM including an EMI filter. Connect to a suitable input supply. Connect at this point for EMI tests.
- **GND_EMI —** Ground connection for the input supply
- **Vin —** Input supply to the IC. Can be connected to a digital multimeter to measure the input voltage after EMI filter.
- **VOUT —** Output voltage test point of EVM. Can be connected to a desired load.
- **GND —** Ground test points
- **PG —** This test point is connected to the PGOOD pin from the IC. Can be tied to an external supply through a pullup resistor or left open.
- **SYNC —** In a **MODE/SYNC** trim part, this test point is connected to the SYNC pin of the IC. This test point can also be connected to an external clock to synchronize the IC. Make sure the RT resistor is not installed when applying a synchronous clock input. If RMOD is installed, JMODE/SYNC jumper must not short pin 2 to either adjacent pins while applying a synchronous clock input. For evaluating **RT** trim parts, see the JMODE/SYNC jumper description in Section 1.2.
- **Vcc —** This test point is connected to the Vcc pin of the IC.
- **AGND—** This test point represents the analog ground test point and is connected to the ground plane.

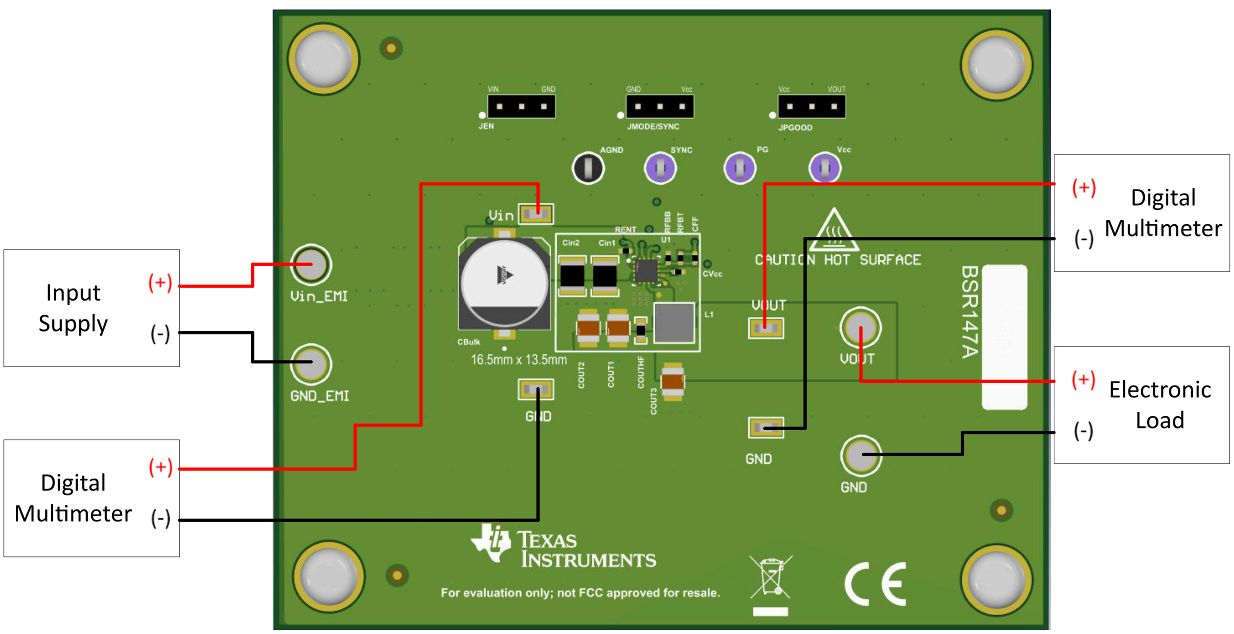

Figure 1-1. EVM Board Connections

1.2 Jumpers

See Figure 1-2 for jumper locations.

- **JMODE/SYNC —** Use this jumper to select the mode of operation in a **MODE/SYNC** trim part. Connecting a jumper between pin 1 and 2 sets the IC operation to PFM (pulse frequency modulation) mode for a higher efficiency at light load. A jumper between pin 2 and pin 3 causes the IC to operate in FPWM (forced pulse width modulation) mode. By default, the jumper is connected between pin 1 and 2. Pin 1 is indicated by the dot on the PCB. When evaluating **RT** trim parts this jumper can be used to set the switching frequency as long as RMOD is populated and RT is not populated. With RMOD populated, connecting a jumper between pin 1 and 2 sets the switching frequency to 2.2 MHz while connecting the jumper between pin 2 and 3 sets the switching frequency to 1 MHz. If the RT resistor is used to set the switching frequency then RMOD should be depopulated, effectively removing the JMODE/SYNC jumper.
- **JEN —** This jumper allows the ENABLE input to be connected to VIN or GND. Connecting a jumper between pin 1 and 2 shorts the ENABLE input to VIN, enabling the part. Connecting a jumper between pin 2 and 3 shorts the ENABLE input to GND, disabling the part. By default, this jumper is left open because there is a pullup resistor RENT to VIN to enable the IC.
- **JPGOOD —** Use this jumper to select how the PGOOD pin is connected. A jumper between pin 1 and 2 uses Vcc as the pullup voltage for PGOOD. In this configuration, the PGOOD pin is pulled up to Vcc through RPG when the output voltage is within regulation. Connecting a jumper between pin 2 and 3 uses VOUT as the pullup voltage for PGOOD. By default, this jumper is not populated.

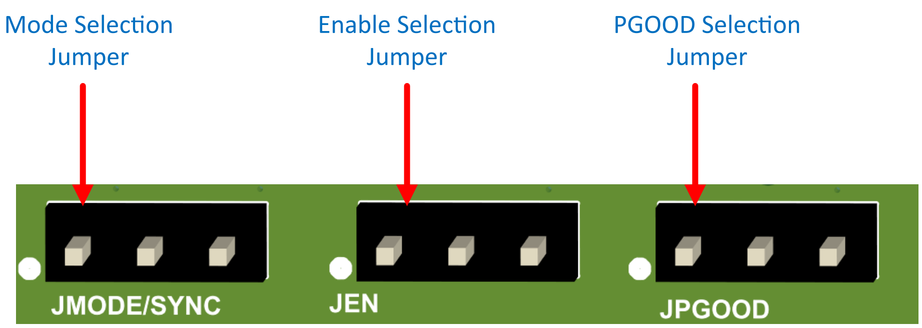

Figure 1-2. Jumper Locations

2 Operation

2.1 Quick Start

1. Connect the voltage supply between the Vin_EMI and GND_EMI supply connections.
2. Connect the load between the VOUT and GND test points.
3. Set the supply voltage at an appropriate level between 3.5 V to 36 V. Set the current limit of the supply to an appropriate level.
4. Turn on the power supply. With the default configuration, the EVM powers up and provides V_{OUT} = 3.3 V.
5. Monitor the output voltage. The maximum load current is rated at 3 A with the LMQ66430-Q1 device.

3 Schematic

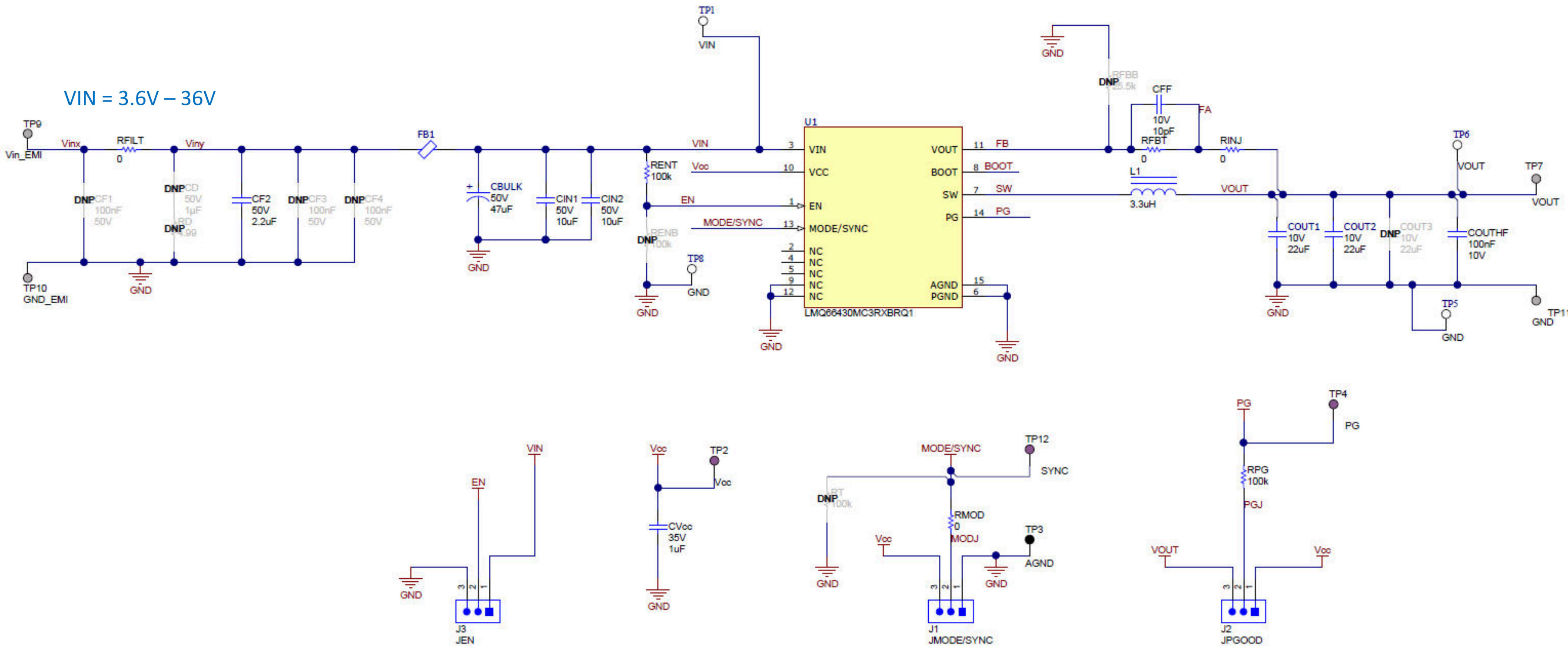

Figure 3-1. LMQ66430-2EVM Schematic

4 Board Layout

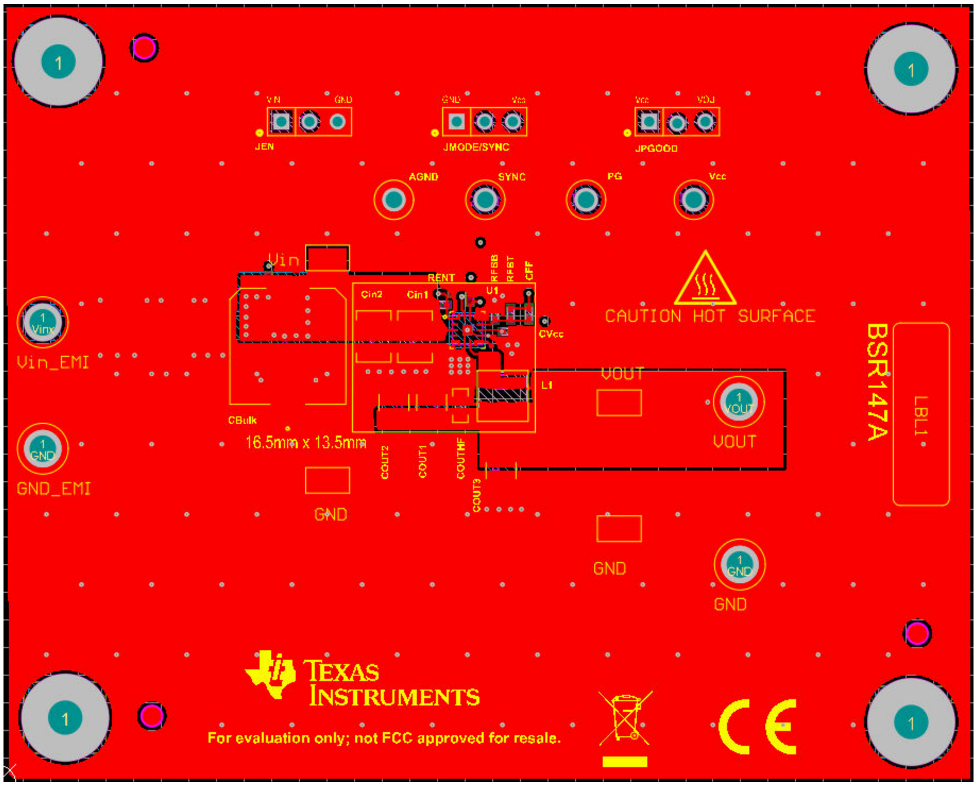

Figure 4-1. Top View of EVM

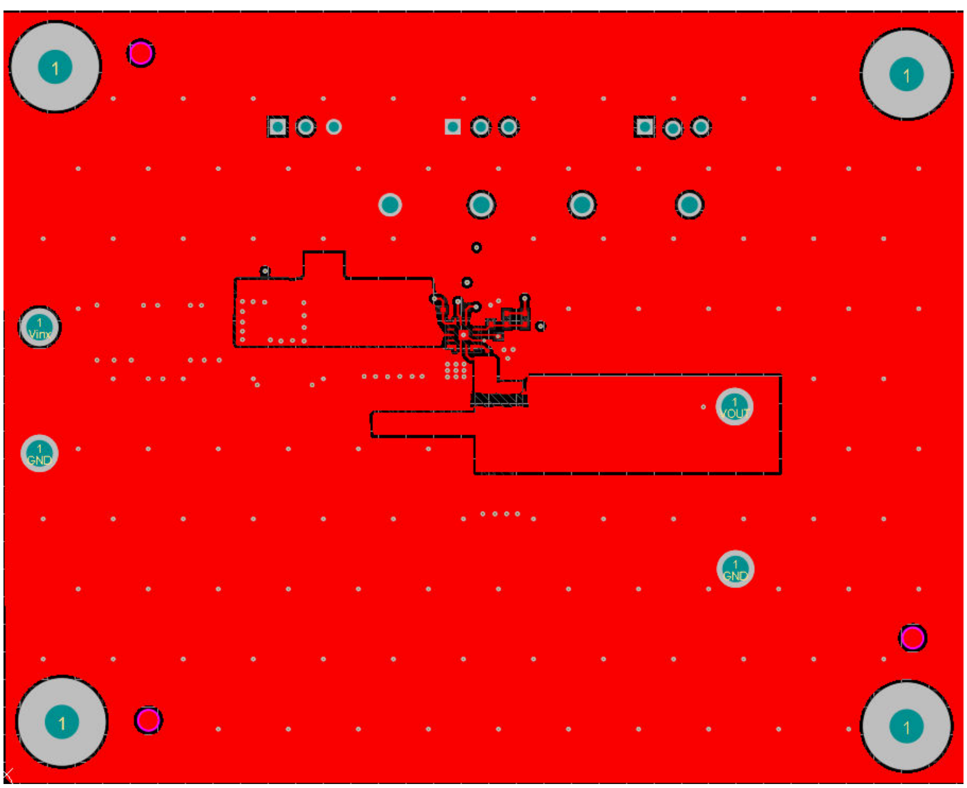

Figure 4-2. EVM Top Copper Layer

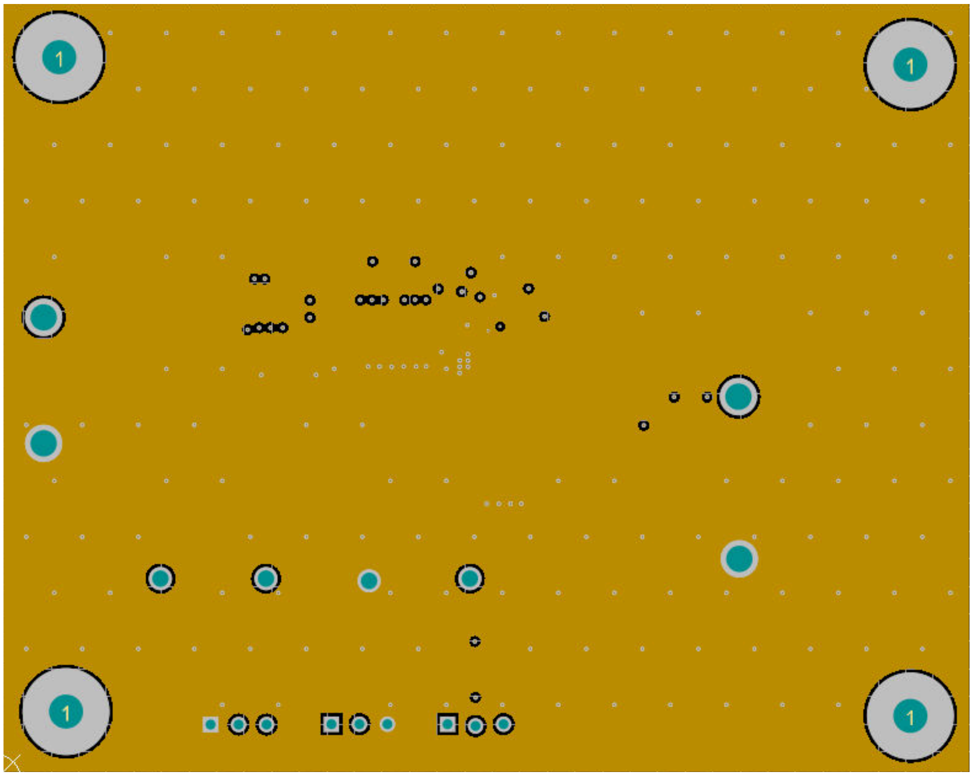

Figure 4-3. Mid-Layer One

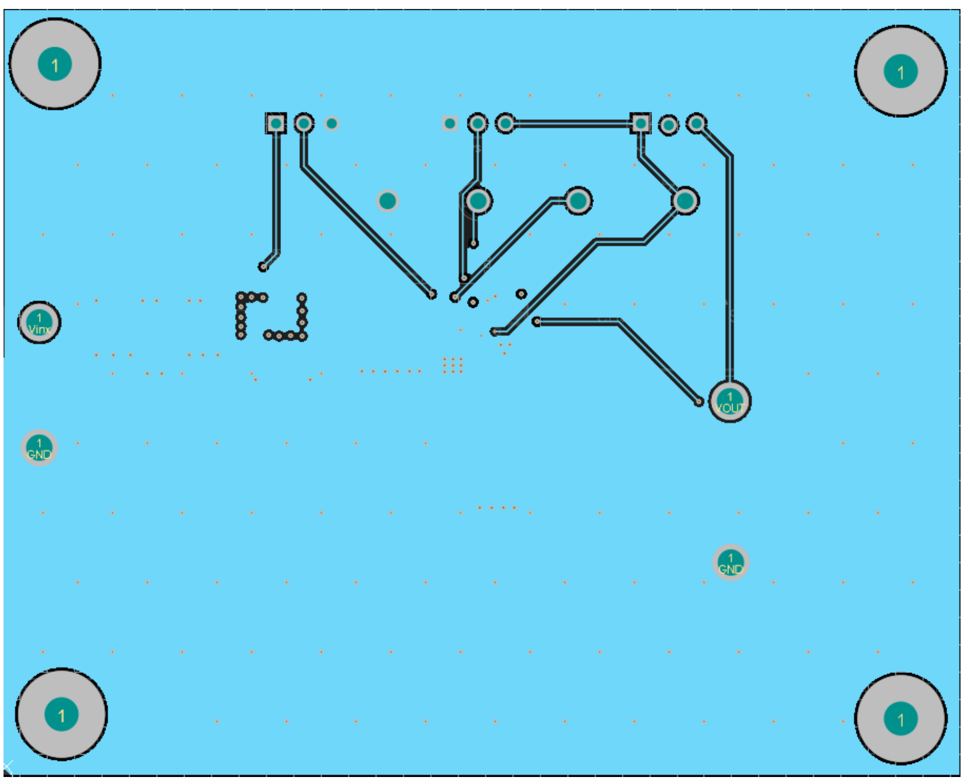

Figure 4-4. Mid-Layer Two

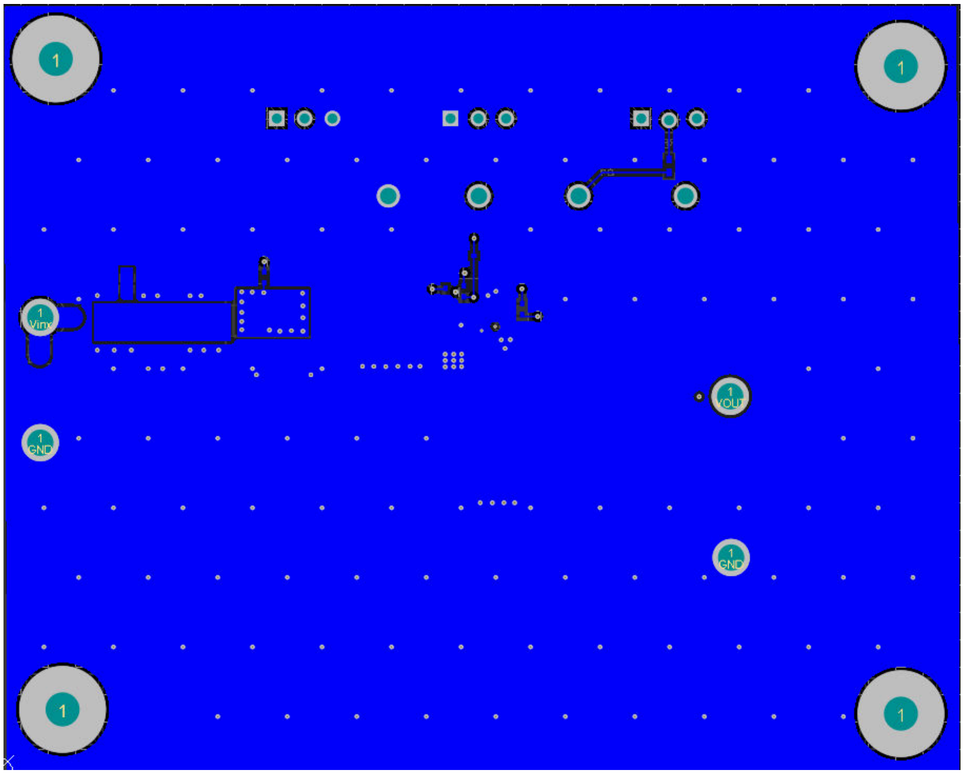

Figure 4-5. EVM Bottom Copper Layer

5 Bill of Materials

Table 5-1. Bill of Materials

Designator	Description	Manufacturer	Part number	QTY
CBULK	47-µF 50-V Aluminum Electrolytic Capacitors Radial, Can - SMD 1500 hours at 125°C	Vishay BC Components	MAL214699101E3	1
CD	CAP, CERM, 1 µF, 50 V,±20%, X5R, AEC-Q200 Grade 3, 0603	MuRata	GRT188R61H105ME13D	0
CF1, CF3, CF4	CAP, CERM, 0.1 µF, 50 V, ±10%, X7R, 0805	TDK	C2012X7R1H104K085AA	0
CF2	CAP, CERM, 2.2 µF, 50 V, ±10%, X5R, 0805	TDK	C2012X5R1H225K125AB	1
CFF	CAP, CERM, 10 pF, 10 V,±2.5%, C0G/NP0, 0402	Kemet	C0402C100C8GACTU	1
CIN1, CIN2	CAP, CERM, 10 µF, 50 V, ±10%, X7R, AEC-Q200 Grade 1, 1210	Taiyo Yuden	UMJ325KB7106KMHT	2
COUT1, COUT2	Ceramic Capacitor for Automotive 22-µF ±10% 10VDC X7R 1210 Embossed T/R	MuRata	GCM32ER71A226KE12L	2
COUT3	Ceramic Capacitor for Automotive 22-µF ±10% 10VDC X7R 1210 Embossed T/R	MuRata	GCM32ER71A226KE12L	0
COUTHF	CAP, CERM, 0.1 µF, 10 V, ±10%, X7R, 0603	AVX	0603ZC104KAT2A	1
CVcc	CAP, CERM, 1 µF, 35 V, ±10%, X5R, 0402	MuRata	GRM155R6YA105KE11D	1
FB1	1 kΩ at 100-MHz 1 Power Line Ferrite Bead 1210 (3225 Metric) 2 A 100 mΩ	Taiyo Yuden	FBMH3225HM102NT	1
FID1, FID2, FID3	Fiducial mark. There is nothing to buy or mount.	N/A	N/A	3
H1, H2, H3, H4	Machine Screw, Round, #4-40 × 1/4, Nylon, Philips panhead	B&F Fastener Supply	NY PMS 440 0025 PH	4
H5, H6, H7, H8	Standoff, Hex, 0.5"L #4-40 Nylon	Keystone	1902C	4
J1, J2, J3	Header, 100mil, 3 × 1, Tin, TH	Sullins Connector Solutions	PEC03SAAN	3
L1	Inductor, Shielded, 3.3 µH, 5 A, 0.0286 Ω, SMD	Coilcraft	XEL4030-332MEB	1
LBL1	Thermal Transfer Printable Labels, 0.650" W × 0.200" H - 10,000 per roll	Brady	THT-14-423-10	1
RENT	RES, 100 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0402	Panasonic	ERJ-2GEJ104X	1
RFBT, RINJ, RMOD	RES, 0, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	KOA Speer	RK73Z1ETTP	3
RFILT	RES, 0, 1%, 0.5 W, 1206	Keystone	5108	1
RPG	RES, 100 k, 1%, 0.0625 W, AEC-Q200 Grade 0, 0402	Yageo America	AC0402FR-07100KL	1
SH-J1	Shunt, 100 mil, Gold plated, Black	Samtec	SNT-100-BK-G	1
TP1, TP5, TP6, TP8	Test Point, Miniature, SMT	Keystone	5015	4
TP2, TP4, TP12	Test Point, Multipurpose, Purple, TH	Keystone	5129	3
TP3	Test Point, Multipurpose, Black, TH	Keystone	5011	1
TP7, TP9, TP10, TP11	Terminal, Turret, TH, Double	Keystone	1502-2	4
U1	3-V to 36-V, 3-A Synchronous Buck Converter Optimized for Ultra Low EMI and Light Load Efficiency	Texas Instruments	LMQ66430MC3RXBRQ1	1

6 Test Results

6.1 LMQ66430-2EVM Test Results

The LMQ66430-2EVM variant is used for all figures below.

6.1.1 Efficiency and Load Regulation

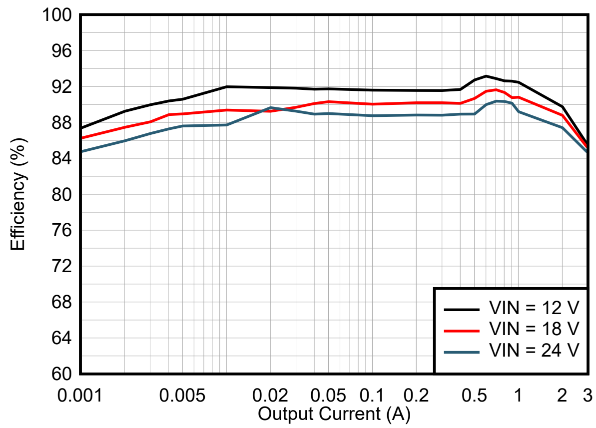

Figure 6-1. 3.3 V_{OUT}, AUTO Mode Efficiency

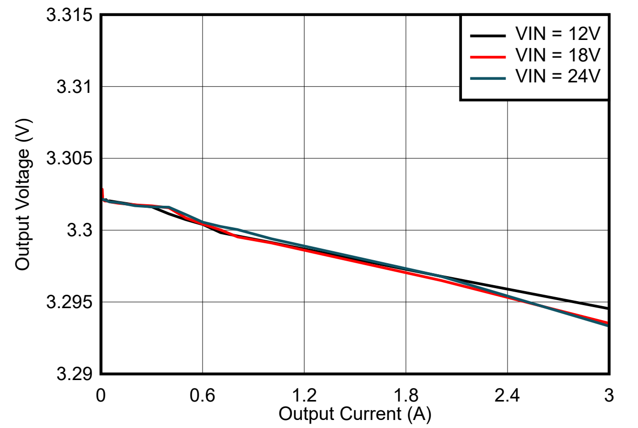

Figure 6-2. 3.3 V_{OUT}, 2.2 MHz Load Regulation

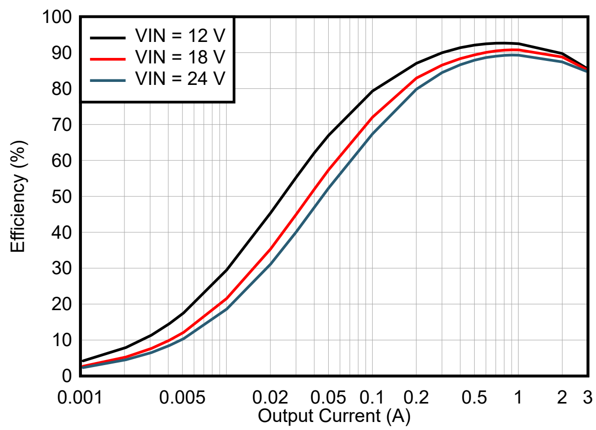

Figure 6-3. 3.3 V_{OUT}, FPWM Mode Efficiency

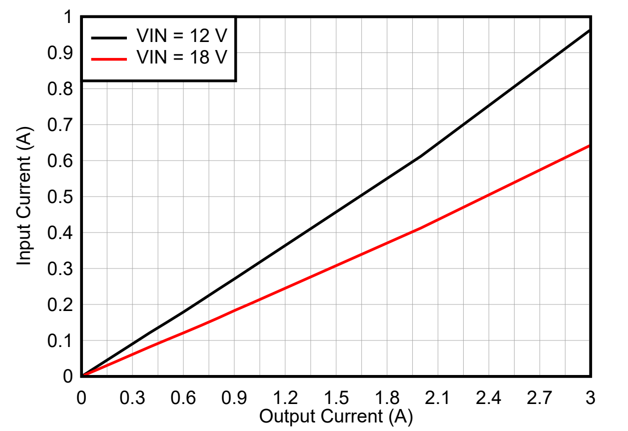

Figure 6-4. Input Current vs Load Current for 3.3 V_{OUT}

6.1.2 Load Transients

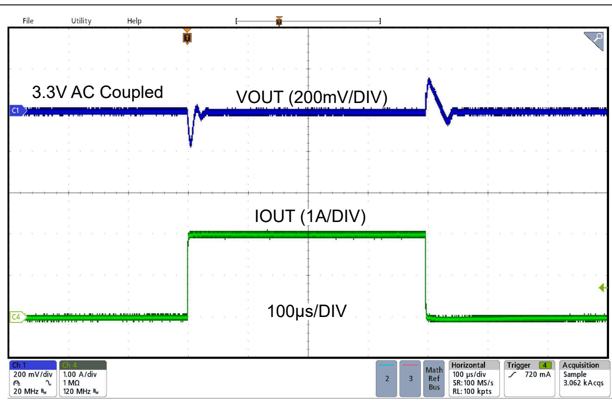

Figure 6-5. Load Transient 12 V_{IN}, 3.3 V_{OUT}, I_{OUT} = 0 A to 2 A, Slew Rate = 1 A/µs, FPWM

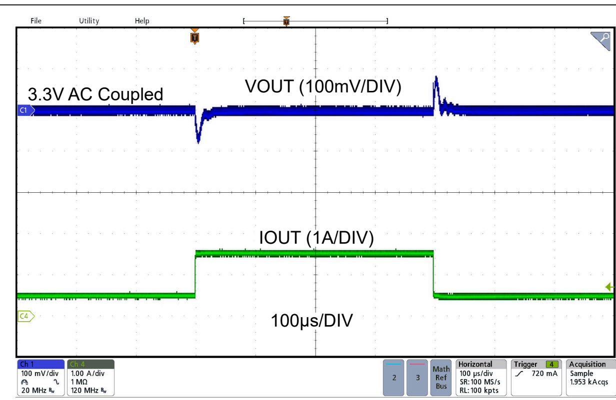

Figure 6-6. Load Transient 12 V_{IN}, 3.3 V_{OUT}, I_{OUT} = 0.5 A to 1.5 A, Slew Rate = 1 A/µs

6.1.3 Output Ripple and Thermal Picture

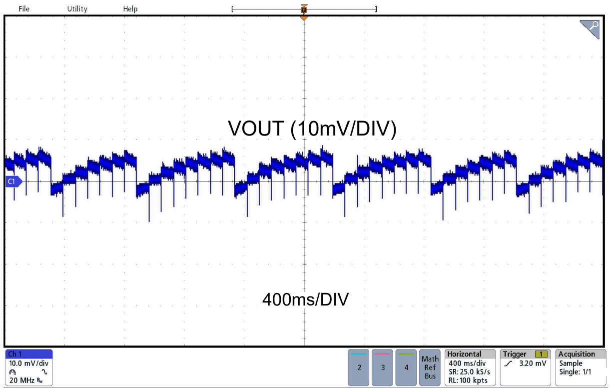

Figure 6-7. Output Ripple at 12 V_{IN}, 3.3 V_{OUT}, No Load

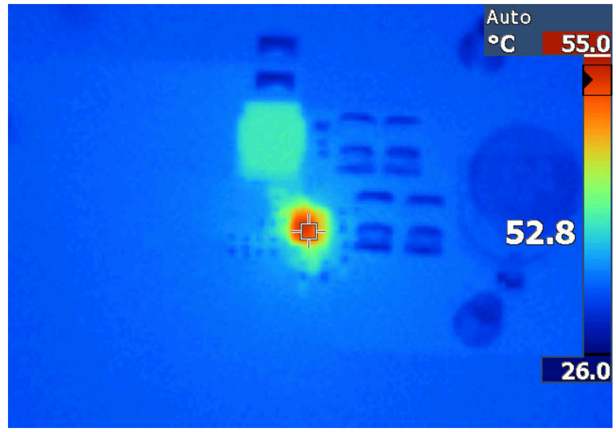

Figure 6-8. Thermal Capture, 12 V_{IN}, 3.3 V_{OUT}, 2 A Load, 2.2 MHz, $\Theta_{JA} \cong$ 40°C/W