Application Note

How to Avoid Sampling Crosstalk and Improve Accuracy in C2000 ADC

Strong Zhang

ABSTRACT

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C2000 devices feature multi-channel SAR ADCs for sampling current and voltage signals in real-time control systems. Improving ADC accuracy and avoiding crosstalk through proper selection of external circuits has always been a design challenge. Through an in-depth analysis of SAR ADCs combined with the internal ADC sample-and-hold timing control of C2000 devices, this article derives guidelines for designing external ADC driver circuits. It presents resistor-capacitor selection methods for both amplifier-based and amplifier-free designs, meeting the requirements of real-time control in terms of both accuracy and cost.

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1 Basic Principles of SAR ADCs

The operation of a SAR ADC consists of two stages: the sample-and-hold stage and the conversion and encoding stage. As shown in the SAR ADC block diagram of Figure 1-1, for a single ADC channel, there are two internal switching switches, S1 and S2. First, S1 is closed and S2 is opened. At this time, the external circuit charges or discharges the internal RC circuit of the ADC module until the voltage on capacitor C_H becomes equal to the external input voltage signal.

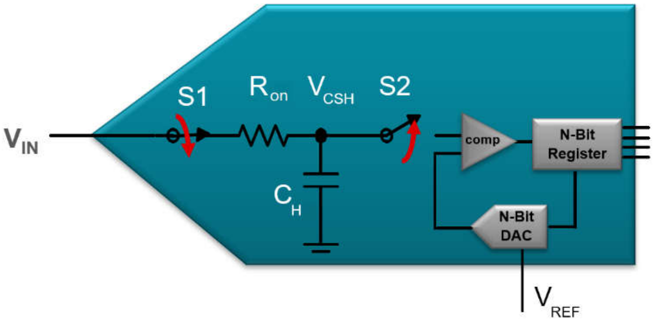


Figure 1-1. SAR ADC Block Diagram

This charging and discharging process requires sufficient time to ensure that the error between the internal capacitor voltage and the external input signal voltage is sufficiently small. Typically, the error can be designed to be within 1/2 LSB. Software can configure this sample-and-hold time. After this process is completed, it enters the conversion and encoding stage, where S2 is closed and S1 is opened.

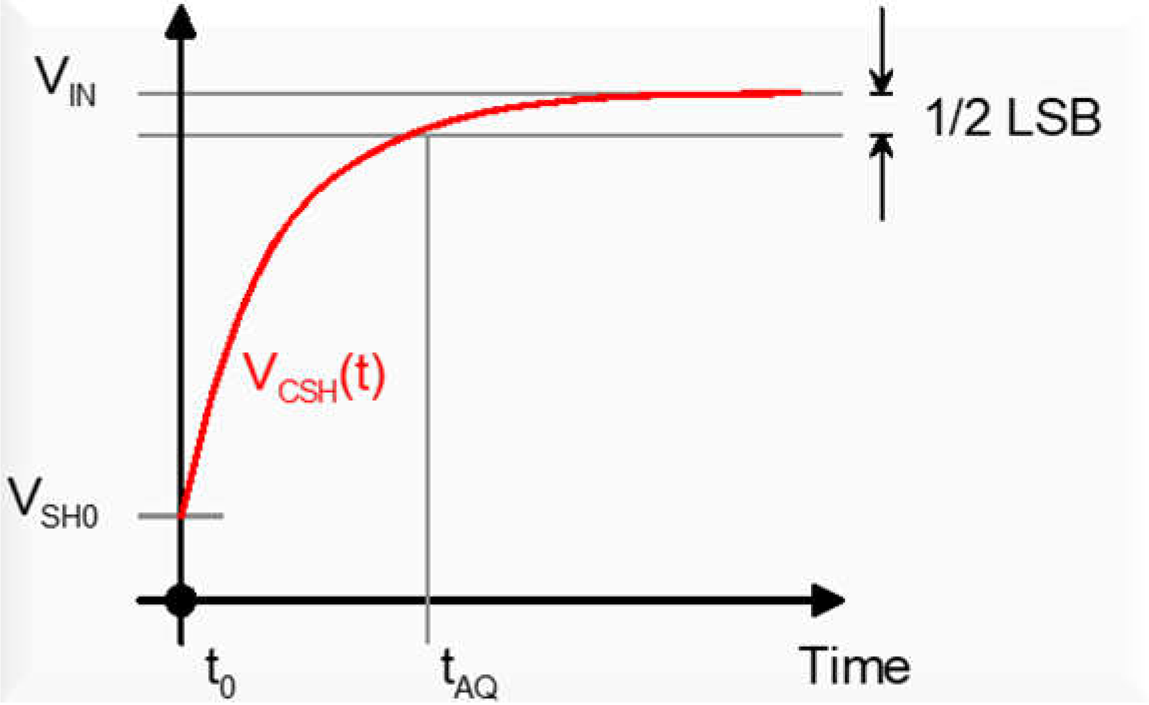


Figure 1-2. Voltage Variation During the Charging Process of Capacitor Cs

The conversion and encoding stage converts the analog voltage signal sampled during the sample-and-hold stage into a digital code. The analog input voltage signal is sequentially compared with different reference voltage levels inside the MCU, namely Vref/2, Vref/2±Vref/4, Vref/2±Vref/4±Vref/8, and so on. When the input signal voltage is greater than the reference voltage, the comparator outputs 1; otherwise, it outputs 0. By continuously comparing and generating outputs in this manner, the SAR ADC converts the analog signal into a digital signal, as shown in Figure 1-3.

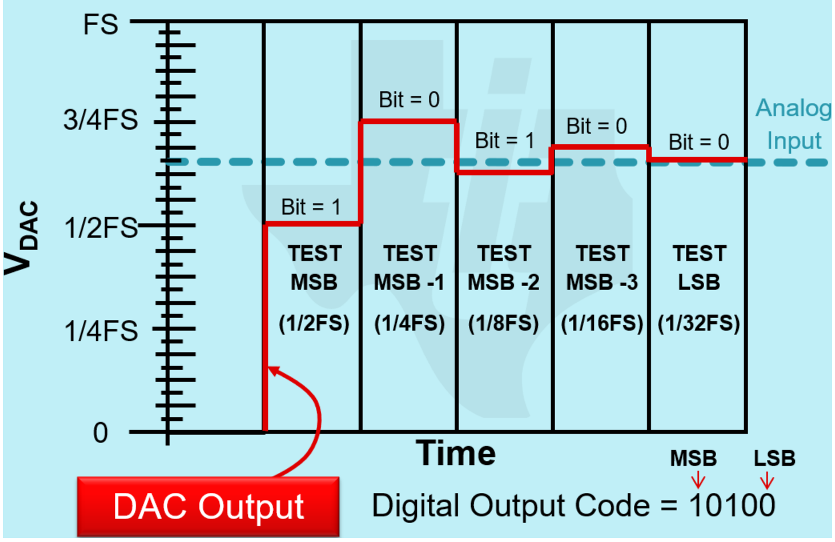


Figure 1-3. SAR ADC Conversion and Encoding Principle

2 Causes of ADC Crosstalk

For the ADC module inside an MCU, when multiple ADC channels are sampled, the internal switching circuit switches between channels and samples them sequentially. Since these channels share the same sample-and-hold circuit inside the ADC, if the sample-and-hold time is not sufficiently long, the sampled value of the current ADC channel will be affected by the input voltage of the previously sampled ADC channel, resulting in inaccurate sampling.

This error cannot be completely eliminated by oversampling and averaging. It can only be mitigated through proper ADC input circuit design and appropriate sample-and-hold time configuration.

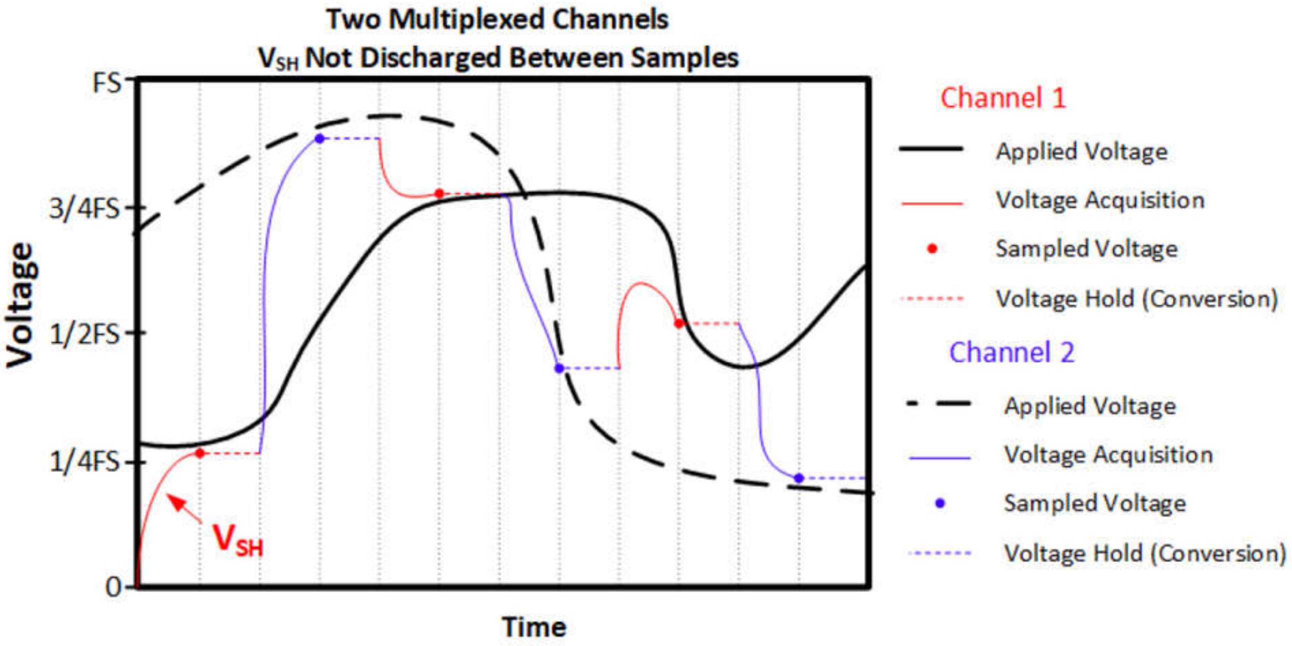


Figure 2-1. ADC Sampling Affected by the Voltage of the Previous Channel

3 Calculation of ADC Sample-and-Hold Time

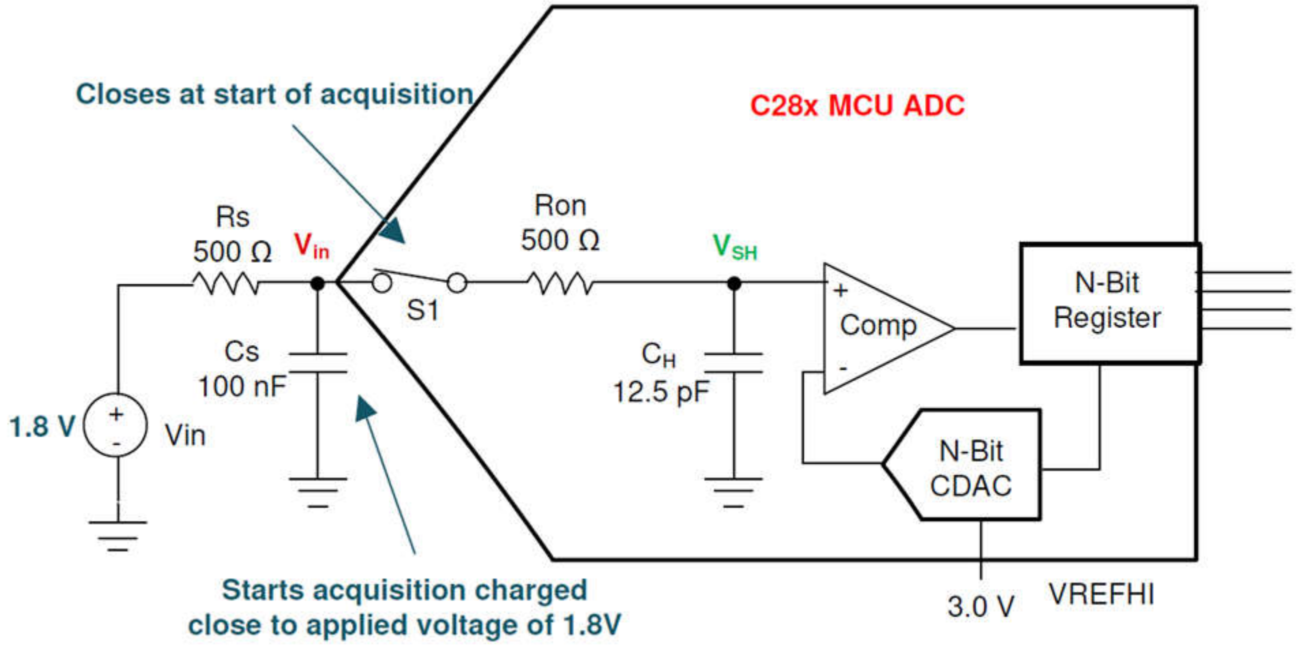


Figure 3-1. Internal ADC Circuit Model

Figure 3-1 shows a simplified model of the ADC internal circuit. Here, R_s and C_s are the external RC filter circuit components; R_{on} and C_H are the internal RC circuit components of the ADC; N is the ADC resolution in bits; and C_p is the parasitic input capacitance. In general, Cp is much smaller than the external filter capacitor C_s and can therefore be neglected in calculations.

The RC time constant of the entire circuit is:

$$\tau = (R_{on} + R_S)^*C_H + R_S{}^*(C_S + C_P) \tag{1}$$

The number of time constants required to achieve an error of 1/2 LSB is:

$$\mathrm{K} = \ln\left(2^{N+1}\right) - \ln\left(\frac{C_S + C_P}{C_H}\right) \tag{2}$$

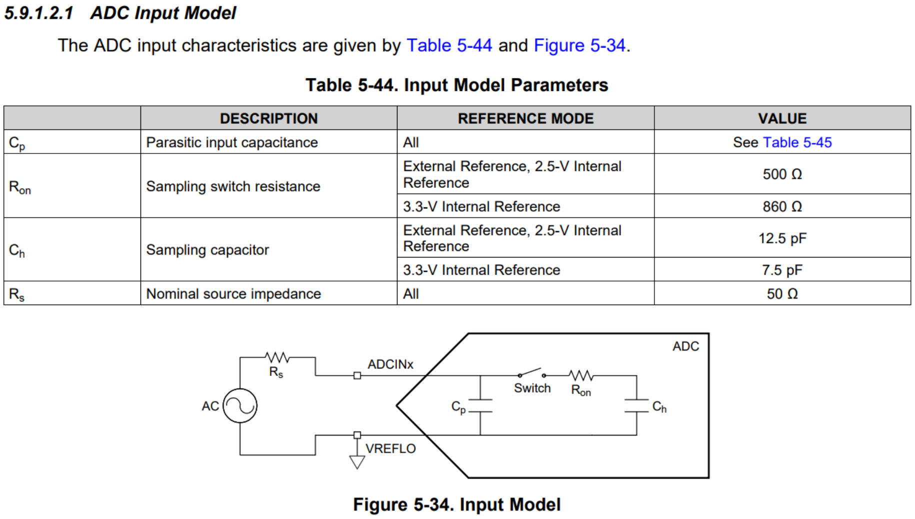
The required sample-and-hold time is:

T=K*τ

In other words, to achieve a sampling accuracy of 1/2 LSB, at least K*τ time is required.

From the above equations, it can be seen that the parameters with the greatest influence on the required sample-and-hold time T are the filter capacitor C_s and resistor R_s. The other parameters, R_{on}, C_p, and C_H, are fixed. The relationship between R_s and T is essentially linear, whereas the relationship between C_s and T is not linear.

For example, for the ADC of the F280049, when using the internal reference voltage, the datasheet provides C_H = 7.5pF, R_{on} = 860Ω, C_p = 13.7pF, and N = 12.



5.9.1.2.1 ADC Input Model

The ADC input characteristics are given by Table 5-44 and Figure 5-34.

Table 5-44. Input Model Parameters

	DESCRIPTION	REFERENCE MODE	VALUE
C_p	Parasitic input capacitance	All	See Table 5-45
R_{on}	Sampling switch resistance	External Reference, 2.5-V Internal Reference	500 Ω
		3.3-V Internal Reference	860 Ω
C_h	Sampling capacitor	External Reference, 2.5-V Internal Reference	12.5 pF
		3.3-V Internal Reference	7.5 pF
R_s	Nominal source impedance	All	50 Ω

Figure 5-34. Input Model

Figure 3-2. F280049 ADC Internal Circuit Parameters

Based on different values of R_S and C_S, the required sample-and-hold time T can be calculated.

The following are calculation results for different R_S and C_S values:

Parameter	**Example 1**	**Example 2**	**Example 3**	**Example 4**	**Example 5**	**Example 6**
Cs	820pf	10nf	100nf	10nf	1nf	100nf
Rs	100ohm	100ohm	100ohm	10Kohm	10Kohm	10Kohm
CH	7.5pf	7.5pf	7.5pf	7.5pf	7.5pf	7.5pf
Cp	13.7pf	13.7pf	13.7pf	13.7pf	13.7pf	13.7pf
Ron	860ohm	860ohm	860ohm	860ohm	860ohm	860ohm
Settling error	0.5LSB	0.5LSB	0.5LSB	0.5LSB	0.5LSB	0.5LSB
t	87.9ns	1.0us	10.0us	100.2us	10.2us	1.0ms
k	4.3	1.8	-4.9	1.8	4.1	-0.49
Settling time T	377.8ns	1.82us	-4.9us	181.8us	41.9us	-487.3us
ACQPS	38	182	7	18179	4192	7

ACQPS is equal to the number of MCU system clock cycles (SYSCLK) corresponding to the sample-and-hold time minus 1. The relationship is:

ACQPS = T / SYSCLK - 1.

ACQPS is configurable in software. For the F280049, the configuration range is 7 to 512.

The calculations above show that when R_S is fixed and C_S increases from approximately 1nf to 100nf, the sample-and-hold time first increases and then decreases, even becoming negative. A negative time indicates that the minimum sample-and-hold time is sufficient to meet the accuracy requirement, meaning ACQPS can simply be set to 7.

The sample-and-hold times calculated in Example 4 and 5 greatly exceed 512 system clock cycles, indicating that the maximum configurable ADC sample-and-hold time is insufficient, resulting in some sacrifice of sampling accuracy.

Figure 3-3 more intuitively shows the relationship between sample-and-hold time and C_S. When R_S is fixed at 100Ω and C_S varies from 1pf to 100nF, the required sample-and-hold time to achieve an error within 0.5LSB changes as follows.

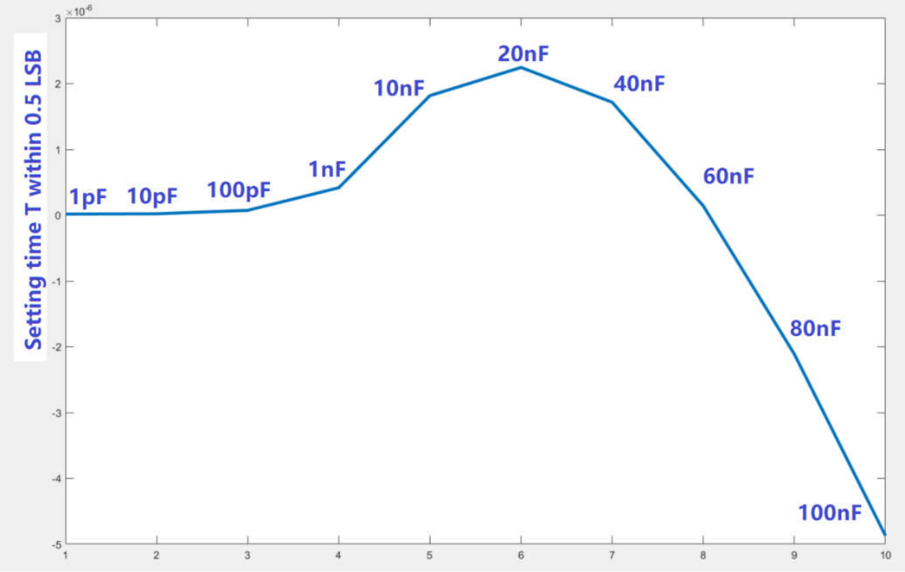


Figure 3-3. Relationship Between Sample-and-Hold Time T and Cs Capacitance

Initially, as C_s increases, the required sample-and-hold time T also increases. However, once Cs becomes relatively large, such as tens of nF, T decreases rapidly. Therefore, the filter capacitor C_s is generally designed to be either relatively large or relatively small, allowing short sample-and-hold times while maintaining sufficient sampling accuracy and avoiding the effects of crosstalk.

4 ADC External Circuit Parameter Design and Experiments

External sampling circuits can be divided into amplifier-based circuits and amplifier-free circuits. For amplifier-based circuits, the external capacitor cannot be too large because it lowers the cutoff frequency and negatively affects amplifier stability. For resistor-divider circuits without amplifiers, the external ADC impedance is relatively high, and a larger filter capacitor is often required. The capacitor should be large enough so that its stored charge alone can provide sufficient sampling accuracy during the sample-and-hold stage without requiring immediate charge replenishment from the external circuit.

4.1 Design of an Amplifier-Based RC Filter Circuit:

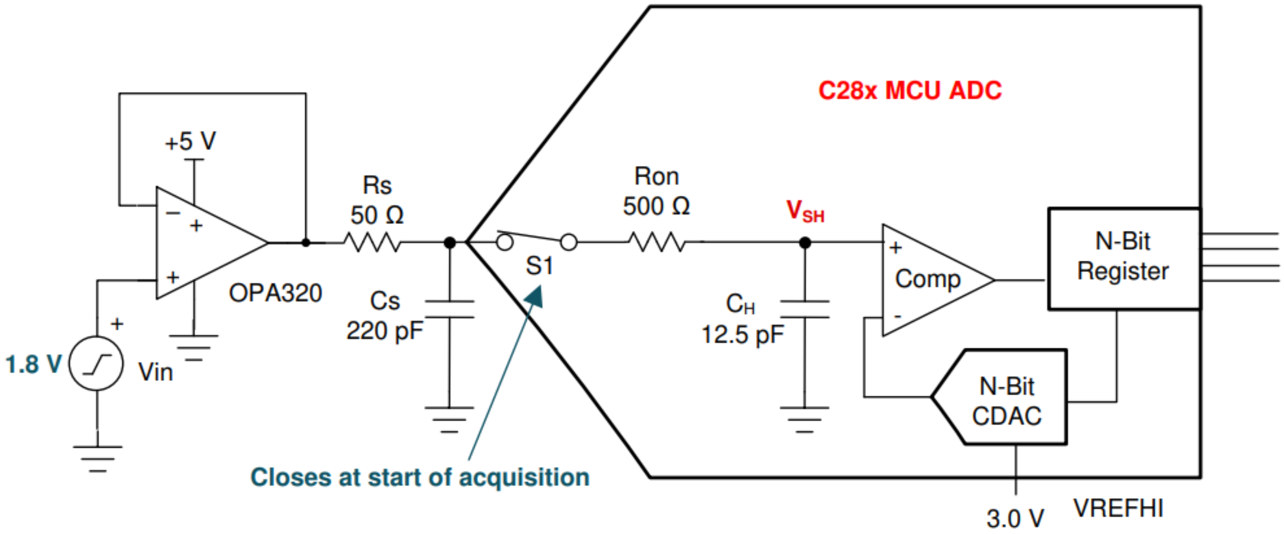


Figure 4-1. ADC Sampling Peripheral Circuit and MCU Internal ADC Circuit

Typically, C_s can be designed to be tens to hundreds of times larger than C_H, for example, 100 times larger. This ensures that during the charging and discharging process, the voltage variation across C_s is no more than 1%, while the amplifier circuit can rapidly adjust the charge and discharge, reducing the voltage error to within 1/2 LSB during the sample-and-hold period.

When using the internal reference voltage, the F280049 datasheet provides C_H = 7.5pF, R_{on} = 860Ω, C_p = 13.7pF, and N = 12.

Thus, C_s = 100* C_H = 750pF.

The number of time constants required for a 1/2LSB settling error can be calculated as:

$$\mathrm{K} = \ln\left(2^{N+1}\right) - \ln\left(\frac{C_S + C_p}{C_H}\right) = 4.39 \tag{3}$$

According to the datasheet, the minimum ADC sample-and-hold time is theoretically 75ns. Software can set ACQPS to 9, corresponding to a sample-and-hold time of T=100ns.

Thus, the RC filter time constant is:

τ=T/K=6.0 ns

Using the previous formula, the external filter resistor R_s can be calculated:

$$R_S = \tau - R_{ON}{}^{*}\frac{C_H}{C_S + C_p + C_H} = 20\Omega \tag{4}$$

Experimental Verification:

Based on the above calculations, R_s =20Ω and C_s =750pF were selected. The input voltage of the voltage follower amplifier was 2V. Software was configured to vary AQCP from 9 to 110, and the sampled value of ADC channel A1 was recorded. The resulting relationship curve is shown in Figure 4-2.

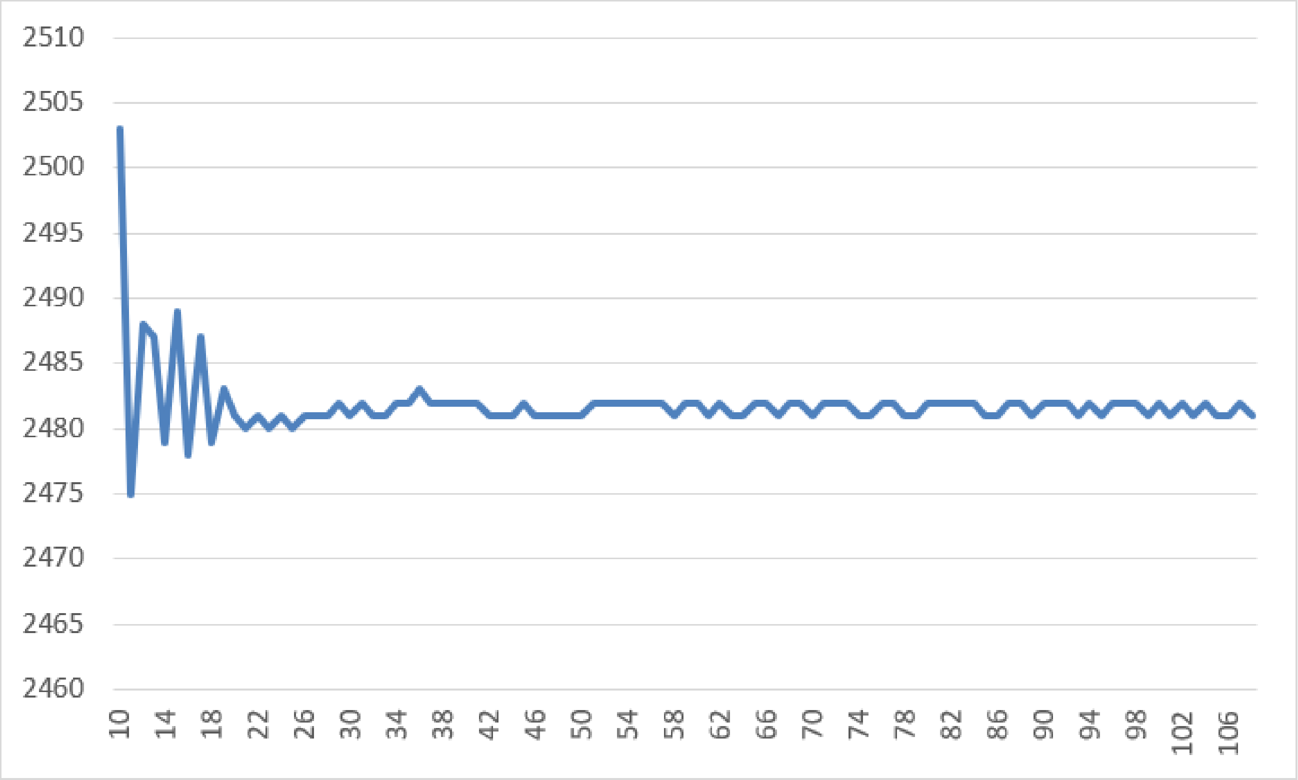


Figure 4-2. Relationship Between ADC Sample Value and Sampling Time Coefficient AQCP

Figure 4-2 shows that although the theoretical design indicates that AQCP=9 should achieve 1/2LSB accuracy, parasitic inductance in the circuit can cause oscillation in the voltage across the ADC internal capacitor C_H. Therefore, even with AQCP=9, inaccurate sampling may occur. In practice, AQCP may be configured to 20 or higher, corresponding to a sample-and-hold time above 200ns, to achieve higher sampling accuracy.

4.2 Designing a Sufficiently Large C_s Capacitor for Amplifier-Free Circuits

To reduce cost, some applications with slowly changing input signals, particularly DC voltage sampling applications, often eliminate the amplifier circuit. In such cases, C_s must be designed sufficiently large to ensure adequate sampling accuracy.

To achieve a settling error of 0.5LSB, the capacitance value of C_s can be calculated using the following formula:

$$C_s = 2^{N+1} * C_H \qquad (5)$$

For a 12-bit ADC, C_s should be 2^{13} times C_H. If C_H is 7.5pF, then C_s should be at least 61nF.

At this point, C_s is large enough that its stored charge alone can charge and discharge C_H, and the resulting voltage fluctuation remains within the 0.5LSB error range. No real-time charge replenishment from the external circuit is required. Regardless of the external filter resistor R_s value or the sample-and-hold time, the single-sample accuracy requirement can be met.

However, for repeated oversampling or very high sampling frequencies, excessive R_s values can still affect sampling accuracy. Therefore, the design must also consider sampling frequency and other factors.

In theory, the sample-and-hold time can be set to the minimum value specified in the datasheet. However, because of parasitic inductance in the circuit, oscillation may occur in the voltage across the internal ADC capacitor. Therefore, sufficient margin should be reserved by increasing the sample-and-hold time appropriately.

Experimental Verification:

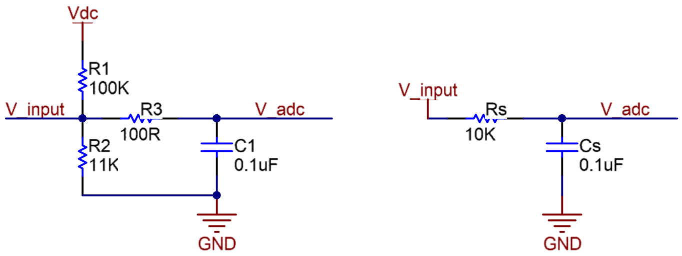


Figure 4-3. Typical Resistor Divider Circuit and Its Equivalent Circuit

A commonly used resistor-divider circuit is shown on the left side of Figure 4-3. According to Thevenin's theorem, its equivalent resistance can be calculated as:

$$R_S = (R1+R2)/R1*R2+R3=10Kohm \tag{6}$$

The equivalent R_s is essentially determined by the resistor-divider circuit. The resistance value cannot be too small; otherwise, power consumption and heat generation will increase. C_s is the adjustable parameter. In the following experiment, different C_s values were selected while using the same AQCP value of 59 (approximately 600ns sample-and-hold time), producing the following sampling results.

ADC Sampling Channel	Input Voltage	R_s	C_s	Sampling Frequency	Actual Sampled Value (LSB)	Theoretical Sampled Value (LSB)
A1	2.0V	10K	100nF	10khz	2480	2482
A1	2.0V	10K	10nF	10khz	2479	2482
A1	2.0V	10K	1nF	10khz	2462	2482
A1	2.0V	10K	10pF	10khz	2417	2482

It can be seen that when the capacitor value is large, the sampled value is relatively accurate, whereas when the capacitor value is small, the error is significant, consistent with theoretical predictions.

Therefore, selecting an appropriate capacitor C_s has a substantial impact on sampling accuracy. In practice, the value of C_s must also be considered together with cutoff frequency, sampling frequency, and other factors.

If the sampling frequency is too high, sampling accuracy will also be affected. The following table shows sampled values obtained using the same RC parameters at different sampling frequencies.

ADC Sampling Channel	Input Voltage	R_s	C_s	Sampling Frequency	Actual Sampled Value (LSB)	Theoretical Sampled Value (LSB)
A1	2.0V	10K	10nF	10khz	2479	2482
A1	2.0V	10K	10nF	100khz	2459	2482
A1	2.0V	10K	10nF	200khz	2434	2482

As shown above, higher sampling frequencies result in lower sampling accuracy. Therefore, for applications requiring high cutoff frequencies and high sampling rates, amplifier-based circuits should be considered to improve accuracy.

5 Summary

Insufficient ADC sample-and-hold time can cause crosstalk between ADC channels and degrade sampling accuracy. Because of the requirements of closed-loop real-time control systems, ADC sampling time is not necessarily better when it is longer. Therefore, proper design of the external ADC sampling circuit is essential. Different filter parameters should be selected for amplifier-based and amplifier-free circuits to ensure the required sampling accuracy.

6 References

1. Methods for Mitigating ADC Memory Cross-Talk (Rev. A)
2. Charge-Sharing Driving Circuits for ADCs

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