User's Guide

Jacinto7 EVM Quad Port Ethernet Expansion Board User's Guide

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Trademarks

1 Introduction

The Jacinto7 EVMs are development and evaluation systems that enable developers to write software and develop hardware around the Jacinto7 family of processors. The main elements of the system are available on the EVM system itself. This gives developers the basic resources needed for most general-purpose type projects that encompass the Jacinto7 processor.

Beyond the basic resources provided, additional functionality can be added via expansion cards.

This Technical User's Guide describes the hardware architecture of the Jacinto7 EVM – Quad Port Ethernet Expansion board (QP-ENET), which is interfaced with J7 EVM boards through Serial Ethernet Expansion Connector.

1.1 Key Features

Key features of QP-ENET:

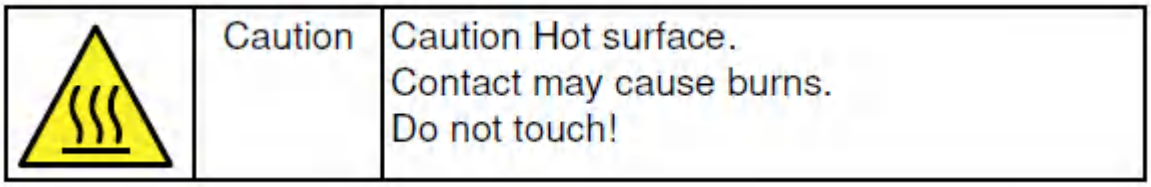
- Ethernet
  - 4x 10/100/1000Mbps - SGMII ports (VSC8514XMK-11)
- Board ID EEPROM
- Programmable Clock Generator

The orderable part number is provided in the table below:

Jacinto7 EVM Add-on Module	
Quad Port Ethernet Expansion	J721EXENETXPANEVM

1.2 Thermal Compliance

There is elevated heat on the processor/heatsink: use caution, particularly at elevated ambient temperatures. Although the processor/heatsink is not a burn hazard, caution should be used when handling the EVM due to increased heat in the area of the heatsink.



1.3 EMC, EMI, and ESD Compliance

Components installed on the product are sensitive to Electrostatic Discharge (ESD). TI recommends that this product be used in an ESD controlled environment. This may include a temperature and/or humidity controlled environment to limit the build-up of ESD. TI also recommends using ESD protection such as wrist straps and ESD mats when interfacing with the product.

The product is used in the basic electromagnetic environment as in laboratory condition and the applied standard will be as per EN IEC 61326-1:2021.

2 QP-ENET Board Identification and Installation

2.1 QP-ENET Board Component Identification

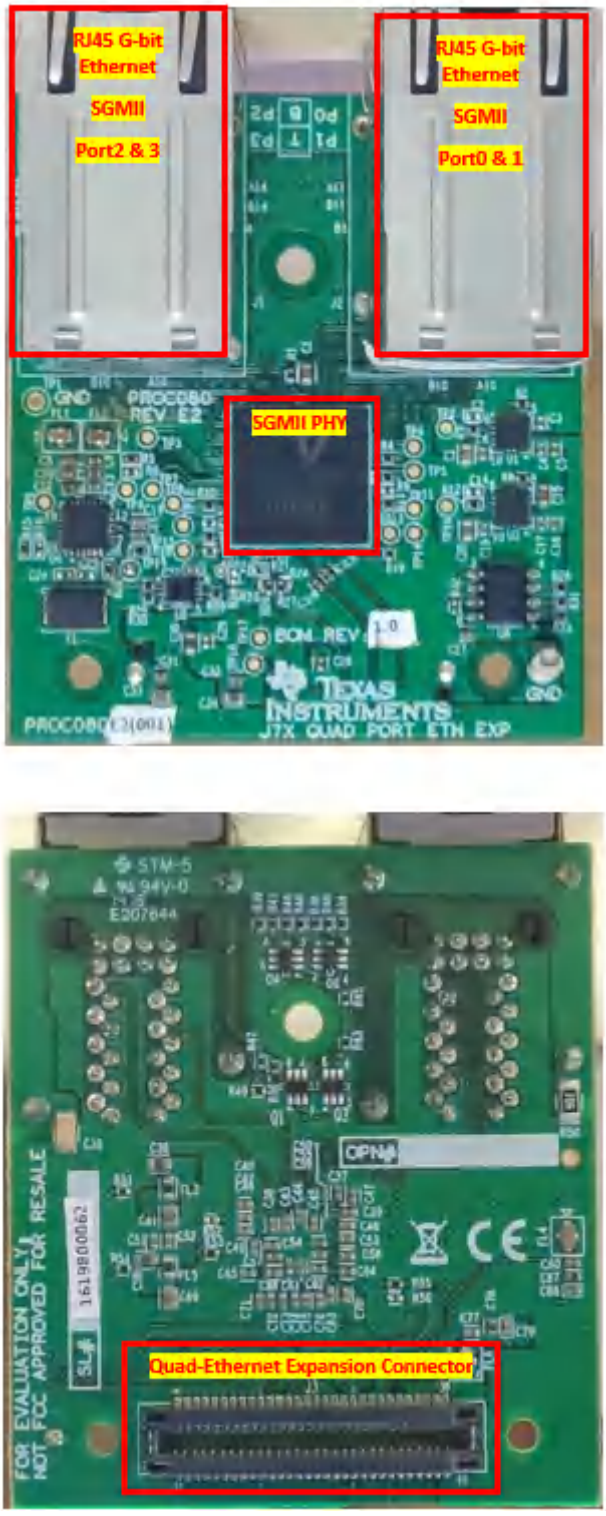


Figure 2-1. QP-ENET Expansion Board Component Identification

2.2 Interfacing QP-ENET Expansion Board with J784S4XG01EVM Board

QP-ENET Expansion boards shall be interfaced with Jacinto7 J784S4XG01EVM in bottom mating configurations. The images below show the J7AHP EVM board connectors **J51 and J52**, which mate with the QP-ENET board as an example, with expansion connectors **J3** on the QP-ENET mated to the SGMII Expansion connectors on the J7AHP EVM. It is valid to support/install on only one QP-ENET board, and in either location.

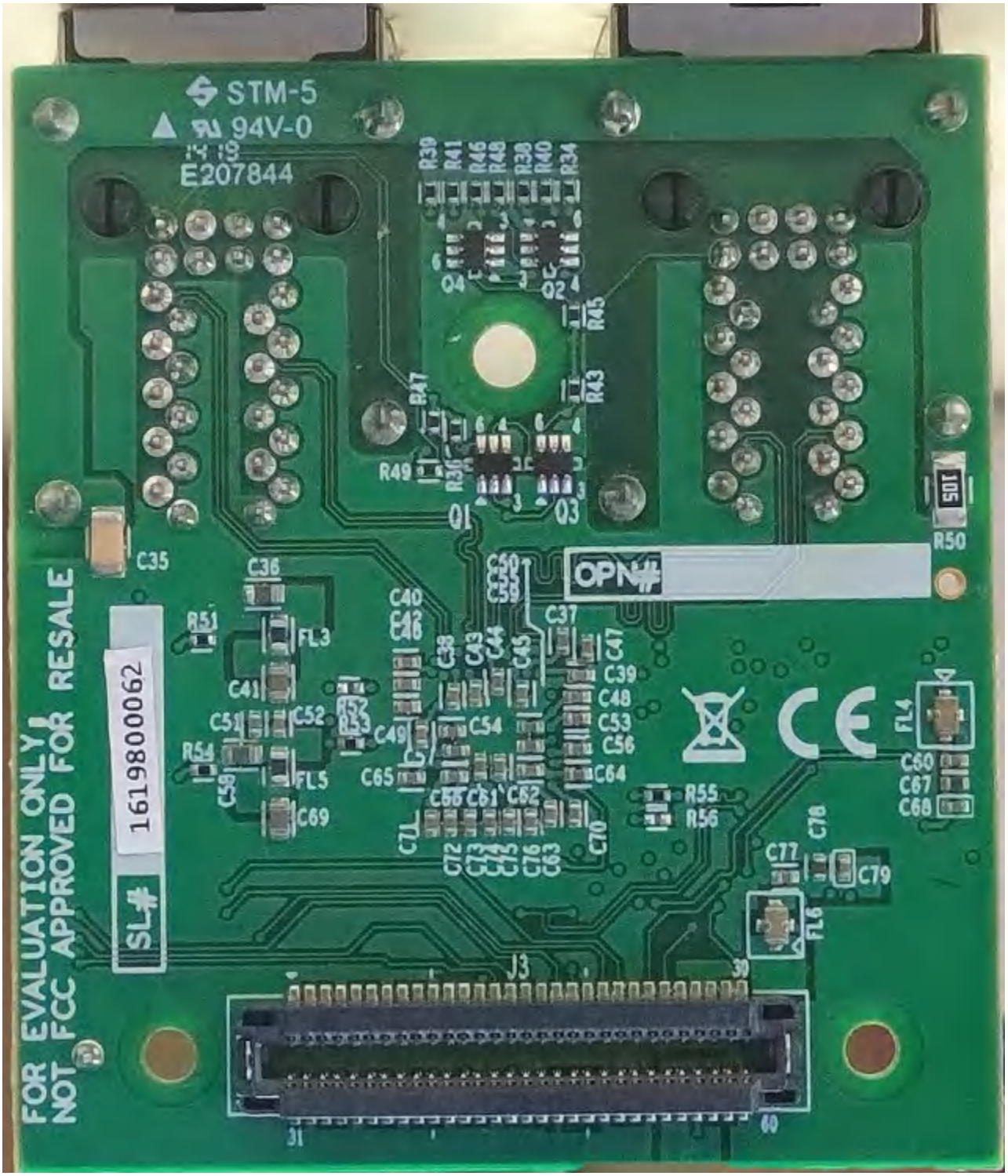


Figure 2-2. QP-ENET Expansion Board Bottom Side

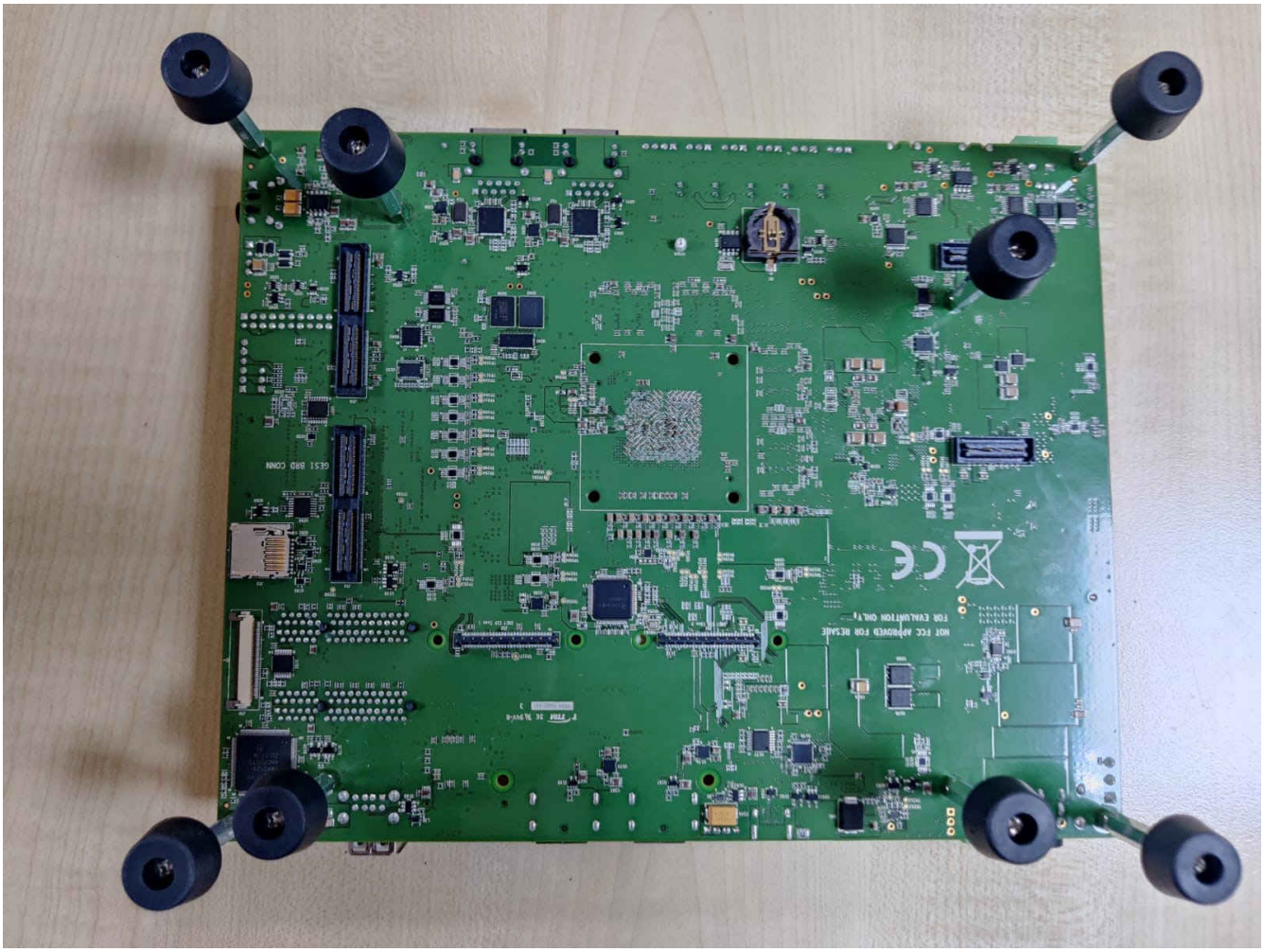


Figure 2-3. Q/SGMII Expansion Connector on J784S4XG01EVM Bottom Side

2.2.1 Detailed Board Assembly Procedure (J784S4XG01EVM)

This assembly procedure example is given for mating the QP-ENET board with the J784S4XG01EVM board.

1. Take the Assembled J784S4XG01EVM Board
2. Add M2.5 x 5mm hex spacers on each mounting holes provided on either sides of the J51 & J52 connector of the J784S4XG01EVM and secure it with M2.5 x 4 mm Phillips screws from the bottom sides to hold the spacer in place.
3. Add M3 x 12mm Phillips screws through the mounting hole provided between the Ethernet connectors on the QP ENET board (shown in the picture below) and secure it with a M3 x 5mm hex spacer from the other side (this step is done only on the QP ENET board).
4. Mount the QP board onto the J784S4XG01EVM connectors J51 & J52, making sure the connectors are seated evenly.
5. Add M2.5 x 4 mm Phillips screws from the top side of the QP to secure the QP mating with the J784S4XG01EVM board.
6. Add the M2.5 x 5 mm male to male spacer from the top side of the J784S4XG01EVM board to secure the remaining M3 screw protruding from the QP.
7. Add a M3 x 5mm spacer from the top side of the J784S4XG01EVM board to lock the other end of the M3 x12mm Phillips screw.

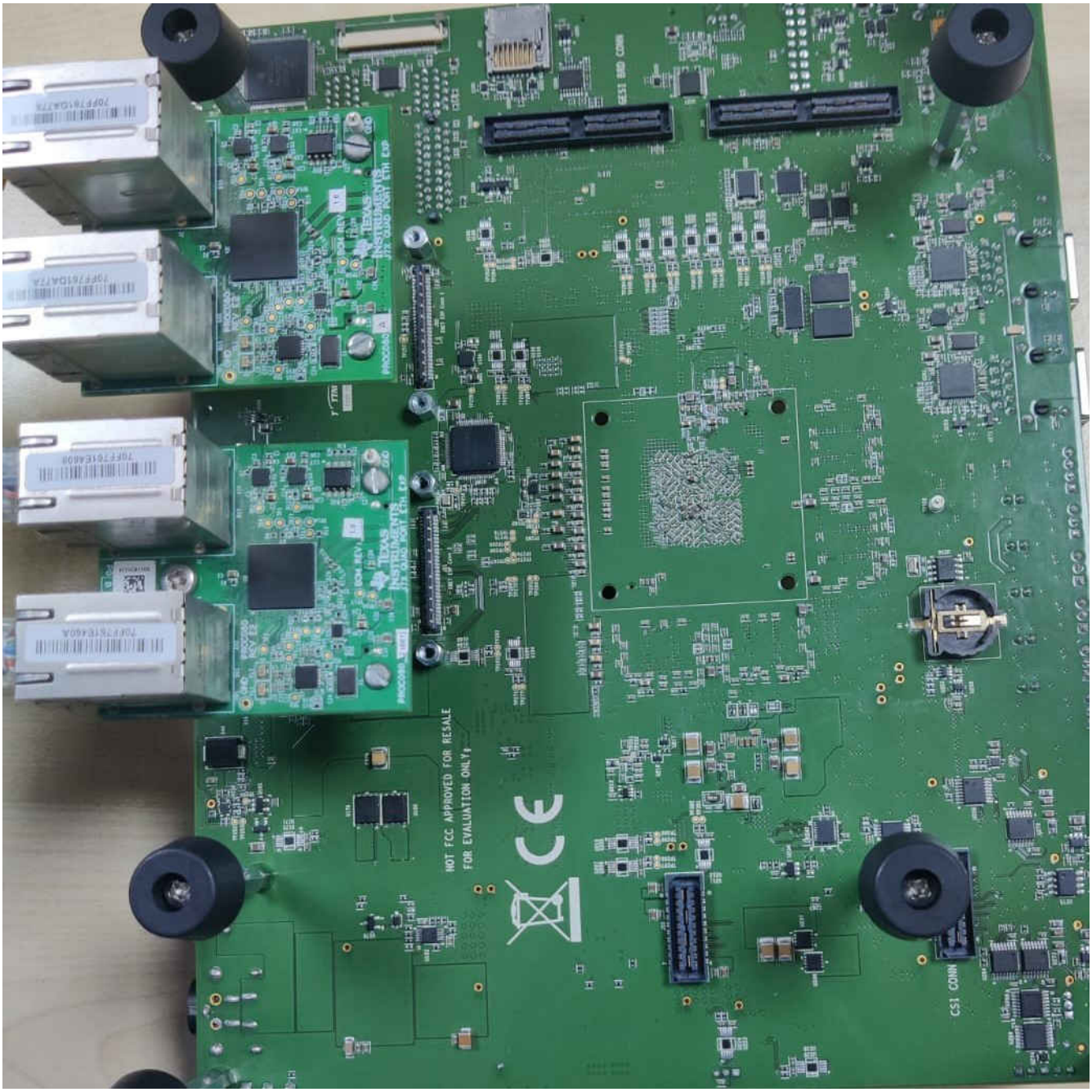


Figure 2-4. QP ENET Board

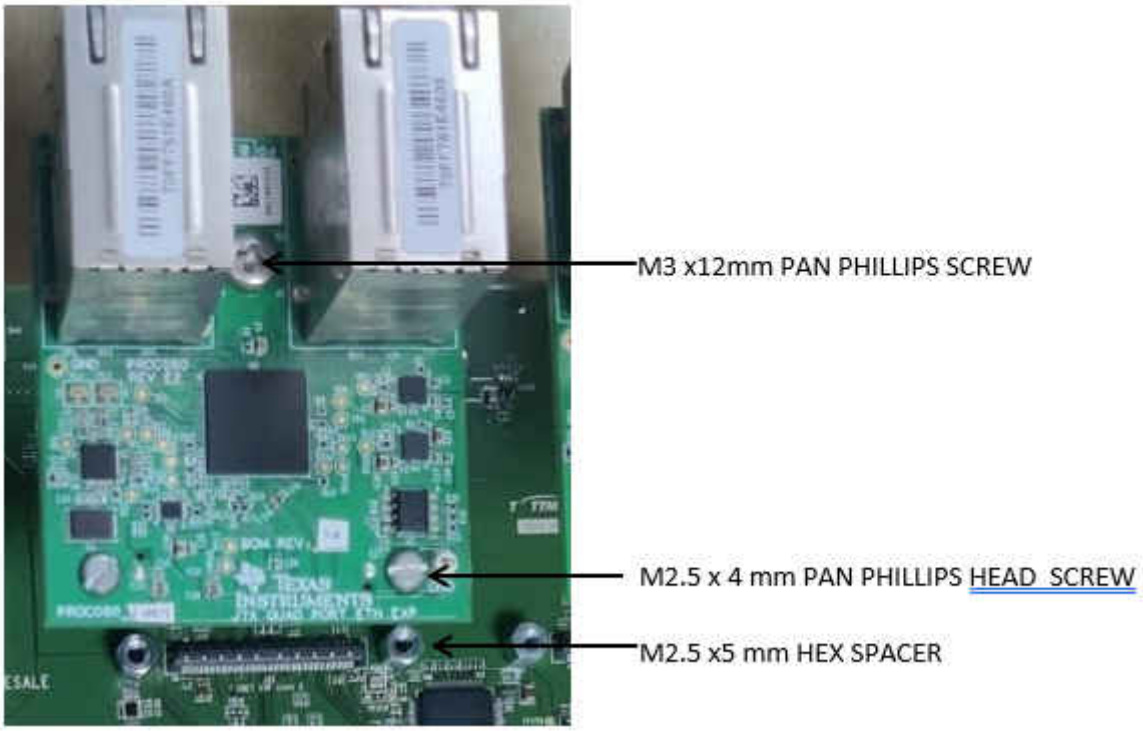


Figure 2-5. Bottom Side of J784S4XG01EVM

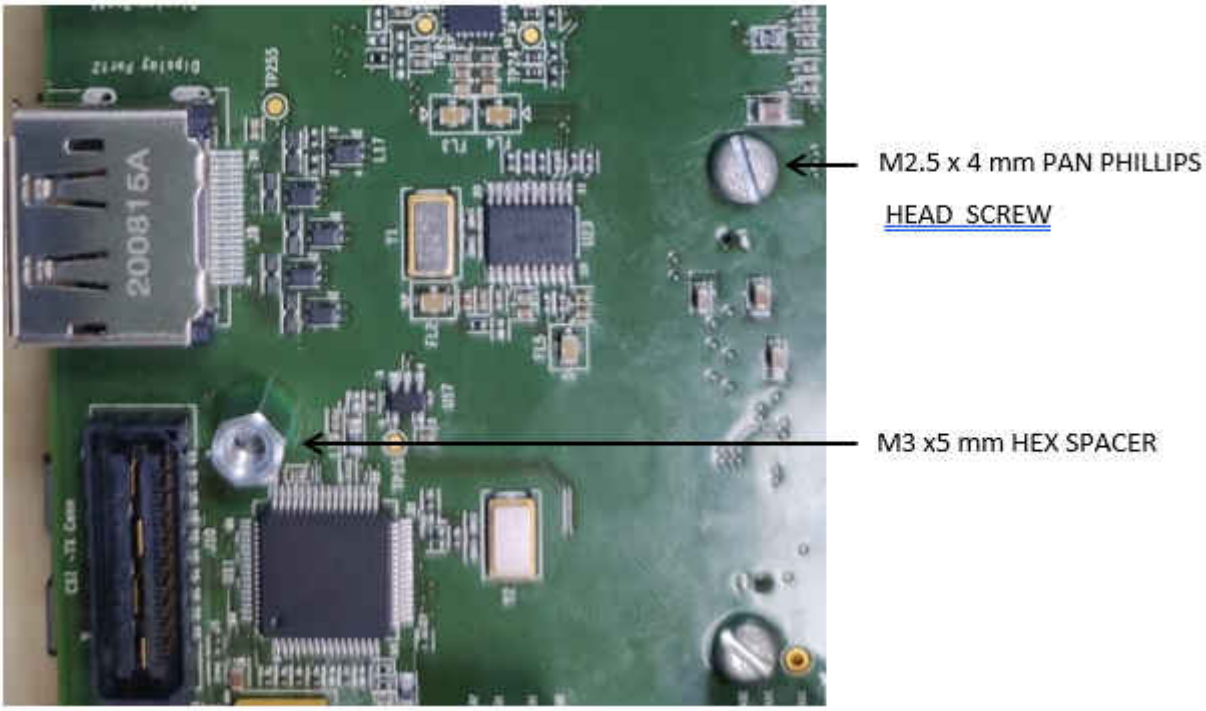


Figure 2-6. Top Side of J784S4XG01EVM

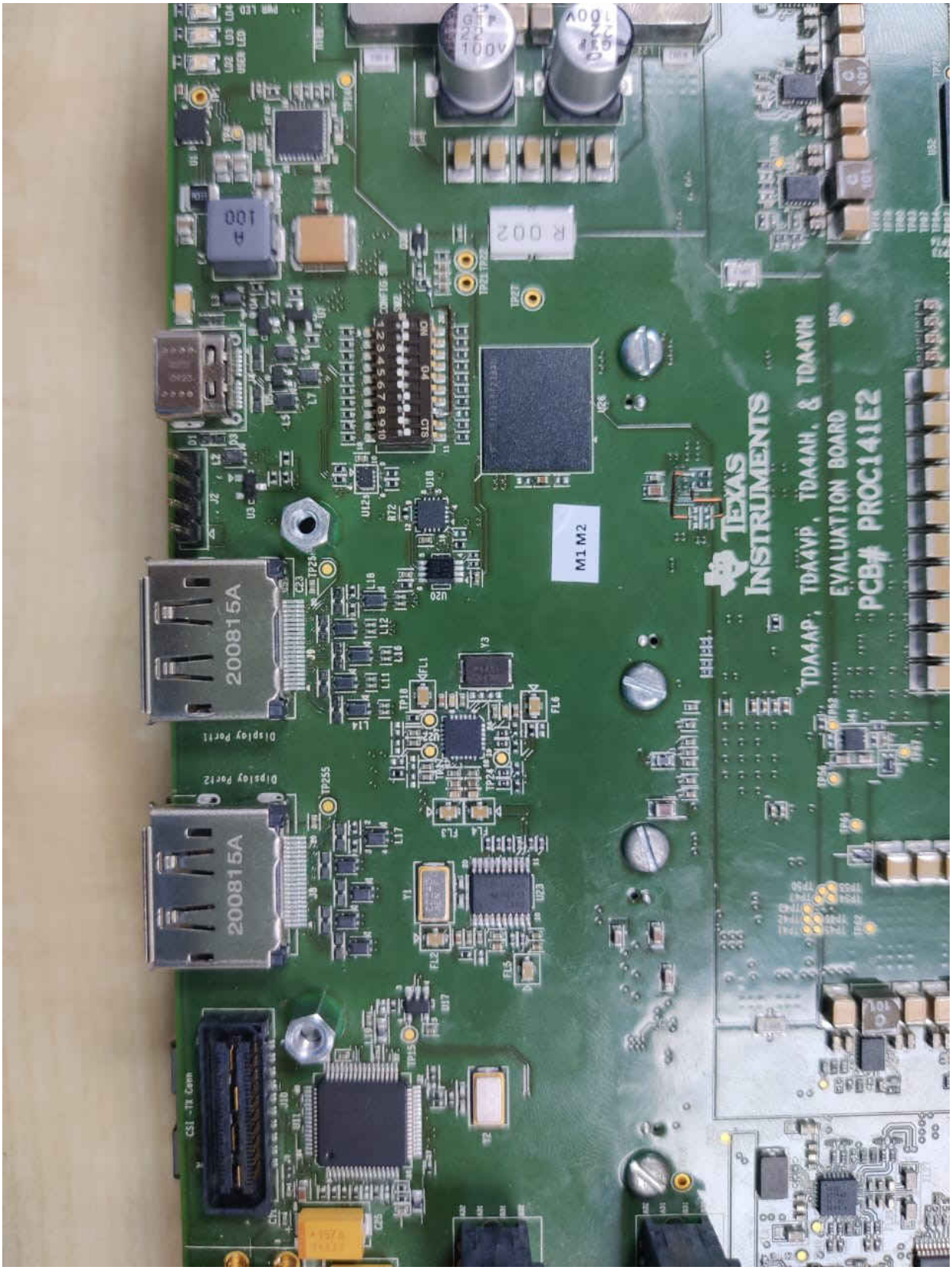


Figure 2-7. J784S4XG01EVM - QP ENET Board Assembly Procedure

3 QP-ENET Expansion Board Hardware Architecture

This section explains the Hardware Architecture of QP-ENET Expansion Board in detail.

3.1 QP-ENET Expansion Board Hardware Top Level Diagram

The generic functional block diagram of the QP-ENET Expansion Board is shown below.

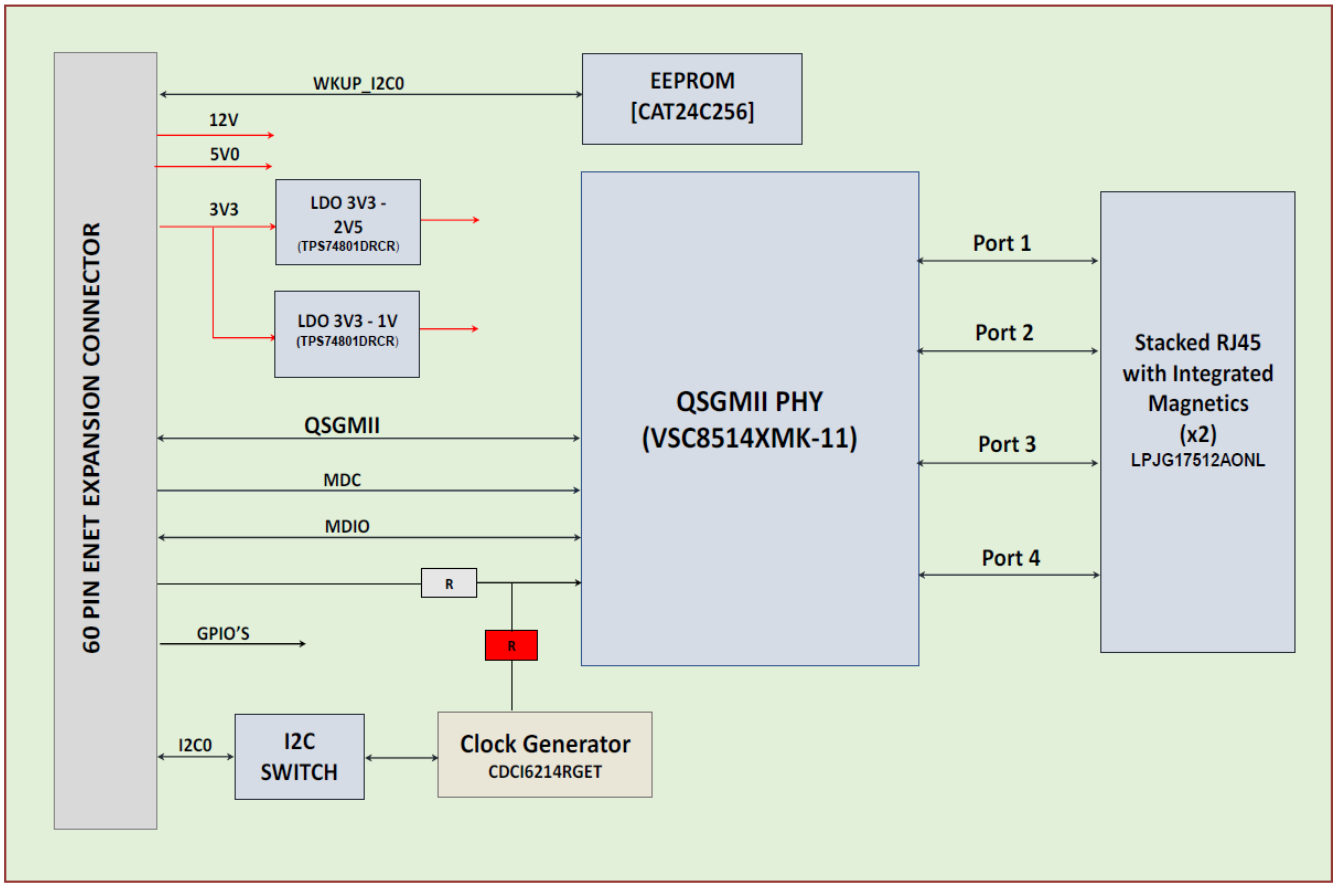


Figure 3-1. Functional Block Diagram of QP-ENET Expansion Board

3.2 Expansion Connectors

The J784S4XG01EVM board includes two Serial Ethernet Expansion connectors of 171446-1109 with 5-mm mating height, allowing the ENET expansion board (Quad-Port Ethernet Expansion) to be stacked on bottom side of the board.

This section provides an overview of the different interfaces and circuits on the Quad port Ethernet Expansion Board. The following table contains the Pin out/Signal mapping for the ENET Expansion connector.

Table 3-1. ENET Expansion Connector J3 Pinouts

PIN	Net Name	PIN	Net Name
1	DGND	31	QSGMII_INTN
2	NC	32	DGND
3	NC	33	QSGMII4_TX_P
4	DGND	34	QSGMII4_TX_N
5	NC	35	DGND
6	NC	36	QSGMII4_RX_P
7	DGND	37	QSGMII4_RX_N
8	NC	38	DGND
9	NC	39	QSGMII_PHY_REFCLK_N

Table 3-1. ENET Expansion Connector J3 Pinouts (continued)

PIN	Net Name	PIN	Net Name
10	DGND	40	QSGMII_PHY_REFCLK_P
11	VSYS_IO_3V3	41	DGND
12	VSYS_IO_3V3	42	QSGMII_MDC
13	DGND	43	QSGMII_MDIO
14	EEPROM_A0	44	DGND
15	EEPROM_A1	45	QSGMII_RESETN
16	EEPROM_A2	46	CDCI_I2C_SEL
17	DGND	47	ENET_EXP_SPARE
18	EEPROM_WP	48	DGND
19	REFCLK_25MHZ	49	VSYS_5V0
20	DGND	50	VSYS_5V0
21	WKUP_I2C0_SCL	51	DGND
22	WKUP_I2C0_SDA	52	NC
23	DGND	53	NC
24	I2C0_SCL	54	DGND
25	I2C0_SDA	55	VCC_3V3
26	DGND	56	VCC_3V3
27	VCC_12V0	57	DGND
28	VCC_12V0	58	NC
29	DGND	59	NC
30	ENET_EXP_PWRDN	60	DGND
SH1	DGND	SH2	DGND

3.3 Board ID EEPROM

The Quad port Ethernet Expansion Board is identified by its version and serial number, which are stored in the onboard EEPROM. On the J784S4XG01EVM, there are two QP-ENET expansion connectors available: one QP-ENET is set to address 0x54, the other one is set to 0x51, which are accessible on WKUP_I2C0.

The first 259 bytes of addressable EEPROM memory are preprogrammed with identification information for each board. The remaining 32509 bytes are available to the user for data or code storage.

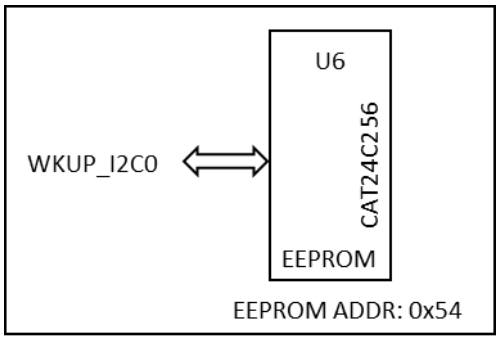


Figure 3-2. Board ID EEPROM

Table 3-2. Board ID Memory Header Information

Header	Field Name	Size (bytes)	Description
	MAGIC	4	Magic Number
	TYPE	1	Fixed length and variable position board ID header
		2	Size of payload
BRD_INFO	TYPE	1	Payload type

Table 3-2. Board ID Memory Header Information (continued)

Header	Field Name	Size (bytes)	Description
	Length	2	Offset to next header
	Board_Name	16	Name of the board
	Design_Rev	2	Revision number of the design
	PROC_Nbr	4	PROC number
	Variant	2	Design variant number
	PCB_Rev	2	Revision number of the PCB
	SCHBOM_Rev	2	Revision number of the schematic
	SWR_Rev	2	First software release number
	VendorID	2	Vendor ID
	Build_Week	2	Week of the year of production
	Build_Year	2	Year of production
	BoardID	6	Reserved. Not populated with any value
	Serial_Nbr	4	Incrementing board number
MAC_ADDR	TYPE	1	payload type
	Length	2	Size of payload
	MAC control	2	MAC header control word
	MAC_addrs	192	MAC address Contains 5 valid MAC addresses. Four MAC addresses for RGMII ports and one MAC address for RMII port.
END_LIST	TYPE	1	End Marker

These board ID details are programmed on the EEPROM from the address 0x0h.

3.4 Ethernet Interface

The Jacinto7 EVM – QP-ENET Expansion board provides an option for users to validate the Jacinto7 SoC's SGMII controllers.

The J7 EVM includes an SGMII connection between the VSC8514XMK Quad Port SGMII PHY and the network subsystem (NSS) of the processor. One channel of SGMII interfaces from the SERDES domain of the J7 processor used on the QP ENET board.

3.4.1 Quad Port SGMII PHY Default Configuration

The QP-ENET uses the PHY of the 138-pin QFN package, designated with the XMK suffix, which supports only the SGMII interface.

The VC8514 device includes three external PHY address pins, PHYADD [4:2] to allow control of multiple PHY devices on a system board sharing a common management bus. These pins set the most significant bits of the PHY address port map. The lower two bits of the address for each port are derived from the physical address of the port (0 to 3) and the setting of the PHY address reversal bit in register 20E1, bit 9.

Table 3-3. RGMII PHY Strap Configuration

Ports	SGMII Port1	SGMII Port2	SGMII Port3	SGMII Port4
Connectors	**J1A**	**J1B**	**J2A**	**J2B**
PHY Address	10010	10011	10000	10001
Auto Negotiation	Enabled	Enabled	Enabled	Enabled
ANEGSel	10/100/1000	10/100/1000	10/100/1000	10/100/1000
CLK_SQUELCH	No RCVRD Clock	No RCVRD Clock	No RCVRD Clock	No RCVRD Clock

3.4.2 SGMII Clocking Scheme

3.4.2.1 Main Clock

The reference clock to the PHY is generated from TI's Clock Generator Mfr. Part Number# CDCI6214RGET, which is placed on the J7AHP EVM Board. Clock inputs are AC coupled and LVDS compliant. The clock generator can be configured by I2C0 of the J7AHP SoC. The I2C address of this clock generator is 0x77.

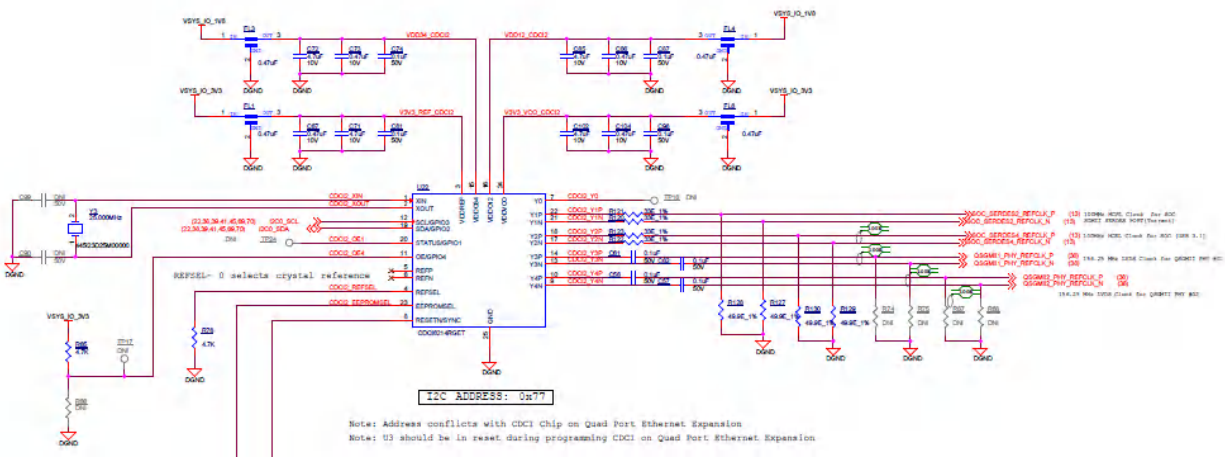


Figure 3-3. Default Clock Source on J7AHP EVM Board

3.4.2.2 Optional Clock

Optionally, the reference clock can be supplied by the SERDES clock generator Mfr. Part Number# CDCI6214RGET located on QP-ENET Board, which can be configured by I2C0 of the J7 SOC. The I2C address of this clock generator is 0x77, and this address conflicts with the CDCI Chip on EVM Boards. An I2C switch on the Quad port Ethernet Expansion Board is used to remove the address conflict by connecting any one of the clock generators.

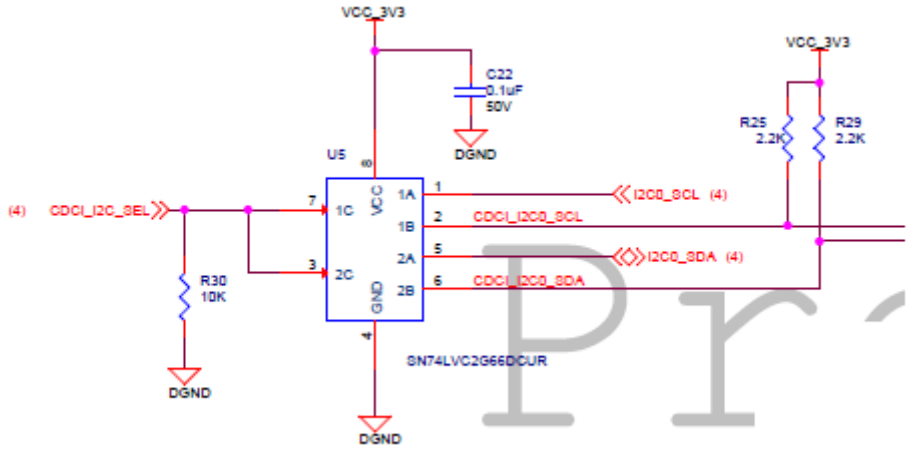


Figure 3-4. Clock Source I2C MUX

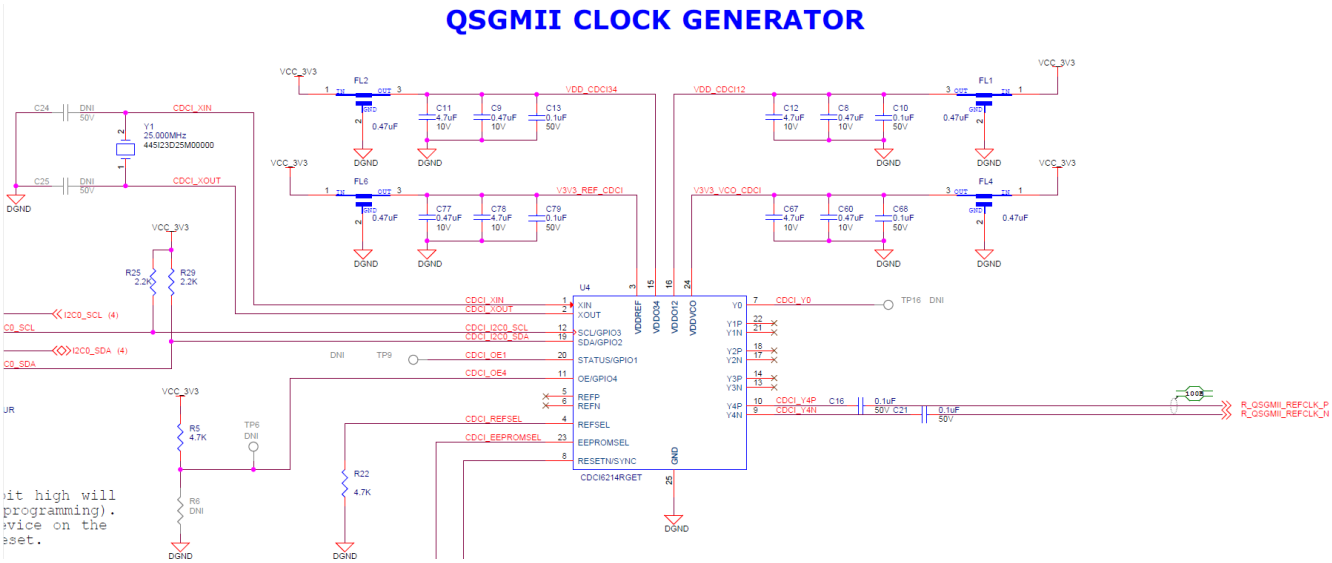


Figure 3-5. QP-ENET Optional Clock Source

Setting the CDCI_I2C_SEL IO EXP bit high will connect the I2C bus to CDCI (for programming) on the Quad Port Ethernet Expansion Board. During this time, the CDCI device on the EVM boards should be in reset mode. Also, there are resistor options provided that must be adjusted to reflect any change in source clock selection; this is given in the following images.

CLOCK SOURCE SELECTION

	Install	Remove	
From on board Clock Generator	R3,R4	R1,R2	
From CP Board	R1,R2	R3,R4	(default)

Figure 3-6. SGMII PHY Clock Input Source Path Selection

Reference Clock Selection

REFCLK_SEL1	REFCLK_SEL0	Frequency
0	0	125MHz
1	0	156.25MHz (default)

Figure 3-7. SGMII PHY Clock Configuration

3.4.3 Ethernet Port LED Indication

The following table shows the LED function of the SGMII ports RJ45 connectors. The Right LED gives the indication of link status and collision presence; if the LED is turned OFF then its means that the link is established in half-duplex mode, or no link established. If the LED is turned ON then the link is established in full-duplex mode. If the LED is blinking or pulse-stretching, then it means the link is established in half-duplex mode but collisions are present. The Left LED gives speed and activity status; if LED is blinking or pulse-stretching it denotes link activity and if not then no activity.

Table 3-4. SGMII Ports LED Function

RGMII Port RJ45-LED	FUNCTION
RIGHT - YELLOW	Duplex/Collision
LEFT - GREEN	10/1000Mbps Speed/Activity
LEFT - ORANGE	100Mbps Speed/Activity

3.4.4 Reset and Power-down Signals

The Reset signal on QP-ENET, QSGMII_RESETz is a reset signal sourced from EVM boards. This signal is used to reset the QSGMII PHY on the board.

QSGMII_RESETz is an AND output of the SOC PORz signal and ENET reset signal. The ENET reset signal is asserted by an I2C GPIO Expander2 (I2C ADD# 0x22, I2C0) on the EVM boards.

The Power-down signal on QP-ENET, ENET_EXP_PWRDN is given by the I2C GPIO Expander2 (I2C ADD# 0x22, I2C0) on the EVM boards; this signal is used to put SGMII PHY on the QP-ENET board to inactive state. By default, this signal has a pull-up on the EVM board, i.e. the PHY is in active state all the time unless low is asserted on this signal.

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
January 2023	*	Initial Release

A Appendix

A.1 Appendix – I (Interface Mapping)

J721EXSOMG01EVM, J7200XSOMG01EVM, and J784S4XG01EVM Interface Mapping on QP-ENET Expansion is provided in the following table.

Table A-1. Interface Mapping

QP-ENET Peripheral	QP-ENET Interface	J721EXSOMG01EVM Connectivity	J7200XSOMG01EVM Connectivity	J784S4XG01EVM Connectivity
SGMII(U2)	SERDES Signals	SERDES0_TX/RX1 Port	SERDES0_TX/RX2 Port	SERDES2_TX/RX2 on ENET Conn1 , SERDES2_TX/RX3 on ENET Conn2
	MDIO Signals	MDIO0	MDIO0	MDIO1
Board ID EEPROM (U6)	Configuration I2C	WKUP_I2C0	WKUP_I2C0	WKUP_I2C0
CLOCK GENERATOR(U4)	Configuration I2C	I2C0	I2C0	I2C0

A.2 Appendix – II (QP-ENET Board GPIO Mapping)

QP-ENET GPIO Mapping is shown in the following table.

Table A-2. QP-ENET GPIO Mapping

QP-ENET Peripheral	Peripheral IO	Direction (for SoC)	Default	Active State	J721EXSOMG01EVM Connectivity	J7200XSOMG01EVM Connectivity	J784S4XG01EVM Connectivity
SGMII Port 0, Port1 Port 2 & Port3	Interrupt	Input	PU	Active Low	GPIO1_22	GPIO0_4	WKUP_GPIO0_84, WKUP_GPIO0_85
	Power Down	Output	PU	Active High	I2C GPIO EXPANDER2(U31.P20 , I2C0)	I2C GPIO EXPANDER2(U31.P20 , I2C0)	I2C GPIO EXPANDER2(U173.P20 , I2C0)
	Reset	Output	PD	Active Low	I2C GPIO EXPANDER2(U31.P21 , I2C0)	I2C GPIO EXPANDER2(U31.P21 , I2C0)	I2C GPIO EXPANDER2(U173.P20 , I2C0), I2C GPIO EXPANDER2(U173.P11 , I2C0)
	I2C MUX select	Output	PD	Select Signal	I2C GPIO EXPANDER2(U31.P22 , I2C0)	I2C GPIO EXPANDER2(U31.P22 , I2C0)	I2C GPIO EXPANDER2(U173.P22 , I2C0), I2C GPIO EXPANDER2(U173.P01 , I2C0)
	Spare GPIO	Input/ Output	NA	NA	I2C GPIO EXPANDER2(U31.P23 , I2C0)	I2C GPIO EXPANDER2(U31.P23 , I2C0)	I2C GPIO EXPANDER2(U173.P23 , I2C0), I2C GPIO EXPANDER2(U173.P12 , I2C0),

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けていないものがあります。 技術適合証明を受けていないもののご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。 日本テキサス・インスツルメンツ株式会社

東京都新宿区西新宿 6 丁目 2 4 番 1 号

西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT, REGARDLESS OF WHEN MADE, CONCEIVED OR ACQUIRED.

7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

   8.1 *General Limitations*. IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS OR THE USE OF THE EVMS , REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN TWELVE (12) MONTHS AFTER THE EVENT THAT GAVE RISE TO THE CAUSE OF ACTION HAS OCCURRED.

   8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY USE OF AN EVM PROVIDED HEREUNDER, INCLUDING FROM ANY WARRANTY, INDEMITY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS, , EXCEED THE TOTAL AMOUNT PAID TO TI BY USER FOR THE PARTICULAR EVM(S) AT ISSUE DURING THE PRIOR TWELVE (12) MONTHS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

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