EVM User's Guide: AM2754, AM2754-Q1, AM2752, AM2752-Q1

AM275x Evaluation Module User's Guide

Description

The AM275x evaluation module (EVM) is a standalone test, development and evaluation platform that lets developers evaluate AM275x functionality and develop prototypes for a variety of applications. The AM275x EVM is equipped with an AM275x microcontroller along with additional components to allow the user to make use of the various device interfaces including the Ethernet™, dual CAN-FD and others to easily create prototypes. Onboard current measurement capabilities are available to monitor power consumption for power-conscious applications. The supplied USB cable paired with embedded emulation logic allows for emulation and debugging using standard development tools such as Code Composer Studio™ (CCSTUDIO).

Features

- Powered through two 5V, 3A USB Type-C® input
- Multirail power supply designed for safety-relevant Applications
- Multi-channel stereo ADC and DAC input/output lines.
- Two Audio expansion connectors
- Two Ethernet add-on board connector for an automotive or industrial Ethernet PHY
- On-board XDS110 debug probe
- Four push buttons:
  - PORz
  - RESETz
  - User Interrupt
  - IO Retention Wake
- Two LEDs for user testing
- CAN connectivity with on-board CAN transceiver
- MMC interface to micro SD card connector
- On-board memory
  - 512Mb OSPI NOR flash
  - 1Kb I2C EEPROM
  - 512Mb HYBERBUS HYPERRAM
  - 256Gb eMMC™ Flash

Table of Contents

1 Evaluation Module Overview

1.1 Introduction

The AM275x EVM was developed to enable easy and rapid prototyping of the AM275 EVM and all of the peripherals. There are several onboard transceivers and PHYs to enable the many interfaces of the AM275x SoC (System on a Chip). This user's guide details the design of the EVM and how to properly use each interface. The user's guide also details many important aspects of the board including but not limited to pin header descriptions, test points, and mux/switch signal routing.

1.2 Preface Read This First

1.2.1 Important Usage Notes

Note

This is the second revision of the User Guide. For any questions or points of clarity, refer to E2E®.

Note

If only the red power status LED (LD14) is on during power-up then the connected power supply is not able to successfully negotiate power delivery with the PD controller on the EVM. This means that the power-up sequence is not initiated and that connecting to the SoC is not possible. A PD-capable power adapter is required for this EVM.

Note

The E2 Revision of the AM275x EVM board is identical to Revision A of the AM275x EVM board.

Note

The E1 revision of the EVM has a known issue surrounding BOOTMODE8 logic during power-up and reset. BOOTMODE8 has two buffers that can both drive during bootup and created unexpected states on BOOTMODE8. With BOOTMODE8 in an unexpected state, any bootmode that depends on BOOTMODE8 configuration are affected. For more details on bootmode configuration, see the Boot Mode Selection.

Veify that J22 is not connected during power-up and reset to have proper BOOTMODE8 values.

All other bootmode signals and configurations are unaffected.

Note

External power supply or power accessory requirements:

- Nominal output voltage: 5VDC
- Max output current: 3000mA
- Efficiency Level V

Note

TI recommends using an external power supply or accessory that complies with applicable regional safety standards such as (by example) UL, CSA, VDE, CCC, PSE.

1.3 Kit Contents

The AM275x Evaluation module kit contains the following items:

- AM275x Evaluation module board
- Type-A to Micro-B USB cable (1 meter length)
- USB Type-C 5V/3A AC/DC cable

Note

The maximum length of the IO cables shall not exceed 3 meters.

Not included:

- Standoffs
- USB Power delivery enabled power supply

1.4 Device Information

The AM275x family of highly-integrated, high-performance microcontrollers is based on the Arm® Cortex™ R5F and C7x floating point DSP cores. The microcontrollers enable original equipment manufacturers (OEM) and original design manufacturers (ODM) to quickly bring to market devices with robust software support and rich user interfaces. The device offers the maximum flexibility of a fully integrated, mixed processor design.

The AM275x features extensive audio interfacing with 5x McASP peripherals. Peripherals supporting system level connectivity are included, such as 2-port Gigabit Ethernet, USB, OSPI/QSPI, CAN-FD, UARTs, SPI and GPIOs. The AM275x supports the latest cybersecurity requirements with the built-in Hardware Security Module (HSM). The dual-core R5Fs are arranged in one or two cluster subsystems with 128KB TCM per cluster (64KB per core) and up to two C7x DSP cores with 2.25MB of L2 SRAM per C7x DSP, greatly reducing the need for external memory.

1.4.1 Security

The AM275x EVM features a High Security, Field Securable (HS-FS) device. An HS-FS device has the ability to use a one time programming to convert the device from HS-FS to High Security, Security Enforced (HS-SE).

The AM275x device leaves the TI factory in an HS-FS state where customer keys are not programmed and has the following attributes:

- Does not enforce the secure boot process
- R5 and C7 JTAG ports are open
- Security Subsystem firewalls are closed
- SoC Firewalls are open
- ROM Boot expects a TI signed binary (encryption is optional)
- TIFS-MCU binary is signed by the TI private key

The One Time Programmable (OTP) keywriter converts the secure device from HS-FS to HS-SE. The OTP keywriter programs customer keys into the device eFuses to enforce secure boot and establish a root of trust. The secure boot requires an image to be encrypted, which is optional, and signed using customer keys, which is verified by the SoC. A secure device in the HS-SE state has the following attributes:

- C7, R5 JTAG ports are both closed
- Security subsystems and SoC firewalls are both closed
- TIFS-MCU and SBL need to be signed with active customer key

1.5 Audio Expansion Connectors

The AM275x EVM features two symmetric shielded 80-pin Audio Expansion Connectors (AEC1 & AEC2) for external Audio device interfacing. AEC1 and AEC2 are placed at fixed distances and specific locations on the left and right side of the AM275x EVM.

The AEC Pinout includes:

- Interspersed Ground Pins to limit EMI
- Audio
  - 2x McASP instances
    - 8 Serializers for both instances
    - transmit and receive bit clock/frame sync for both instances
  - Reference clock input/output to/from the daughter card
  - 2x eCAP inputs
- General Connectivity
  - SPI, I2C, MCAN, UART
- Power
  - 5V, I/O VDD
- 3x PWM Channels
- Up to 47 GPIOs
- 10x Reserved pins for futureproofing

For more information on Audio expansion connectors refer to the AEC Mapping chapter.

2 Hardware

2.1 Component Identification

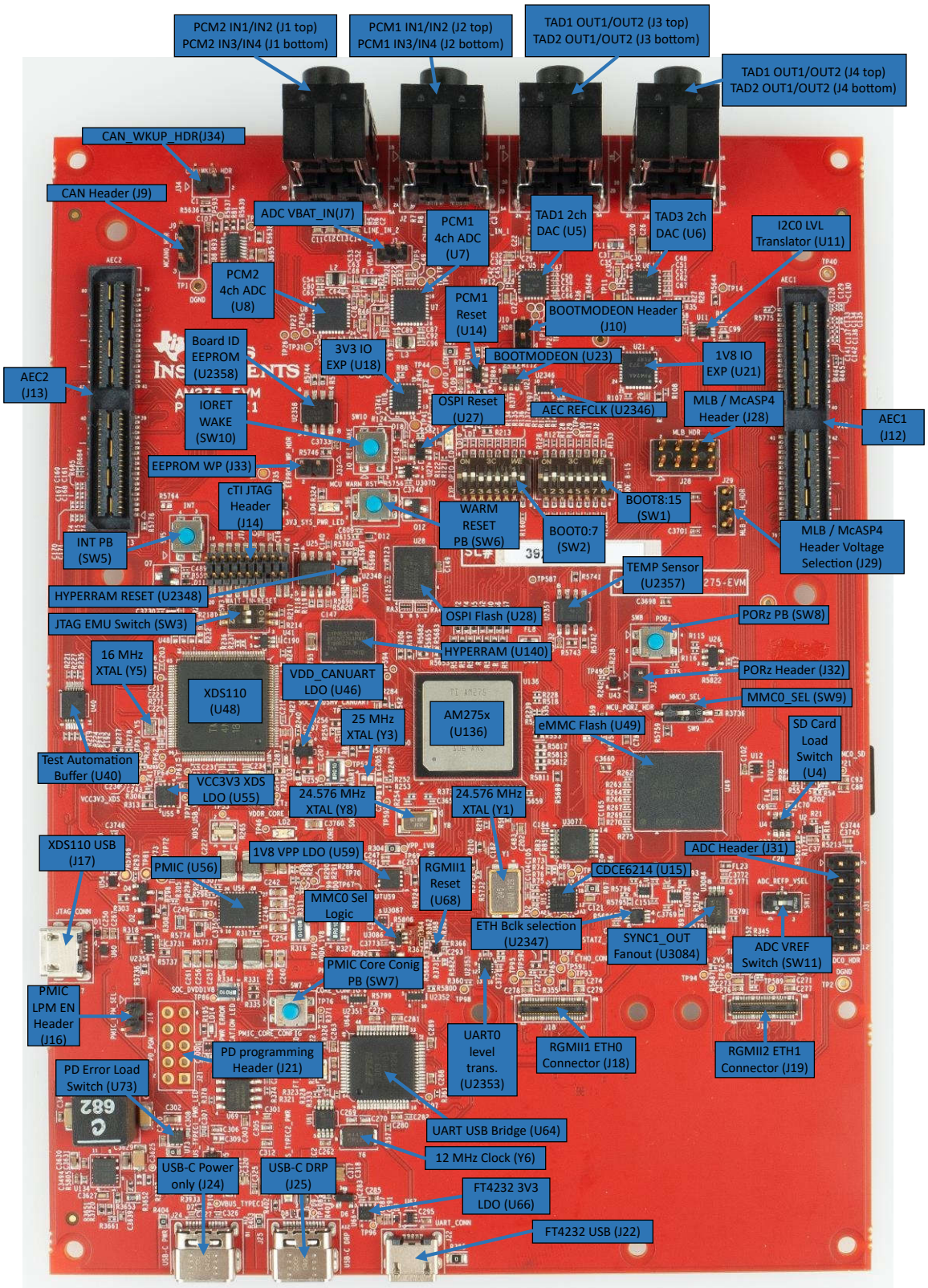


Figure 2-1. Top Component Identification

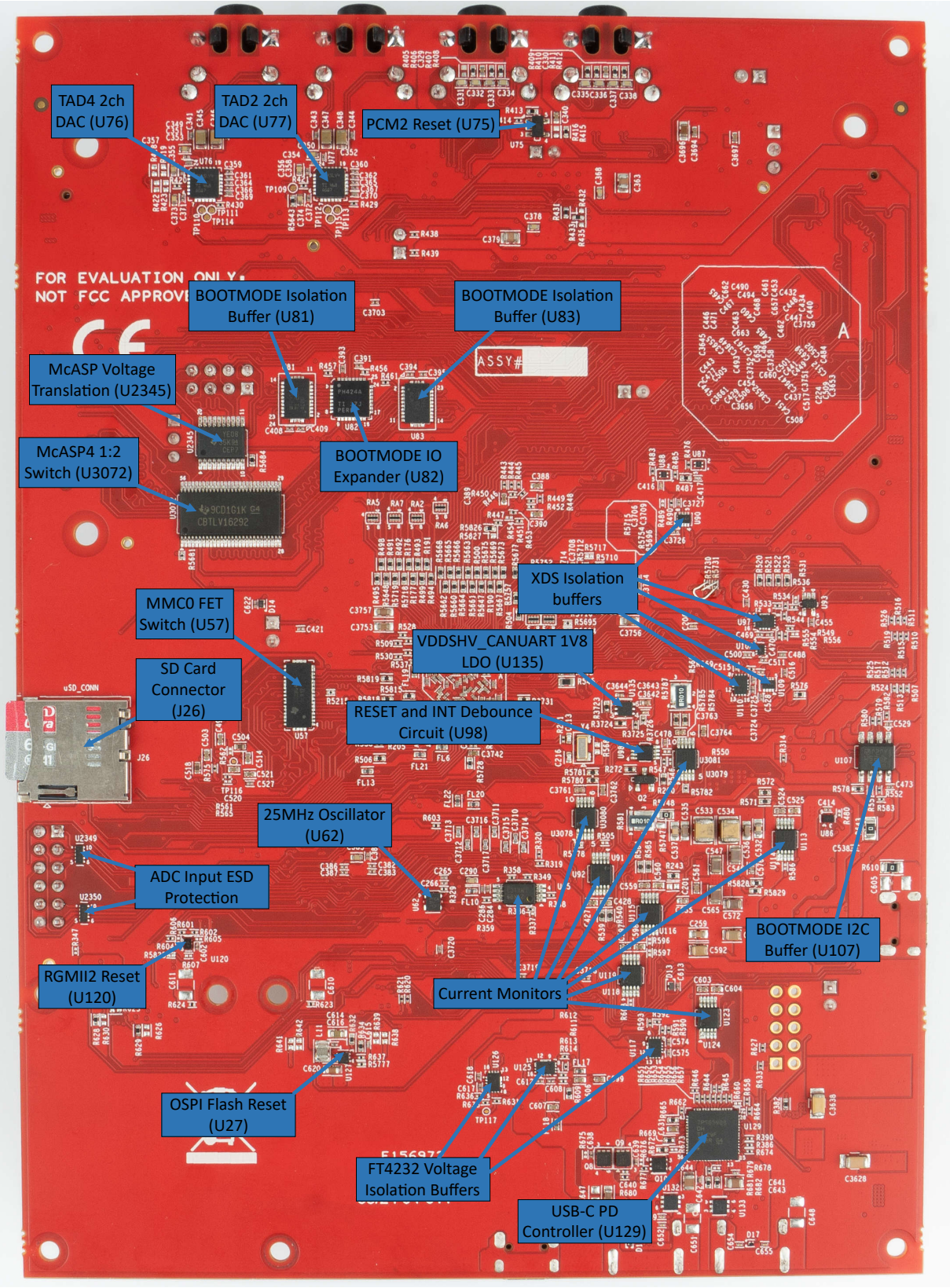


Figure 2-2. Bottom Component ID

2.2 Power Requirements

The AM275x EVM is powered from either of two USB Type-C inputs. The following sections describe the power distribution network topology that supply the AM275x EVM, supporting components, and the reference voltages.

Power supply designs that are compatible with the AM275x EVM:

- Power delivery enabled power adapter with USB-C® receptacle
- Power delivery enabled power adapter with captive USB-C cable
- PC USB Type-C port that has power delivery classification
  - Thunderbolt
  - Battery behind USB logo

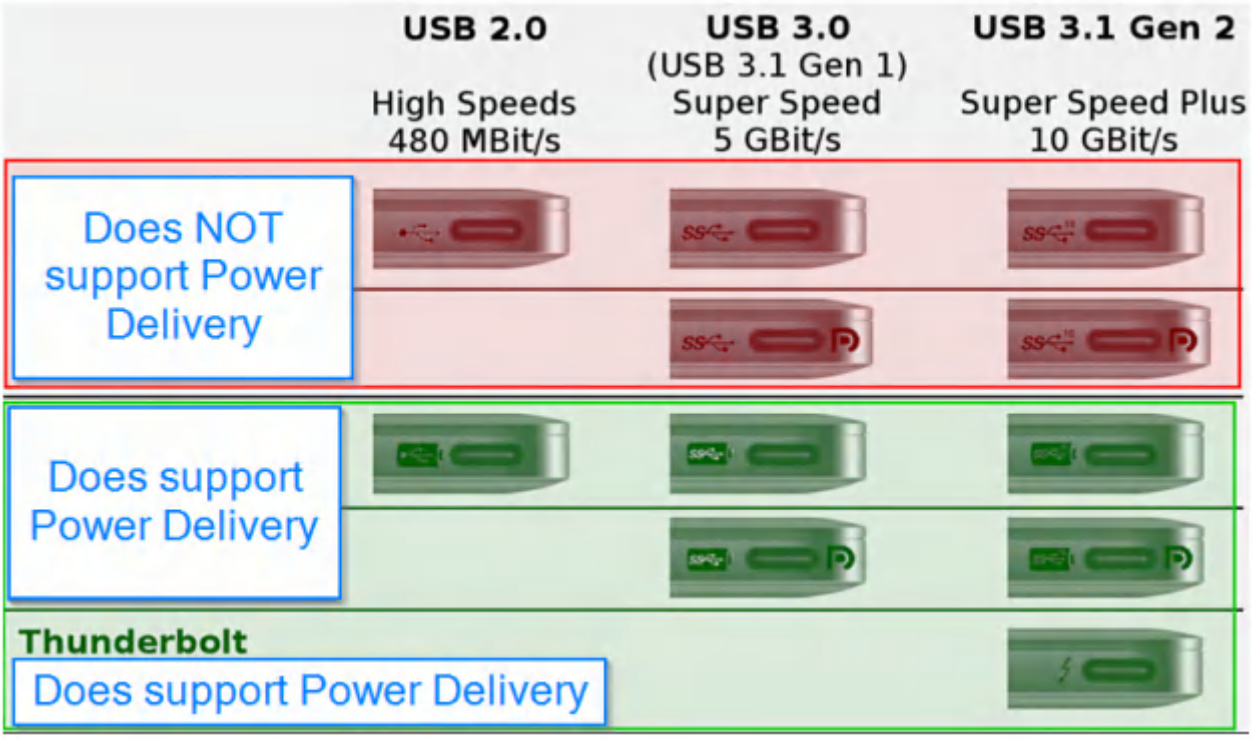


Figure 2-3. USB Type_C Power Delivery Classification

Power supply designs that are NOT compatible with the AM275x EVM:

- Any USB adapter cables such as:
  - Type-A to Type-C
  - micro-B to Type-C
  - DC barrel jack to Type-
- 5V, 1.5A power adapter with USB-C captive cable or receptacle
- PC USB Type-C port not capable of 3A

2.2.1 Power Input Using USB Type-C Connector

The AM275x is powered through either of the two USB Type-C connections. The USB Type-C source is capable of providing power delivery of more than 15W (3A at 5V). On this EVM, the channel configuration pins, CC1 and CC2, from either of the two the USB Type-C connector are interfaced to the Type C DUAL Power Delivery (PD) Controller (TPS65988DHRSHR). The PD controller monitors the USBC_CONNx_CC1 and USBC_CONNx_CC2 pins of either of both USB-C connectors to detect port attach/detach, attached device type (source, sink, or dual role power), cable orientation, and cable capacity. When a power source device is connected, the PD controller detects the device and identifies its role (source, sink, or dual role power). The PD controller then uses the PD protocol over the USBC_CONNx_CC1 and USBC_CONNx_CC2 pins to negotiate power requirements with the power source.

The minimum power requirement of the AM275x EVM is 15W (5V at 3A). When the power negotiation is unsuccessful and the source is not capable of providing the required power, then the output at the OR gate remains low which means the VMAIN Load switch (TPS22810DRVT) is disabled. Therefore, if the power requirement is not met, all power supplies remain in the off state. The board gets powered on completely only when the source can provide a minimum of 15W (5V at 3A).

The AM275x EVM includes a power supply based on a Burton (TPS6522430) Power Management Integrated Chip (PMIC) for each of the power rails. During the initial stage of the power supply, A minimum 5V supplied by the Type-C USB connector is used to generate all of the necessary voltages required by the PMIC and subsequently the rest of the board via the PMIC LDO outputs. For more information about the PMIC, refer to Section 2.2.5.

2.2.2 Power Status LEDs

Multiple power-indication LEDs are provided onboard to indicate to users the output status of major supplies. The LEDs indicate power across various domains as shown in Table 2-1.

Table 2-1. Power Status LEDs

Name	Default Status	Operation	Function
LD1	OFF	SoC_GPIO1_49	User Test LED
LD2	ON	VDDR_CORE	Power indicator for VDDR CORE
LD3	OFF	XDS Data	Red LED glows during XDS110 data transaction
LD4	ON	PMIC_RSTOUT	Power Good indicator for PMIC
LD5	ON 1	XDS Power	XDS Power Green LED
LD6	ON	VCC_3V3_SYS	Power indicator LED for VCC_3V3_SYS
LD7	ON 1	VCC_3V3_FT4232	FT4232 Power LED
LD9	OFF	VBUS_TYPEC2	Indicator LED for Type_C USB connector 2
LD10	OFF	IO_EXP_TEST_LED	User Test LED for 3V3 IO expander
LD13	OFF	VBUS_TYPEC2	Indicator LED for Type_C USB connector 2
LD14	OFF	VMAIN_EN	Power Delivery Error Indicator, Type-C connection not supplying minimum 15W (5V at 3A)

1. ON as long as micro-USB cable is connected.

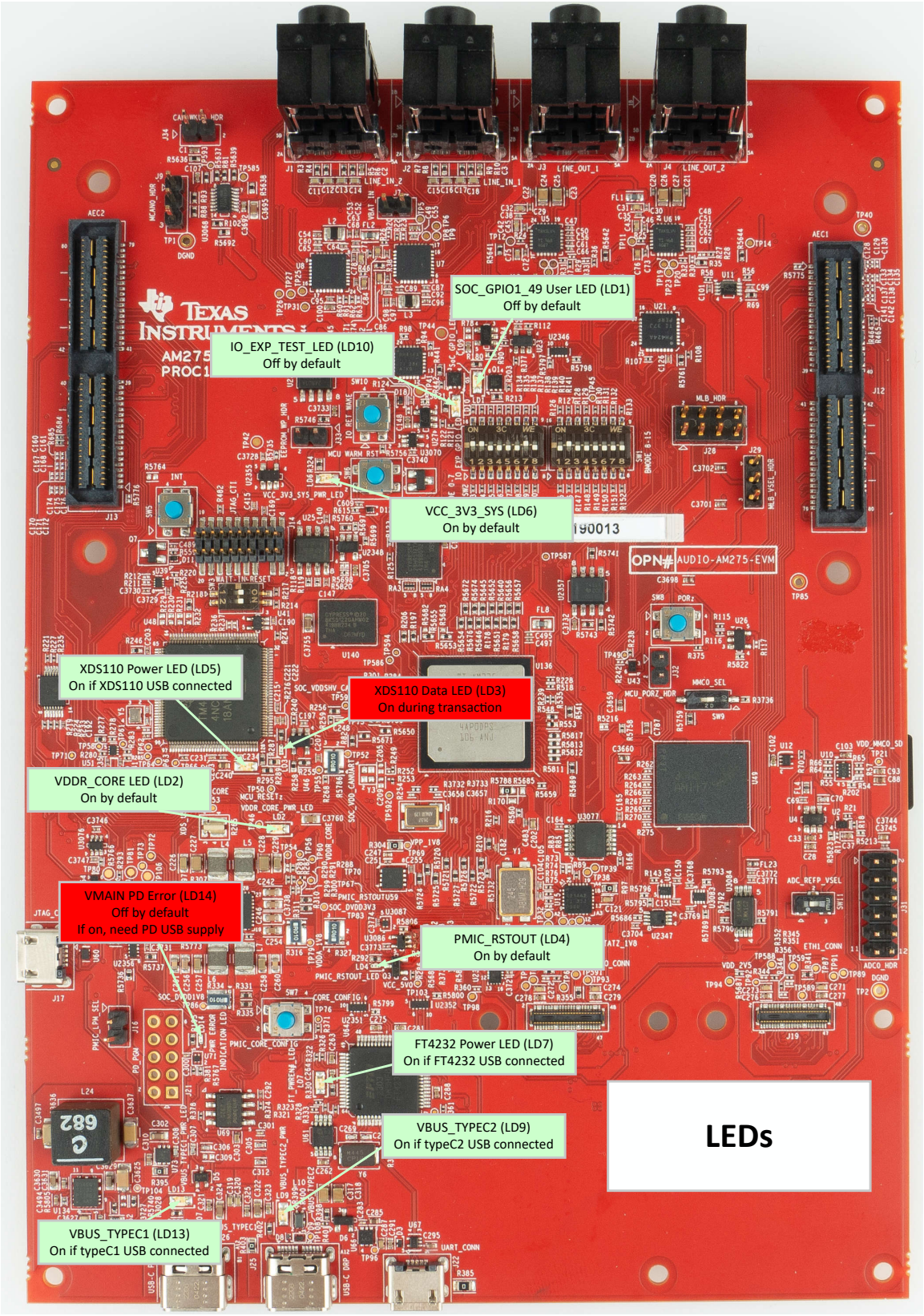
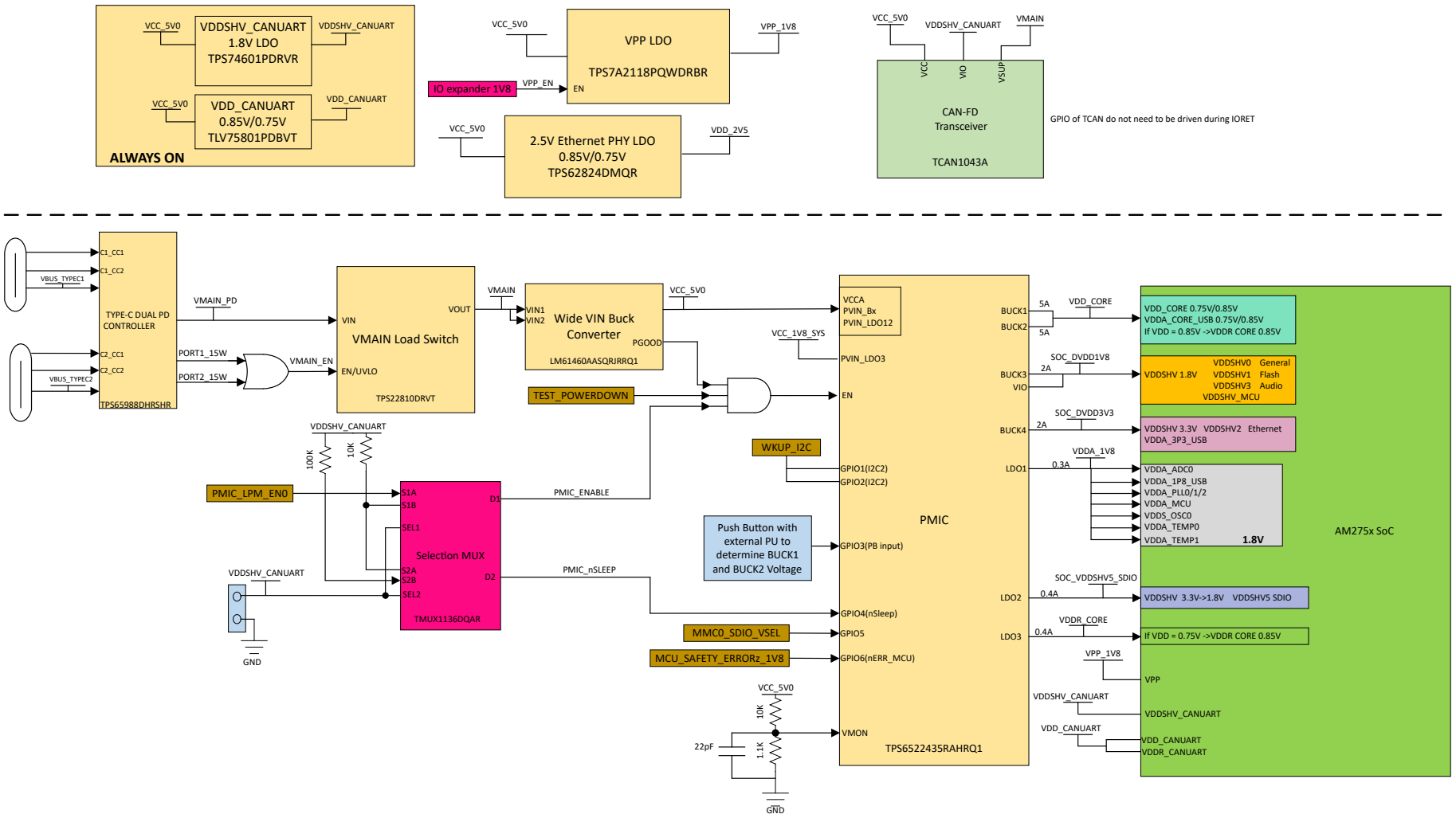


Figure 2-4. Power Status LEDs

2.2.3 Power Tree



2.2.4 Power Sequence

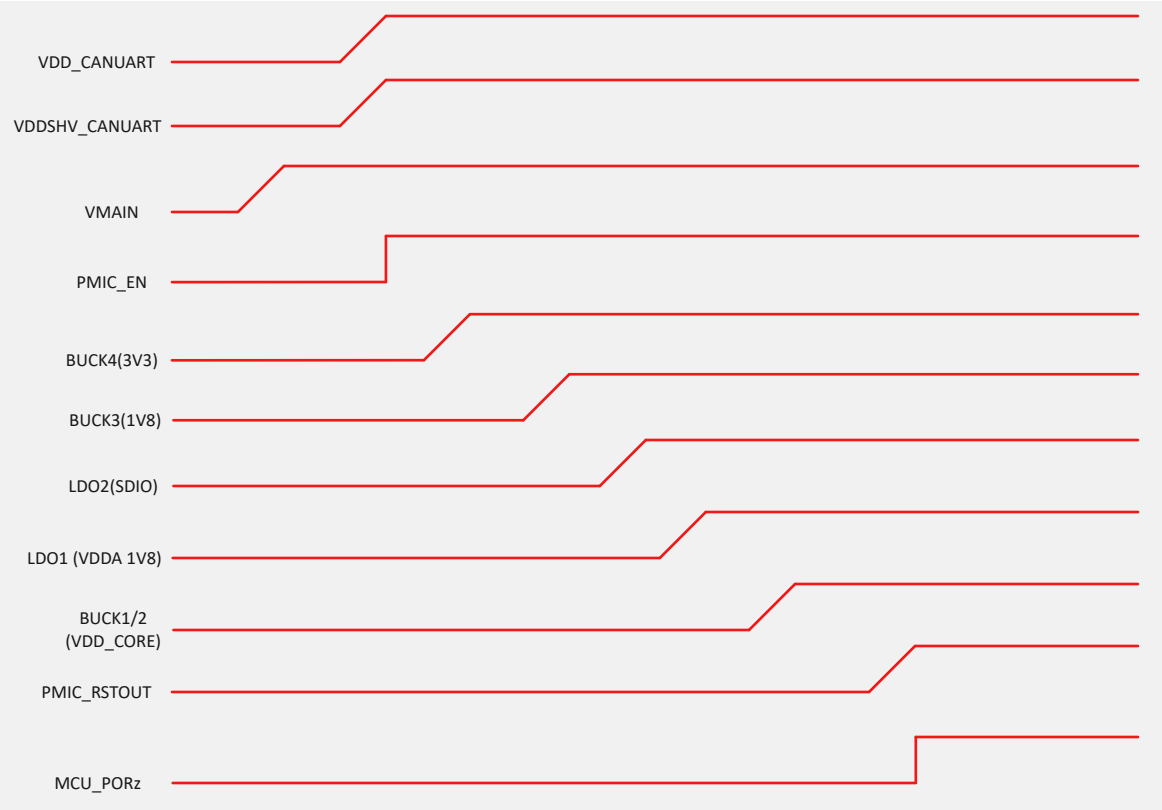


Figure 2-6. Power Sequence Diagram

Note

LDO3 is intentionally not included in this diagram because this configuration is for a 0.85V VDD Core which is shared with VDDR Core. LDO3 is OFF by default unless BUCK1/2 are configured for 0.75V.

2.2.5 PMIC

The AM275x EVM makes use of a Burton multirail power management IC (PMIC) (TPS6522435RAHRQ1). The PMIC integrates multiple supply rails to power the MCU, and other on-board peripherals.

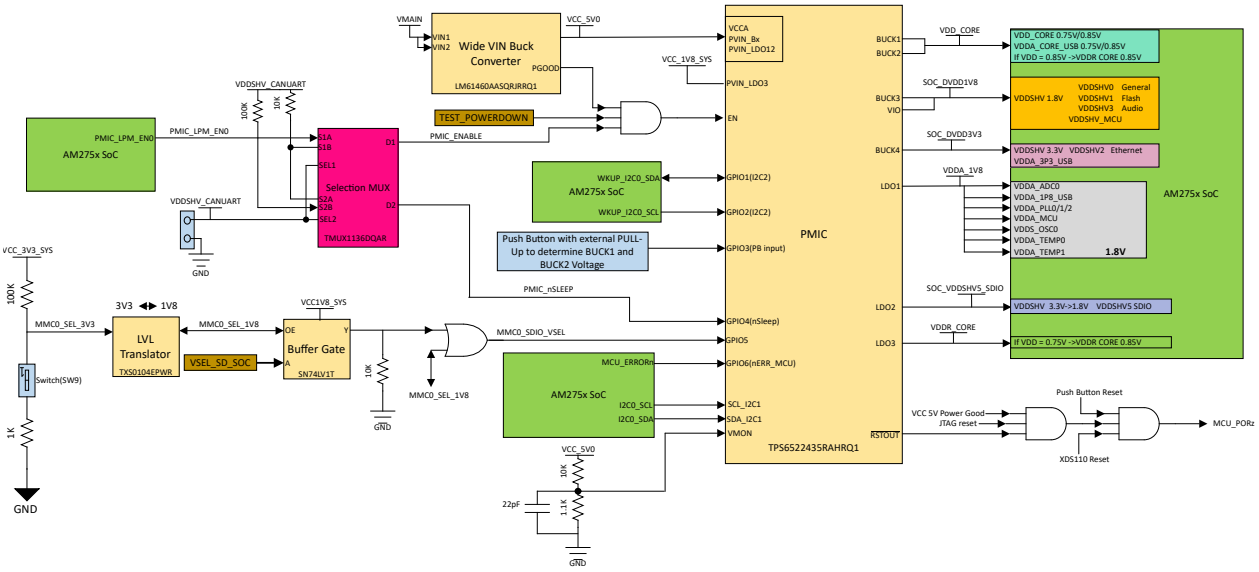


Figure 2-7. PMIC

An independent voltage monitoring unit inside the PMIC monitors undervoltage and overvoltage on all internal supply rails and regulator outputs of the power delivery supply. All supplies are protected with current limiting and overtemperature warning and shutdown.

The PMIC features multiple GPIO pins which serve as boot pins and various interfaces post-boot.

Table 2-2 shows the functions, boot configuration and default states of the GPIOs:

Table 2-2. PMIC GPIOs

GPIOx	Function	Boot Configuration
GPIO1	I2C SDA Wake-up	N/A
GPIO2	I2C SCL Wake-up	N/A
GPIO3	Push Button for Buck1/2 voltage	Populated External pull-up to 1.8V: VDD_CORE = 0.85V (DEFAULT)
		Non-populated External pull-up to 1.8V: VDD_CORE= 0.75V
GPIO4	PMIC Sleep signal (nSLEEP)	N/A
GPIO5	SD card or eMMC I/O voltage select	Digital high: 1.8V LDO2 output (SW9 OFF)
		Digital Low: 3.3V LDO2 output (SW9 ON)
GPIO6	Watchdog timeout Enable/Disable	Populated External pull-up to 1.8V: Watchdog Timer disabled (DEFAULT)
		Non-populated External pull-up to 1.8V: Watchdog timeout enabled

2.3 Reset

Figure 2-8 shows the reset architecture of the AM275x EVM.

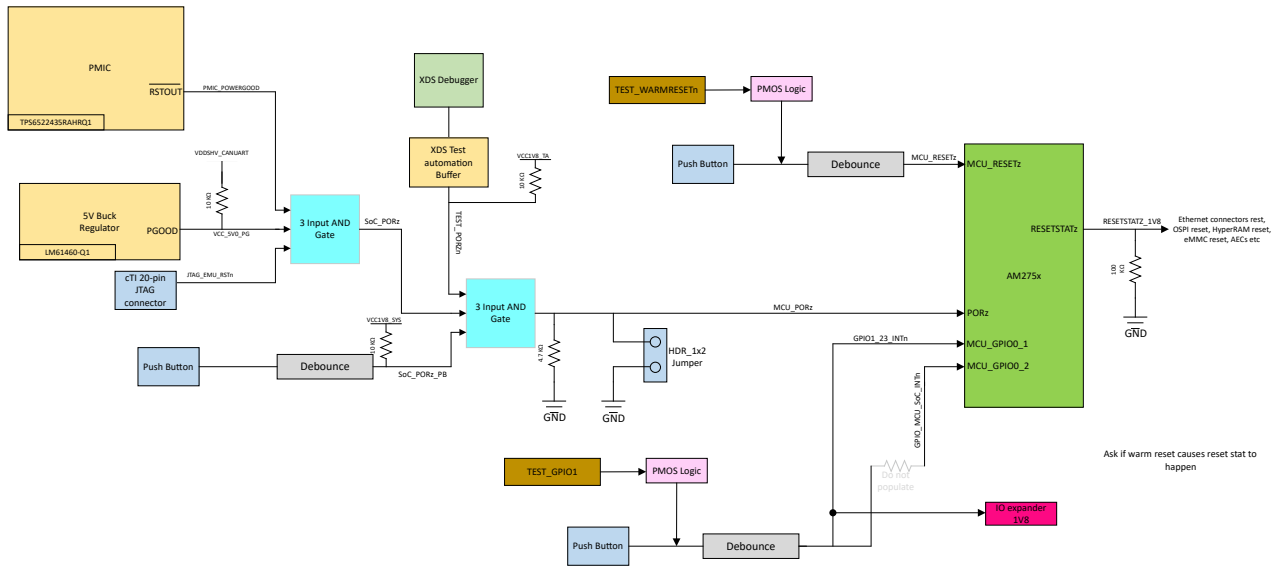


Figure 2-8. Reset Architecture Diagram

The AM275x SoC has the following resets:

- MCU_PORz is the Power-On-Reset for the AM275 SoC.
- MCU_RESETz is the Warm Reset to AM275 SoC.
- RESETSTATz_1V8 is the reset status output for the Main Domain.

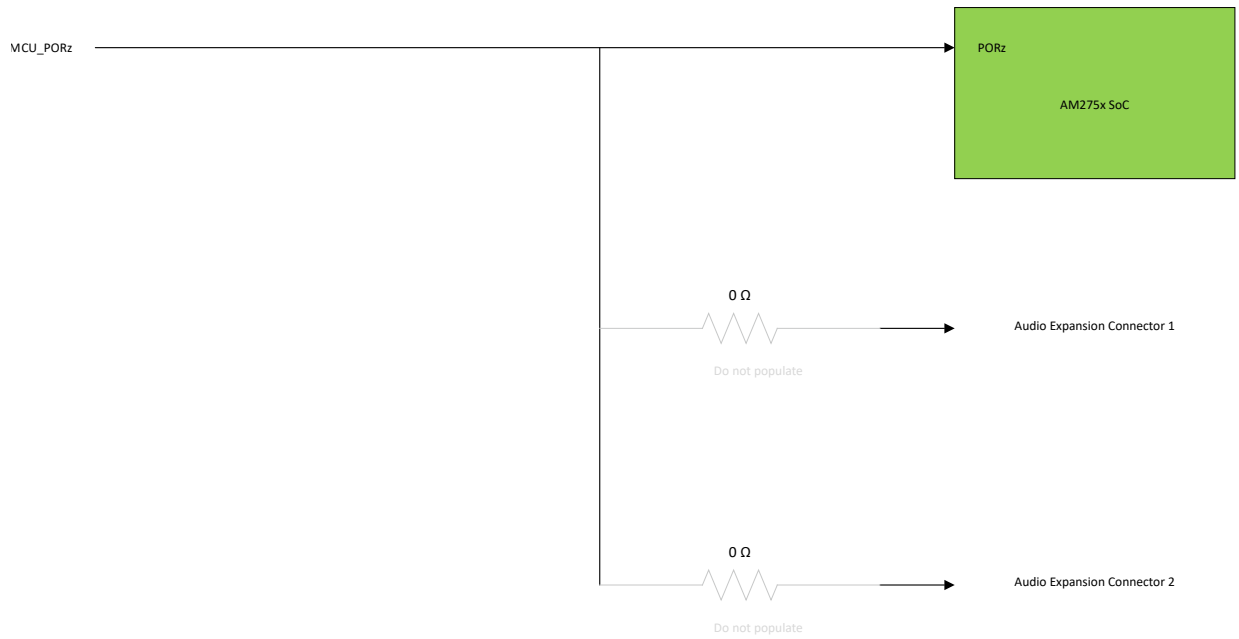


Figure 2-9. MCU_PORz Reset Signal Tree

The MCU_PORz signal is driven by a 3-input AND gates that generates a power on reset to the SoC when:

- The PMIC drives the PMIC PowerGood output signal low.
- The 5V buck regulator outputs a low signal for the power good signal.
- An external JTAG debugger drives the JTAG emulation reset signal low.
- The XDS Test Automation Header outputs a logic LOW signal (TEST_MCU_PORzn).
- The user push button (SW8) is pressed.

The MCU_PORz signal is tied to:

- AM275x SoC PORz input
- Audio Expansion Connectors (1 and 2)

MCU_PORz is also driven LOW by populating Jumper J32, thus shorting MCU_PORz to ground.

The MCU_RESETz signal creates a warm reset to the SoC when:

- The user push button (SW6) is pressed.
- The Test Automation Header outputs a logic LOW signal (TEST_WARMRESETn) to a P-Channel MOSFET gate that causes V_GS of the PMOS to be less than zero and so the MCU_RESETz signal connects to the PMOS drain that is tied directly to ground.

The MCU_RESETz signal is tied to:

- AM275x SoC MCU_RESETz input

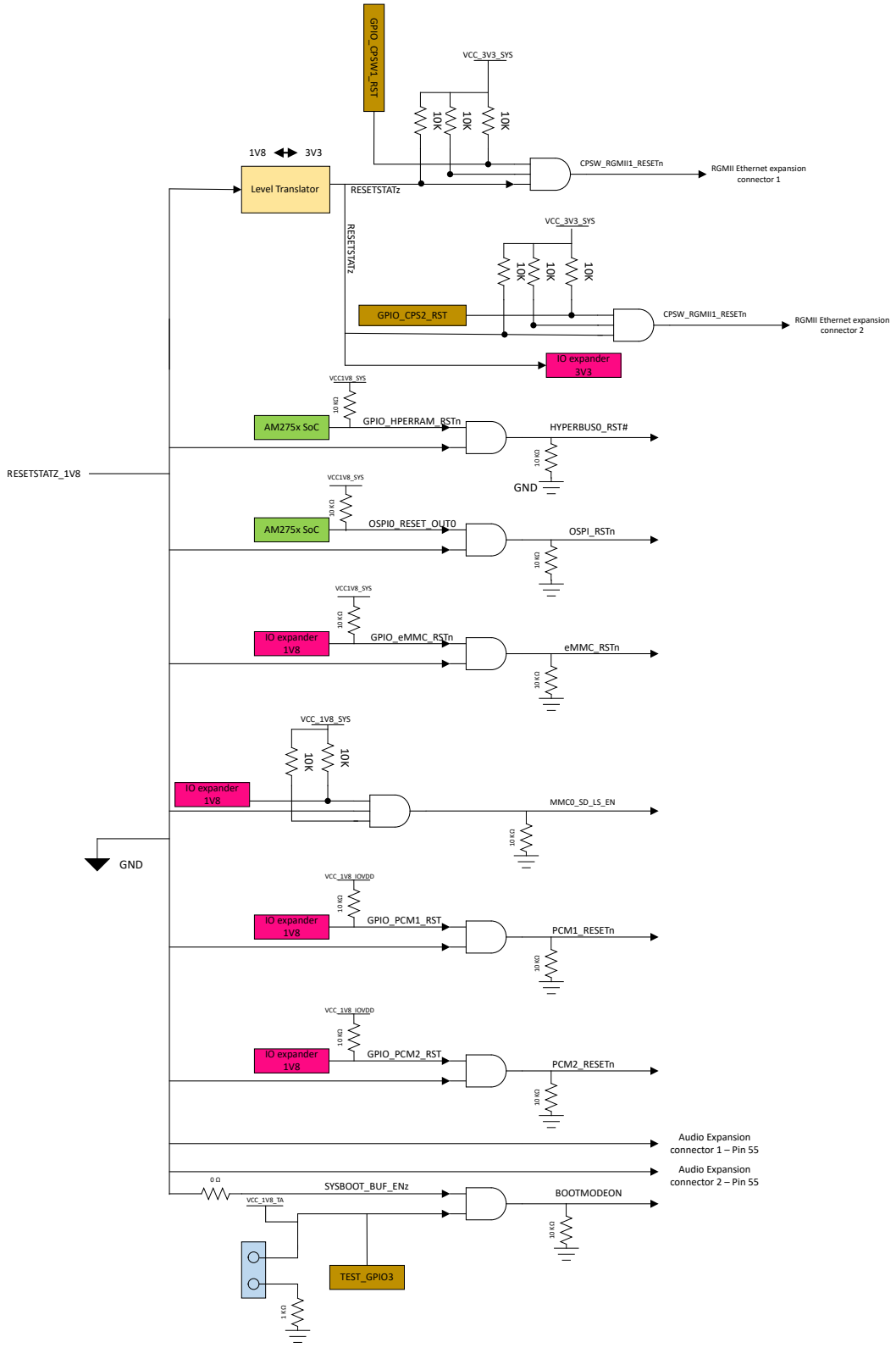


Figure 2-10. RESETSTATz Reset Signal Tree

The RESETSTATz_1V8 signal is the reset status signal for when a power-on reset or warm reset is triggered

The RESETSTATz_1V8 signal is tied to:

- Ethernet Expansion Connector reset (1 and 2)
- IO expander(U18) reset
- HYPERRAM reset
- OSPI reset
- eMMC reset
- MMC0 SD enable
- PCM reset (1 and 2)
- Audio Expansion Connector (1 and 2)
- BOOTMODE buffer output enable

The AM275x EVM has two dedicated external interrupts to the SoC:

1. GPIO1_23_INTn, that occurs when:
   - The user push button (SW5) is pressed.
   - The Test Automation Header outputs a logic LOW signal (TEST_GPIO1) to a P-Channel MOSFET gate that causes V_GS of the PMOS to be less than zero and so the GPIO1_23_INTn signal connects to the PMOS drain that is tied directly to ground.
2. PMIC generated Interrupt output is tied to either:
   - GPIO1_29 of the AM275x SoC
   - EXTINTn of the AM275x SoC
   - Both Ethernet Add-on connectors

2.4 Clock

The AM275x SoC requires a 25MHz clock input for MCU_OSC0. All reference clocks required for the SoC and the two Ethernet expansion connectors are generated from a single three output clock buffer (LMK1C1103PWR), which is sourced from a single 25MHz LVCMOS Oscillator (LMK6CE25000) by default.

The EVM also requires a 16MHz clock source for the TM4C129 microcontroller for UART-USB JTAG support, and another 16MHz clock source for the USB-to-UART bridge FTDI chip.

A 32.768KHz low frequency crystal is also available for Real Time Clock (RTC) applications.

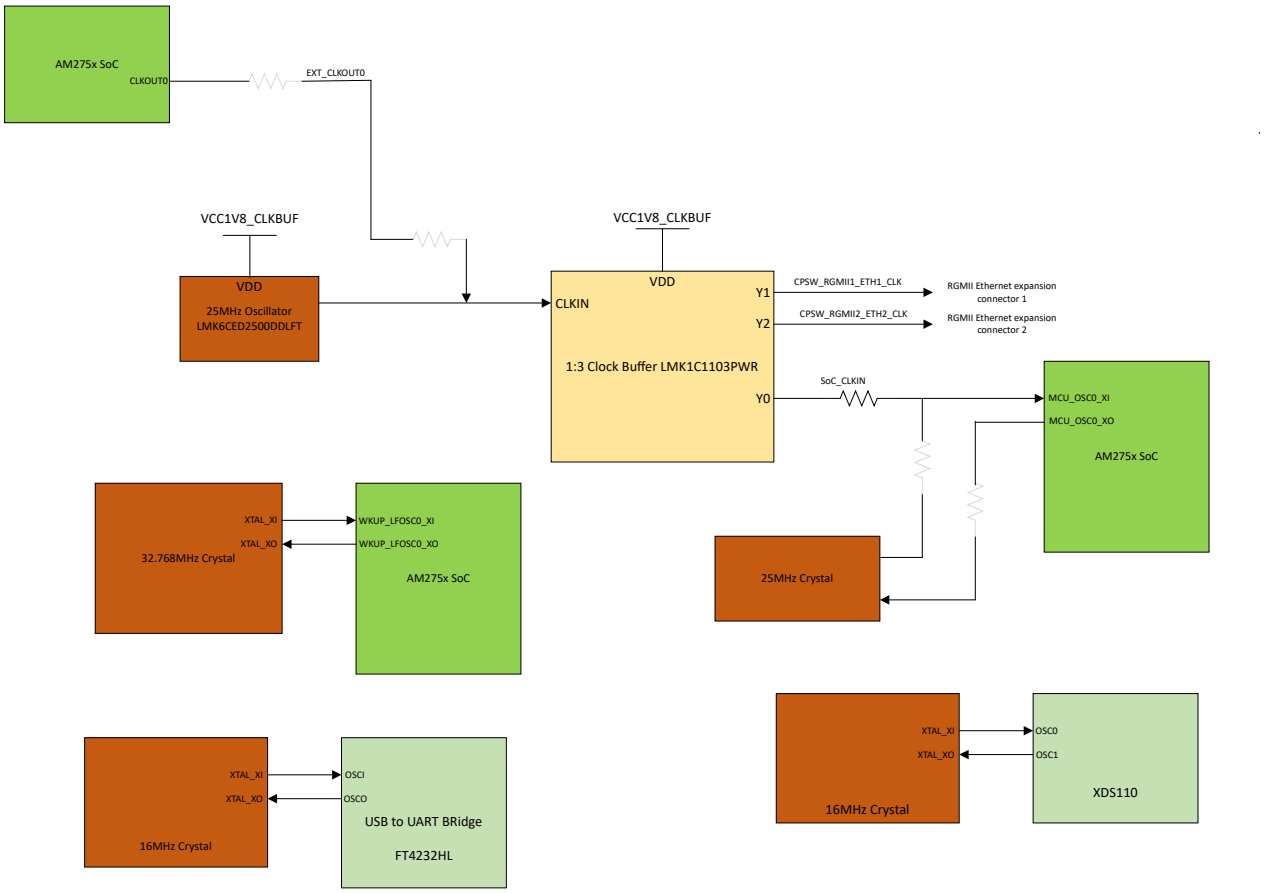


Figure 2-11. Oscillator Clock Tree

The SoC clock input can also be sourced from a single 25MHz crystal. To use the crystal there must be resistors mounted and unmounted. When the crystal is used as a clock source then the AM275x CLKOUT0 (P1) signal is used to source the three output clock buffer for the Ethernet expansion connector reference clock signals.

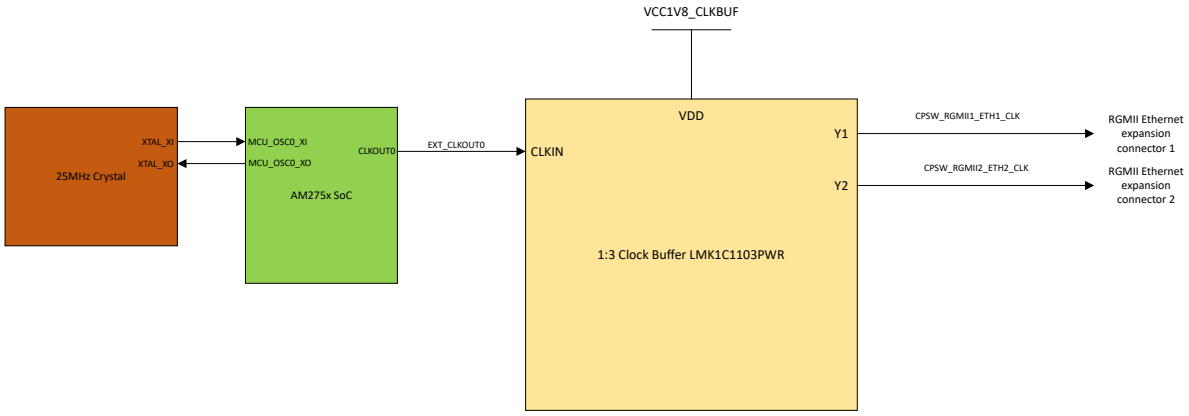


Figure 2-12. Crystal Clock Tree

Table 2-3 describes the proper resistors and capacitors to be mounted and DNI'd for each clock source configuration.

Table 2-3. Clock Source

Clock Source	Mounted	DNI
25MHz LVCMOS Oscillator (default)	R336, R249, R349	R337, R170, R252, R253,C205,C209
25MHz Crystal	R337, R170, R252, R253,C205,C209	R336, R249, R349

The AM275x EVM has three bi-directional Audio external reference clock signals used to provide audio reference clocks from external audio devices to the AM275x Multi Channel Audio Serial Ports (McASP), or from the internal audio clock sources such as McASP high-clocks or the Audio PLL to external audio devices:

- AUDIO_EXT_REFCLK2
- AUDIO_EXT_REFCLK1
- AUDIO_EXT_REFCLK0

AUDIO_EXT_REFCLK2 reference clock signal source is selected through a Multiplexer (TS5A3357QDCURQ1) from three inputs:

- CPSW_RGMII1_BCLK_1V8 signal, an Ethernet Audio Video Bridging (eAVB) bit clock signal from RGMII Ethernet connector 1 for Audio over Ethernet applications.
- CPSW_RGMII2_BCLK_1V8 signal, an eAVB bit clock signal from RGMII Ethernet connector 2 for Audio over Ethernet applications.
- CDCE_CLK_OUT1 signal, a clock output generated from a clock generator(CDCE6214RGET) that has a 24.576MHz crystal as a clock source.

The AVB bit clock signals from both RGMII Ethernet connectors (CPSW_RGMII1_BCLK) are both level translated by Level Translator (SN74AVC2T244DQMR), from 3.3V to 1.8V before being applied to the Multiplexer inputs.

AUDIO_EXT_REFCLK2_S0 and AUDIO_EXT_REFCLK2_S1 serve as Multiplexer input selection bits for selecting AUDIO_EXT_REFCLK2 clock input.

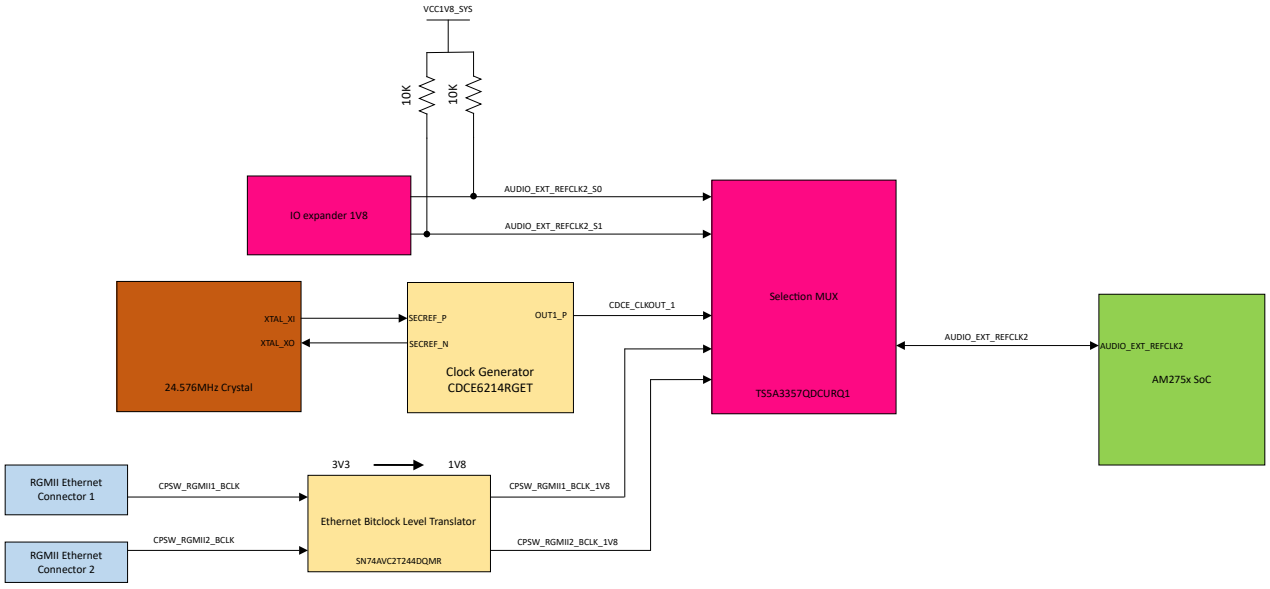


Figure 2-13. Audio_EXT_REFCLK2 Clock Tree

Table 2-4 shows the selection options for AUDIO_EXT_REFCLK2 reference clock source.

Table 2-4. AUDIO_EXT_REFCLK2 Selection Truth Table

AUDIO_EXT_REFCLK2_S0	AUDIO_EXT_REFCLK2_S1	AUDIO_EXT_REFCLK2
0	0	————
1	0	CPSW_RGMII2_BCLK_1V8
0	1	CPSW_RGMII1_BCLK_1V8
1	1	CDCE_CLK_OUT1(DEFAULT SELECTION)

AUDIO_EXT_REFCLK1 and AUDIO_EXT_REFCLK0 reference clock signals are selected through the same bi-directional Multiplexer (TMUX1136DQAR) from two options each:

AUDIO_EXT_REFCLK0 is selected from:

- AEC1_REFCLKOUT, a reference audio clock signal from Audio Expansion Connector 1. If AEC1_REFCLKOUT is selected (Default), it gets output to AUDIO_EXT_REFCLK0 signal.
- AEC1_REFCLKIN, a reference audio clock to Audio Expansion Connector 1. If AEC1_REFCLKIN is selected, it gets the reference audio clock signal AUDIO_EXT_REFCLK0, from the AM275x SoC.

AUDIO_EXT_REFCLK1 is selected from:

- AEC2_REFCLKOUT, a reference audio clock signal from Audio Expansion Connector 2. If AEC2_REFCLKOUT is selected, it gets output to AUDIO_EXT_REFCLK1 signal.
- AEC2_REFCLKIN, a reference audio clock to Audio Expansion Connector 2. If AEC2_REFCLKIN is selected, it gets the reference audio clock signal AUDIO_EXT_REFCLK1, from the AM275x SoC.

AEC1_REFCLK_SEL and AEC2_REFCLK_SEL serve as Multiplexer input selection bits to AUDIO_EXT_REFCLK0 and AUDIO_EXT_REFCLK1, respectively.

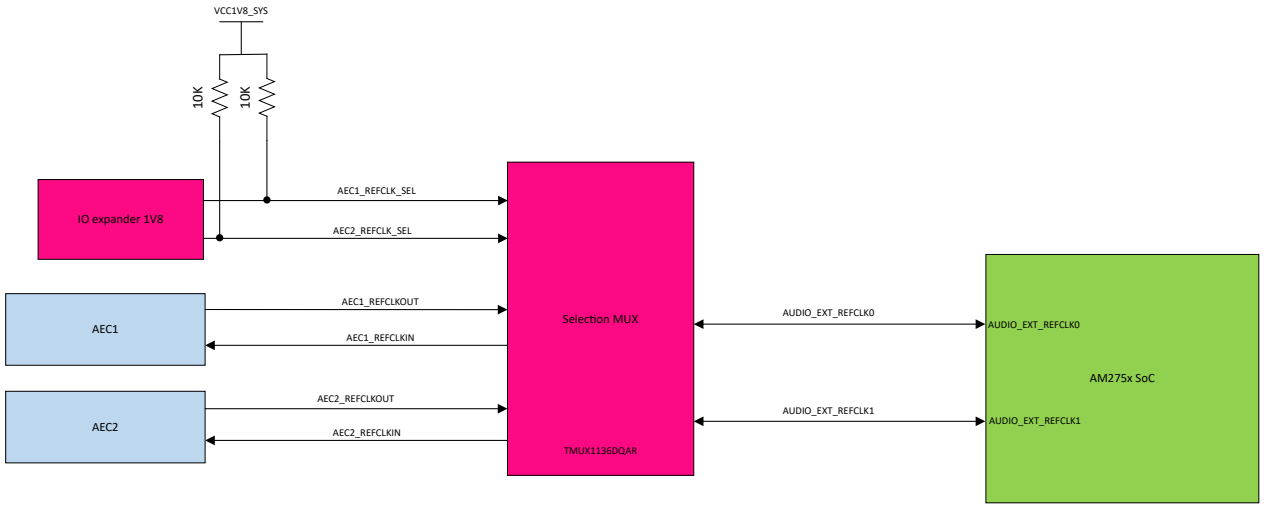


Figure 2-14. AUDIO_EXT_REFCLK0 and AUDIO_EXT_REFCLK1 Clock Tree

Table 2-5 shows the selection options for AUDIO_EXT_REFCLK0 and AUDIO_EXT_REFCLK1 reference clock signals:

Table 2-5. AUDIO_EXT_REFCLK0 and AUDIO_EXT_REFCLK1 Selection Truth Table

AECx_REFCLK_SEL	AUDIO_EXT_REFCLK0	AUDIO_EXT_REFCLK1
0	AEC1_REFCLKOUT	AEC2_REFCLKOUT
1(DEFAULT SELECTION)	AEC1_REFCLKIN	AEC2_REFCLKIN

A 24.576MHz crystal is also used to provide an Audio clock input OSC1 to the AM275x SoC for applications requiring specific audio frequencies.

2.5 Boot Mode Selection

The bootmode for the AM275x is selected by two DIP switches SW2(0:7) and SW1(8:15).

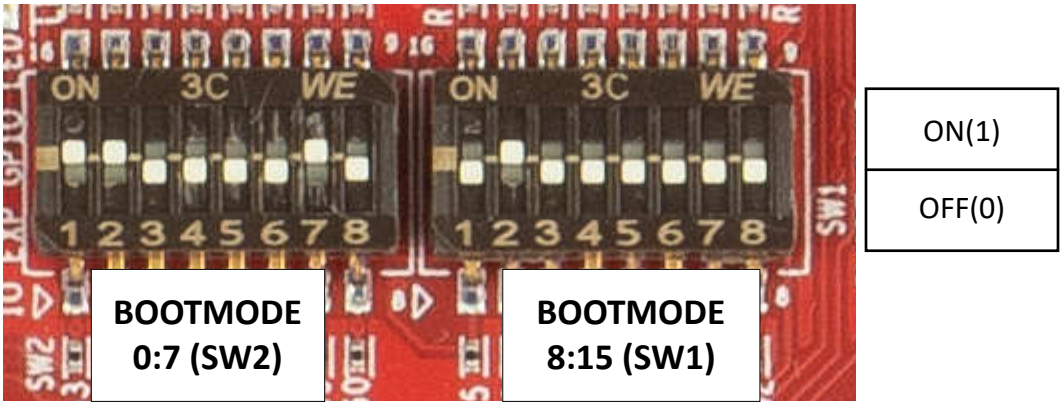


Figure 2-15. Boot Mode Switches SW2 and SW1 (MMC SD Card Boot)

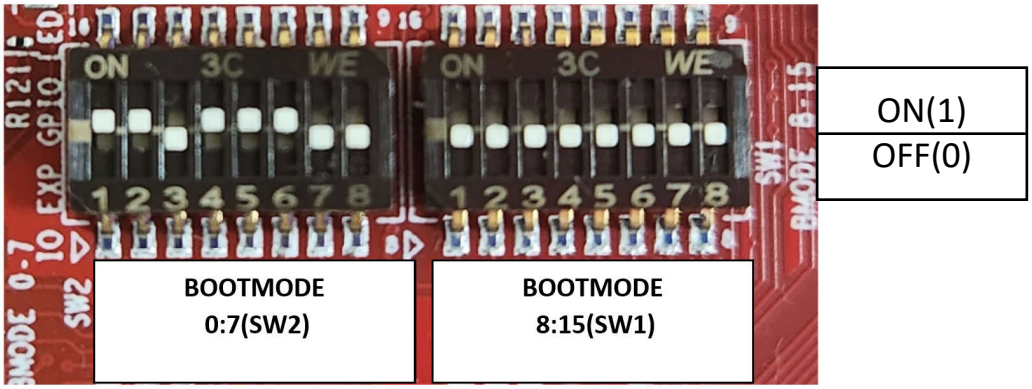


Figure 2-16. Boot Mode Switches SW2 and SW1 (UART Boot)

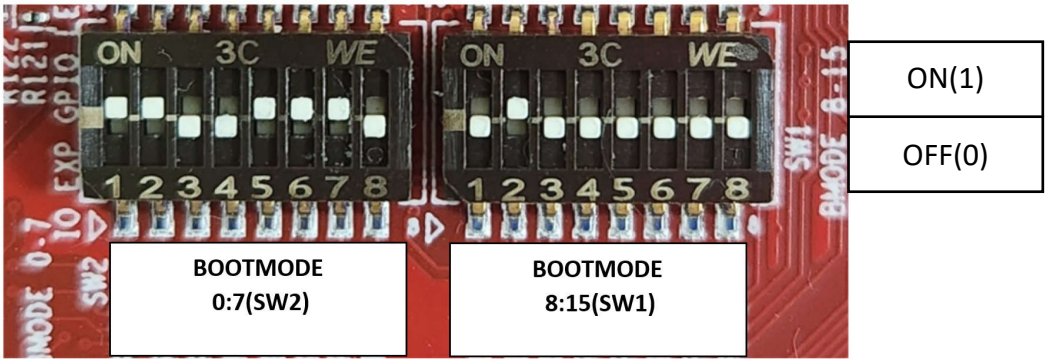


Figure 2-17. Boot Mode Switches SW2 and SW1 (OSPI Boot)

Table 2-6. PLL Reference Clock Selection BOOTMODE[2:0]

SW2.3	SW2.2	SW2.1	PLL REF CLK (MHz)
OFF	OFF	OFF	RVSD
OFF	OFF	ON	RSVD
OFF	ON	OFF	24MHz
OFF	ON	ON	25MHz
ON	OFF	OFF	26MHz
ON	OFF	ON	RSVD
ON	ON	OFF	RSVD
ON	ON	ON	RSVD

Table 2-7. Primary Boot Mode Selection[6:3]

SW2.7	SW2.6	SW2.5	SW2.4	Primary Boot Mode Selected
OFF	OFF	OFF	OFF	Serial NAND
OFF	OFF	OFF	ON	OSPI
OFF	OFF	ON	OFF	QSPI
OFF	OFF	ON	ON	SPI
OFF	ON	OFF	OFF	RGMII1
OFF	ON	OFF	ON	RMII1
OFF	ON	ON	OFF	I2C0
OFF	ON	ON	ON	UART0
ON	OFF	OFF	OFF	MMC/SD Card (SW9 ON)
ON	OFF	OFF	ON	eMMC (SW9 OFF)
ON	OFF	ON	OFF	USB
ON	OFF	ON	ON	RSVD
ON	ON	OFF	OFF	RSVD
ON	ON	OFF	ON	Fast-xSPI
ON	ON	ON	OFF	xSPI
ON	ON	ON	ON	No-boot/Dev boot

Table 2-8. Primary Boot Mode Configuration[9:7]

SW1.2		SW1.1		SW2.8		Primary Boot Mode
RVSD		Read Mode2	0: RSVD (Read mode is taken from Read Mode 1)	Read Mode1	0 : OSPI/ 1-1-8 Mode (valid only when Read Mode 2 is 0)	Serial NAND
			1: SPI/ 1-1-1 Mode (Read mode is taken from Read Mode 2 and Read Mode 1 is ignored)		1 : QSPI/ 1-1-4 Mode (valid only when Read Mode 2 is 0)	
RVSD		RSVD		Csel	0: Chip Select 0	OSPI
					1: Chip Select 1	
RVSD		RSVD		Csel	0: Chip Select 0	QSPI
					1: Chip Select 1	
RVSD		Mode	0: SPI Mode 0	Csel	0: Chip Select 0	SPI
			1: SPI Mode 3		1: Chip Select 1	
0		0		Link stat	0: Phy scan used for speed/duplex setup	RGMII1
					1: RGMII status register used for speed/ duplex setup	
CLKOUT	0: 50MHz clock not generated on CLKOUT0	CLK SRC	0: External clock source	0		RMII1
	1: 50MHz clock generated on CLKOUT0		1: Internal clock source			
Bus reset	0: Hung bus reset attempt after 1ms	RSVD		Addr	0: 0x50	I2C0
	1: No hung Bus reset attempted				1: 0x51	
RSVD		RSVD		RSVD		UART0
0		RSVD		Fs/Raw	0: FileSystem Mode	MMC/SD Card
					1: Raw Mode	
RSVD		RSVD		RSVD		eMMC
Core Volt	0: 0.85V Core Voltage	Mode	0: DFU(Device)	Lane Swap	0: No swapping of DP/DM	USB
	1: 0.75V Core Voltage		1: TBD		1: DP/DM is swapped	
RSVD		RSVD		RSVD		RSVD
RSVD		RSVD		RSVD		RSVD
RSVD		RSVD		RSVD		Fast-xSPI
SFDP	0: SFDP disabled	Read Cmd	0: 0x0B Read Command	Mode	0: 1S-1S-1S mode @ 50MHz	xSPI
	1: SFDP enabled		1: 0xEE Read Command		1:8D-8D-8D mode @ 25 MHz	
RSVD		ARM/ Thumb	0: ARM mode	No/Dev	0: Development Boot	No-boot/Dev boot
			1: Thumb mode		1: No Boot	

Table 2-9. Backup Bootmode Selection BOOTMODE[12:10]

SW1.5	SW1.4	SW1.3	Backup Boot Mode Selected
OFF	OFF	OFF	None
OFF	OFF	ON	USB
OFF	ON	OFF	RSVD
OFF	ON	ON	UART
ON	OFF	OFF	Ethernet
ON	OFF	ON	MMC/SD
ON	ON	OFF	SPI
ON	ON	ON	I2C

Table 2-10. Backup Bootmode Configuration BOOTMODE[13]

SW1.6		Backup Boot Mode	Defaulted Values for Back up Boot Mode
RSVD		None	
Mode	0: DFU (Device)	USB	Core Volt bit = 0 Lane Swap bit = 0
	1: TBD		
RSVD		RSVD	
RSVD		UART	
IF	0: RGMII with internal Delay	Ethernet	Link Stat bit = 0 (If RGMII)
	1: RGMII with external clock source		ClkOut bit= 0 and Clksrc bit = 1 (If RMII)
0		MMC	Mode bit = 0
RSVD		SPI	Csel bit = 0 Mode = 0
RSVD		I2C	Addr = 0 Bus Rest = 0

2.6 Header Information

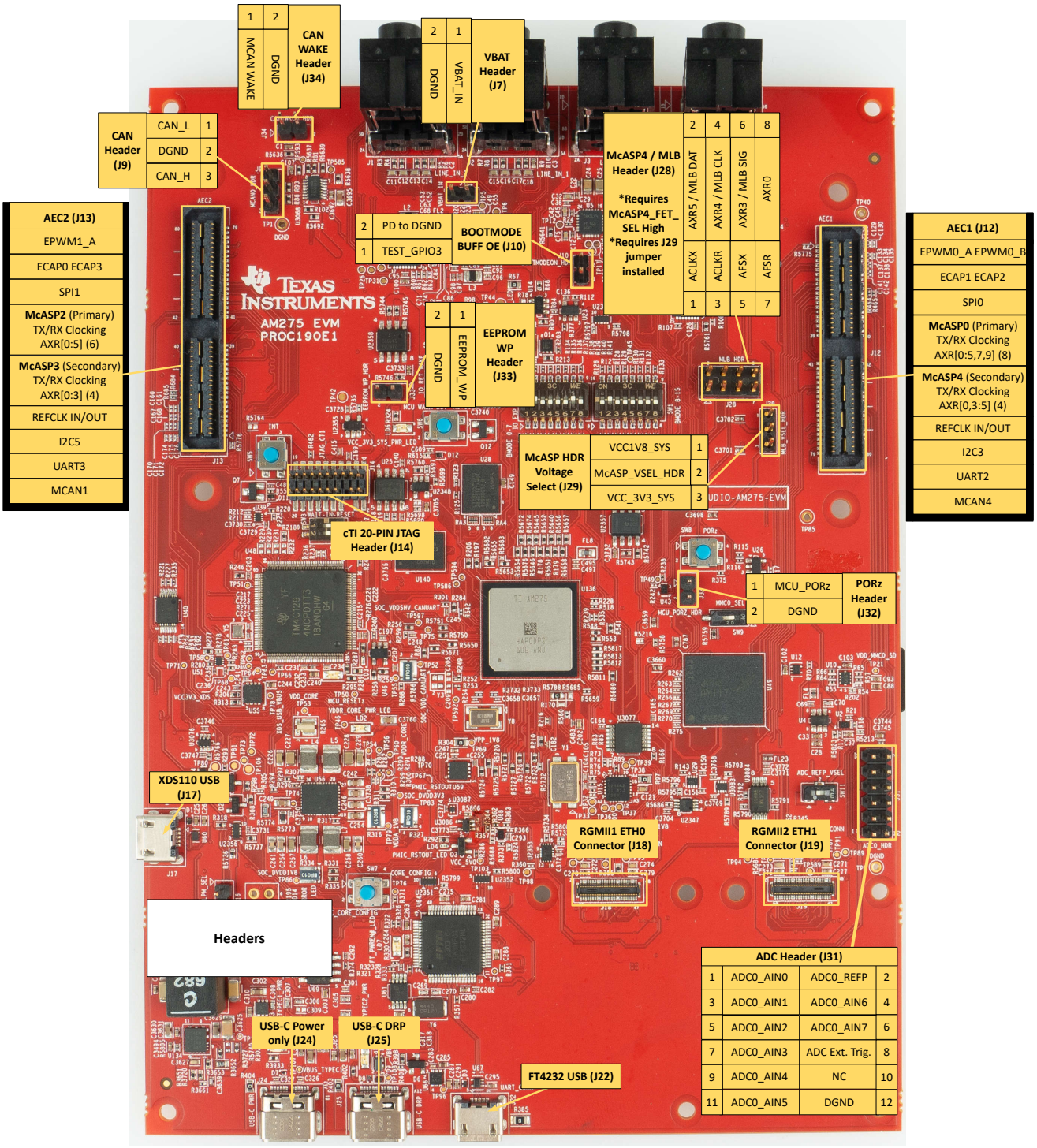


Figure 2-18. Headers

2.7 Push Buttons

The EVM supports multiple user push buttons that provide reset inputs to the processor.

EVM Push Buttons lists the push buttons for AM275x EVM.

Table 2-11. Push Buttons

Push Button	Signal	Function
SW8	PORz	SoC PORz Reset Input
SW6	RESETz	SoC Warm Reset input
SW5	INTn	User Interrupt Signal
SW10	IO RET WAKE PB	I/O retention wake input

2.8 Switches

SW9 dictates routing logic of MMC0 IO to eMMC or SDcard.

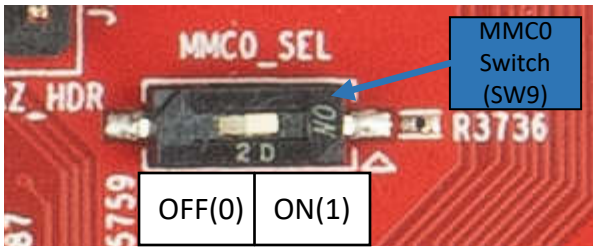


Figure 2-19. MMC0 Routing Switch

Table 2-12. SW9 Position Table

Switch Position	MMC0 Routing
ON	uSD Interface
OFF	eMMC Interface

SW11 dictates which reference 1.8V the AM275x ADC0 uses: VDDA_1V8 PMIC analog output, or an external 1.8V reference from Header J31(Pin 2).

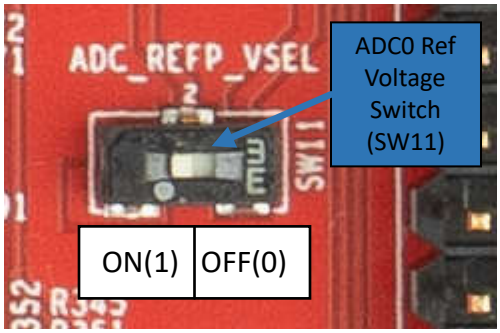


Figure 2-20. ADC0 Voltage Reference Switch

Table 2-13. SW11 Position Table

Switch Position	ADC Reference Source
SW11 Position 1-2	VDDA_1V8
SW11 Position 3-2	ADC0_REFP_HDR (External Reference from J31)

2.9 GPIO Mapping

Table 2-14. GPIO Mapping Table

Sl No.	GPIO Description	GPIO Net Name	Functionality	GPIO used	Package Signal Name	Direction With Respect to Control	Default State	Active State	Voltage Domain ON SoC SIDE	Voltage Rail Connected ON AM275x EVM
1	User_Test_LED_1	SOC_GPIO1_49	GPIO	GPIO1_38	MCASP1_AXR3	OUTPUT	LOW	HIGH	VDDSHV3	SoC_DVDD1V8
2	User_interrupt	GPIO_MCU_SoC_INTn	GPIO	MCU_GPIO0_2	MCU_GPIO0_2	INPUT	NA	NA	VDDSHV_MCU	SoC_DVDD1V8
3	PMIC SD/DDR voltage select, and EMMC/SD FET path select	VSEL_SD_SOC	VOLTAGE SELECTION	MCU_GPIO0_0	WKUP_TIMER_IO0	OUTPUT	NA	NA	VDDSHV_MCU	SoC_DVDD1V8
4	Push button IORET WAKE	IORET_WAKE	GPIO	MCU_GPIO0_16	MCU_GPIO0_16	INPUT	HIGH	LOW	VDDSHV_CANUART	SOC_VDDSHV_CANUART
5	AEC conn 1 GPIO_0	AEC1_GPIO0_0	GPIO	MCU_GPIO0_15	MCU_GPIO0_15	NA	NA	NA	VDDSHV_CANUART	
6	AEC conn 1 GPIO_1	AEC1_GPIO0_1	GPIO	GPIO0_12	OSPI0_CSn1	NA	NA	NA	VDDSHV1	SoC_DVDD1V8
7	For PMIC interrupt	MCU_INTn	Interrupt	GPIO1_29	I2C1_SDA	INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD1V8
8	User Interrupt IO Expander Interrupt	GPIO1_23_INTn	INTERRUPT	MCU_GPIO0_1	WKUP_TIMER_IO1	INPUT	HIGH	LOW	VDDSHV_MCU	SoC_DVDD1V8
9	AEC conn 2 GPIO_0	AEC2_GPIO0_0	GPIO	MCU_GPIO0_4	MCU_GPIO0_4	NA	NA	NA	VDDSHV_MCU	SoC_DVDD1V8
10	AEC conn 2 GPIO_1	AEC2_GPIO0_1	GPIO	MCU_GPIO0_3	MCU_GPIO0_3	NA	NA	NA	VDDSHV_MCU	SoC_DVDD1V8
IO EXPANDER-01										
1	RGMII2_RST	GPIO_CPSW2_RST	ENABLE	IO EXPANDER-P10		OUTPUT	HIGH	LOW		VCC_3V3_SYS
2	RGMII1_RST	GPIO_CPSW1_RST	ENABLE	IO EXPANDER-P11		OUTPUT	HIGH	LOW		VCC_3V3_SYS
3	MMC0 FET selection	MMC0_FET_EN	Peripheral selection	IO EXPANDER-P02		OUTPUT	HIGH	LOW		VCC_3V3_SYS
4	McASP4 FET selection	McASP4_FET_SEL	Peripheral selection	IO EXPANDER-P03		OUTPUT	LOW	HIGH		VCC_3V3_SYS
5	Power Delivery I2C Interrupt Request	PD_I2C_IRQ	ENABLE	IO EXPANDER-P05		INPUT	HIGH	LOW		VCC_3V3_SYS
6	User Test LED 2	IO_EXP_TEST_LED	GPIO	IO EXPANDER-P12		OUTPUT	LOW	HIGH		VCC_3V3_SYS
IO EXPANDER-02										
1	PCM1 RESET	GPIO_PCM1_RST	ENABLE	IO EXPANDER-P20		OUTPUT	HIGH	LOW		VCC1V8_SYS
2	PCM2 RESET	GPIO_PCM2_RST	ENABLE	IO EXPANDER-P22		OUTPUT	HIGH	LOW		VCC1V8_SYS
3	Test GPIO from the XDS IC	TEST_GPIO2	GPIO	IO EXPANDER-P21		NA	HIGH	NA		VCC1V8_TA
4	Audio ext refclk2 selection	AUDIO_EXT_REFCLK2_S0	Clock selection	IO EXPANDER-P24		OUTPUT	HIGH	LOW		VCC1V8_SYS
5	Audio ext refclk2 selection	AUDIO_EXT_REFCLK2_S1	Clock selection	IO EXPANDER-P25		OUTPUT	HIGH	LOW		VCC1V8_SYS
6	AEC 1 and 2 connector refclk selection	AEC1_REFCLK_SEL	Clock selection	IO EXPANDER-P26		OUTPUT	HIGH	LOW		VCC1V8_SYS
7	AEC 1 and 2 connector refclk selection	AEC2_REFCLK_SEL	Clock selection	IO EXPANDER-P27		OUTPUT	HIGH	LOW		VCC1V8_SYS
8	eMMC flash reset	GPIO_eMMC_RSTn	ENABLE	IO EXPANDER-P10		OUTPUT	HIGH	LOW		VCC1V8_SYS
9	TCAN1043A enable	IO_MCAN0_EN	ENABLE	IO EXPANDER-P11		OUTPUT	HIGH	LOW		VDDSHV_CANUART

Table 2-14. GPIO Mapping Table (continued)

Sl No.	GPIO Description	GPIO Net Name	Functionality	GPIO used	Package Signal Name	Direction With Respect to Control	Default State	Active State	Voltage Domain ON SoC SIDE	Voltage Rail Connected ON AM275x EVM
10	TCAN1043A STB control	IO_MCAN0_STB#	MODE SELECTION	IO EXPANDER-P13		OUTPUT	HIGH	LOW		VDDSHV_CANUART
11	UART2 FET selection	UART2_FET_SEL	Peripheral selection	IO EXPANDER-P14		OUTPUT	LOW	HIGH		VCC1V8_SYS
12	UART3 FET selection	UART3_FET_SEL	Peripheral selection	IO EXPANDER-P15		OUTPUT	LOW	HIGH		VCC1V8_SYS
13	PCM6240_INT	PCM1_INT_1V8	INTERRUPT	IO EXPANDER-P16		INPUT	NA	HIGH		VCC1V8_SYS
14	PCM6240_INT	PCM2_INT_1V8	INTERRUPT	IO EXPANDER-P17		INPUT	NA	HIGH		VCC1V8_SYS
15	uSD interface voltage enable	MMC0_SD_EN	ENABLE	IO EXPANDER-P03		OUTPUT	HIGH	LOW		VCC1V8_SYS
16	VPP supply enable	VPP_EN	ENABLE	IO EXPANDER-P04		OUTPUT	LOW	HIGH		VCC1V8_SYS

2.10 Interfaces

2.10.1 Memory Interface

2.10.1.1 OSPI Interface

The AM275 EVM features a 512Mb OSPI memory device (S28HS512TGABHM010) that is connected to the OSPI0 interface of the AM275x SoC. The OSPI0 interface supports single and double data rates up to 166MHz SDR and 166MHz DDR (333MB/s).

The AM275 EVM provides 0-ohm resistors for OSPI_DQ[0:7], OSPI_DQS, OSPI_CLK, and OSPI_INTn signals. The OSPI Flash footprint allows for the installation of either a QSPI Flash or an OSPI Flash. The 0-ohm series resistors provided for signals OSPI_DQ[4:7] can be removed if a QSPI flash is to be mounted. External pull up resistors are provided on OSPI_DQ[0:7] to prevent bus floating.

The OSPI Flash reset signal OSPI_RSTn is the output of an AND Gate that ANDs the Cold/Warm reset signal RESTSTATz_1V8 from the AM275x SoC, and the OSPI specific reset signal OSPI0_RESET_OUT0 from the AM275x SoC.

The OSPI Flash is supplied through an on board 1.8V system power VCC1V8_SYS. The OSPI I/O group is powered by the VDDSHV1 domain of the AM275x SoC and is also connected to 1.8V system power VCC1V8_SYS.

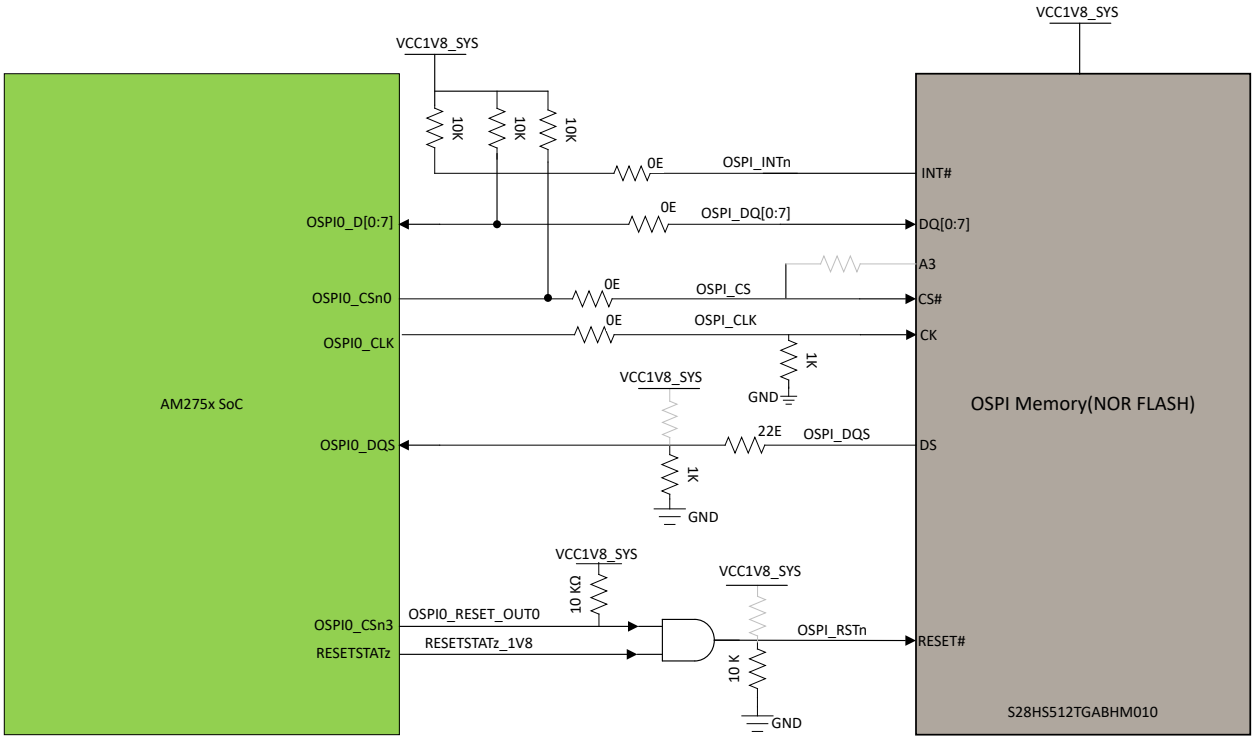


Figure 2-21. OSPI Interface Block Diagram

2.10.1.2 Board ID EEPROM

The AM275x EVM features an on-board EEPROM (CAT24M01WI-GT3) which stores the board's version and serial number data. The Board ID EEPROM is interfaced with the I2C0 port of the AM275x EVM SoC and is configured to respond to address 0x54. The I2C address of the EEPROM can be modified by driving the A2 and A1 pin HIGH/LOW to select one of the four possible addresses. The memory is preprogrammed with identification information for each board.

The EEPROM feautures write protection for the entire memory. To perform a write operation to the EEPROM, the WP pin must be shorted with jumper J33.

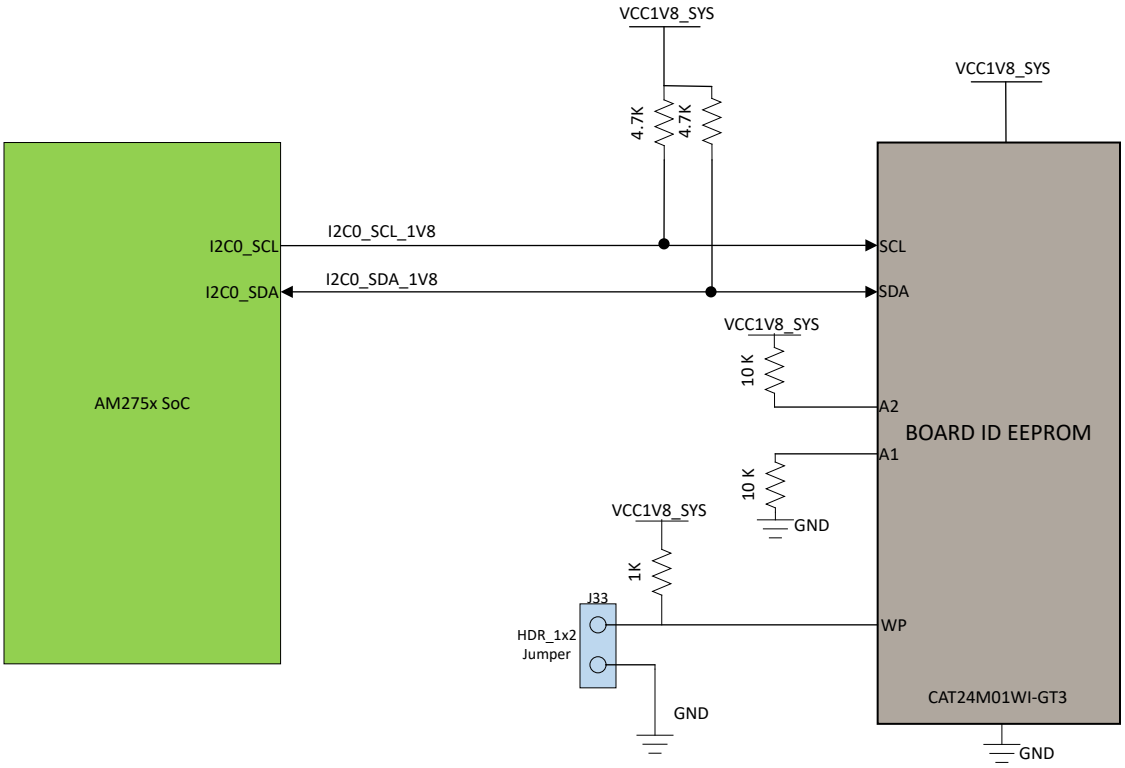


Figure 2-22. Board ID EEPROM Interface Diagram

2.10.1.3 MMC0 Interface

The AM275x SoC features a single MMC0 port (MMC0). MMC0 can be routed to either an eMMC Flash (MTFC32GAZAQHD-IT) or a Micro SD Card connector (MEM2052-00-195-00-A) through a 1:2 FET Switch (TS3DDR3812RUAR). MMC0 routing direction is determined by the MMC0_SEL_3V3 signal tied to the SELx pins of the FET Switch. MMC0_SEL_3V3 signal state (High or Low) is controlled by SW9 as shown in Figure 2-19.

Table 2-15. MMC0 Routing Truth Table

MMC0_SEL_3V3	MMC0	VDDSHV5 IO Voltage	SW9 Position
0	Micro SD interface	3.3V	ON
1	eMMC interface	1.8V	OFF

The AM275x EVM features a 32GB eMMC Flash memory (MTFC32GAZAQHD-IT), to which MMC0 can be routed to when SW9 (Figure 2-19) is OFF.

The eMMC Flash is a communication and mass data storage device that includes a Multimedia Card (MMC) interface and a NAND Flash component.

The AM275x SoC MMC0 Interface supports High Speed Double Data Rates (DDR) up to 50MHz or 100MBps when routed to the eMMC Flash. The AM275x EVM features the option to populate external pull-up resistors on data lines eMMC0_D[1:7] to prevent bus floating. A series resistor close to the AM275X SoC is provided for the clock signal MMC0_CLK for signal integrity.

The eMMC Flash is powered by 3.3V (VCC_3V3_SYS) for NAND Memory and 1.8V (VCC1V8_SYS) for the eMMC Interface. The MMC0 I/O group is powered by the VDDSHV5 power domain, which is connected to 1.8V IO supply (SW9 OFF).

The eMMC Flash requires an active low reset from the host. By default, the hardware reset function is temporarily disabled in the eMMC Flash. The host must set ECSD register byte 162, bits [1:0] to 0x1 to enable this functionality before the host can use it. External Reset is provided by ANDing RESETSTATz from the AM275x SoC, and the eMMC specific reset signal GPIO_eMMC_RSTn from the 1.8V I/O Expander.

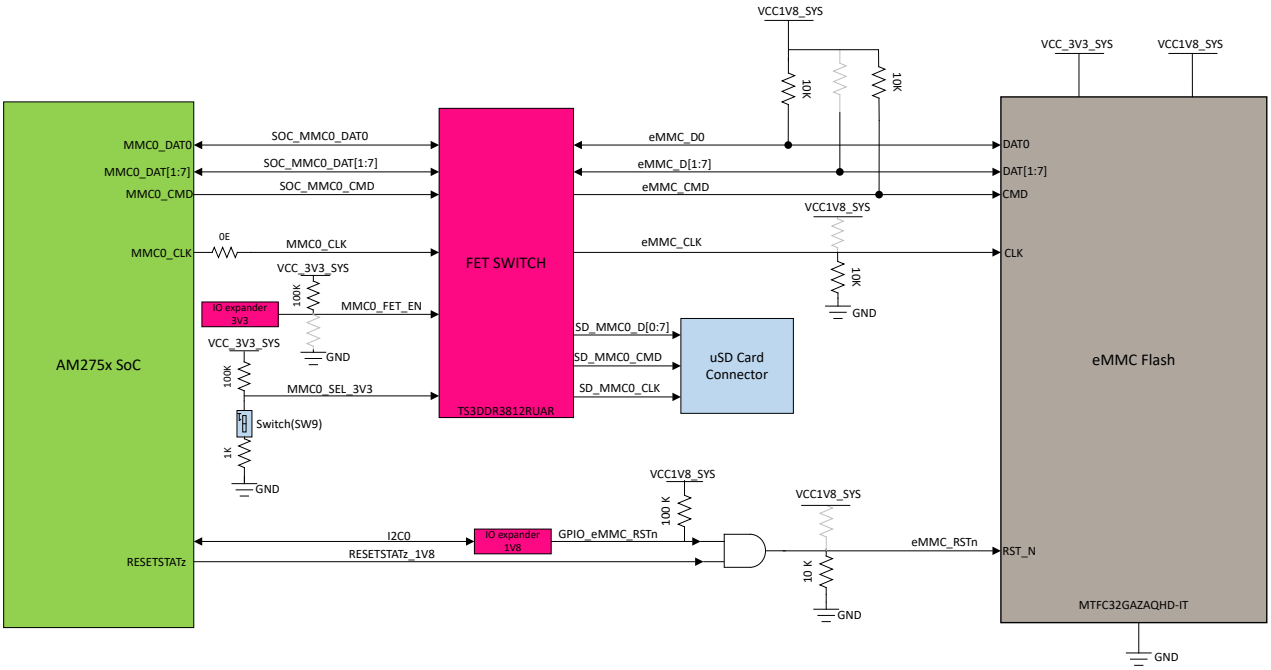


Figure 2-23. eMMC Interface Block Diagram

Additionally, MMC0 can be routed to a Micro SD card connector (MEM2052-00-195-00-A) when SW9 (Figure 2-19) is ON.

The AM275x SoC MMC0 Interface supports Ultra High-Speed Phase I (UHS_I) operation when routed to the Micro SD card.

The Micro SD card interface is set to operate in SD mode by default. For high-speed cards, the ROM Code of the AM275x SoC attempts to find the fastest speed that the card and the controller can support, then transition to 1.8V I/O through the VSEL_SD_SoC signal from the AM275x SoC.

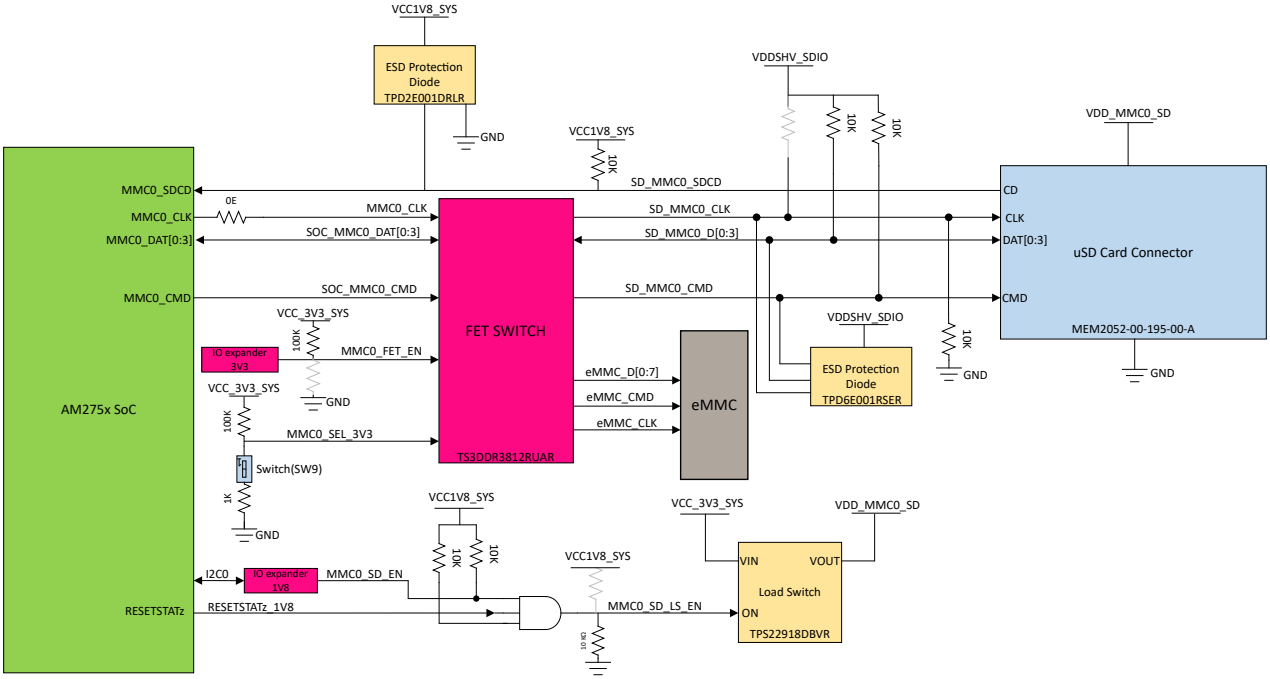


Figure 2-24. Micro SD Card Interface Block Diagram

2.10.1.4 HYPERRAM

The AM275x EVM features a 512Mb HYPERRAM (S80KS5122) that is mapped to the HYPERBUS0 interface of the AM275x SoC. The HYPERBUS0 interface supports clock speeds up to 166MHz DDR, achieving throughput of up to 333MBps.

The HYPERRAM reset signal HYPERBUS0_RST# is the output of an AND Gate that ANDs the Cold/ Warm reset signal RESTSTATz_1V8 from the AM275x SoC, and the HYPERRAM specific reset signal GPIO_HYPERRAM_RSTn from the AM275x SoC.

The HYPERRAM is supplied through an on board 1.8V system power VCC1V8_SYS. The OSPI I/O group is powered by the VDDSHV1 domain of the AM275x SoC and is also connected to 1.8V system power VCC1V8_SYS.

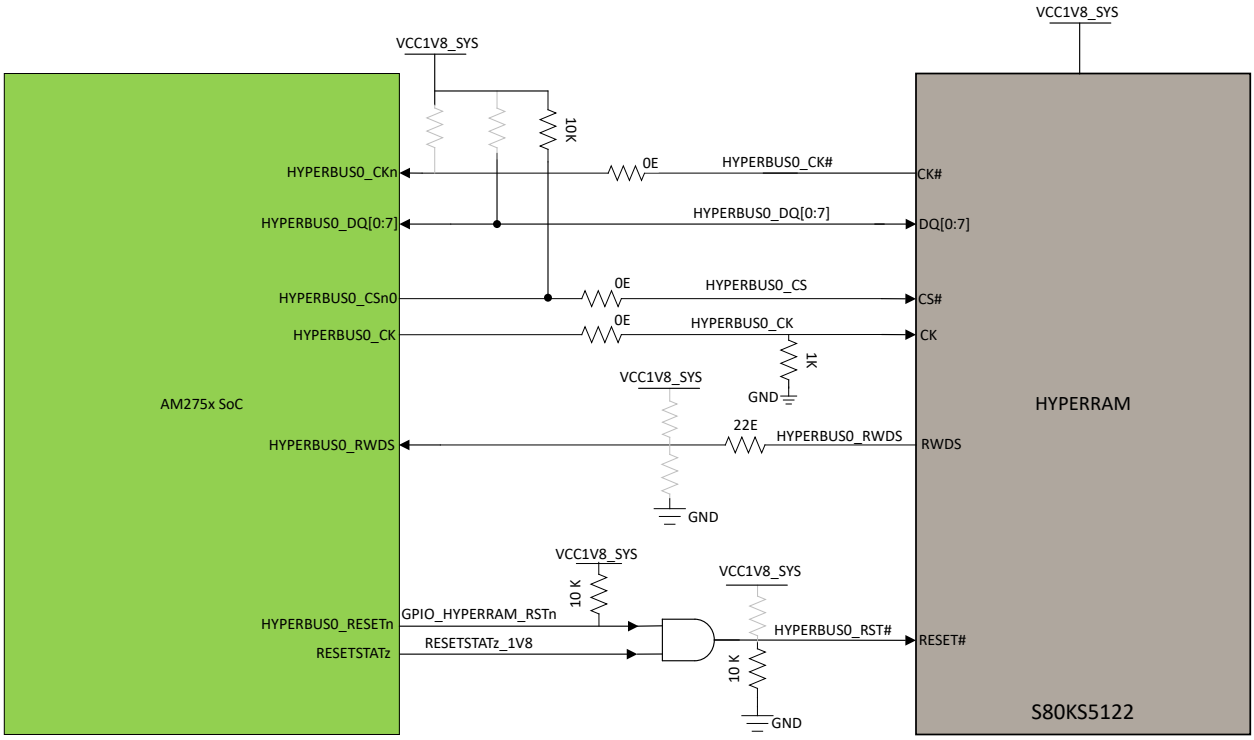


Figure 2-25. HYPERRAM Interface Block Diagram

2.10.2 Ethernet Interface

The AM275 EVM offers two 1Gb Ethernet Ports for external Communication. The AM275x SoC offers two CPSW3G Ethernet Reduced Gigabit Media Independent Interface(RGMII) Channels, RGMII1 and RGMII2, that are routed to two separate Ethernet Expansion Connectors.

The Ethernet Expansion Connectors can be interfaced with an Industrial Ethernet Daughter Card or an Automotive Ethernet Daughter Card, which provides flexibility.

Ethernet Expansion Connectors (CPSW RGMII1 and CPSW RGMII2) Ports share a common MDIO Bus to communicate with an external PHY Transceiver.

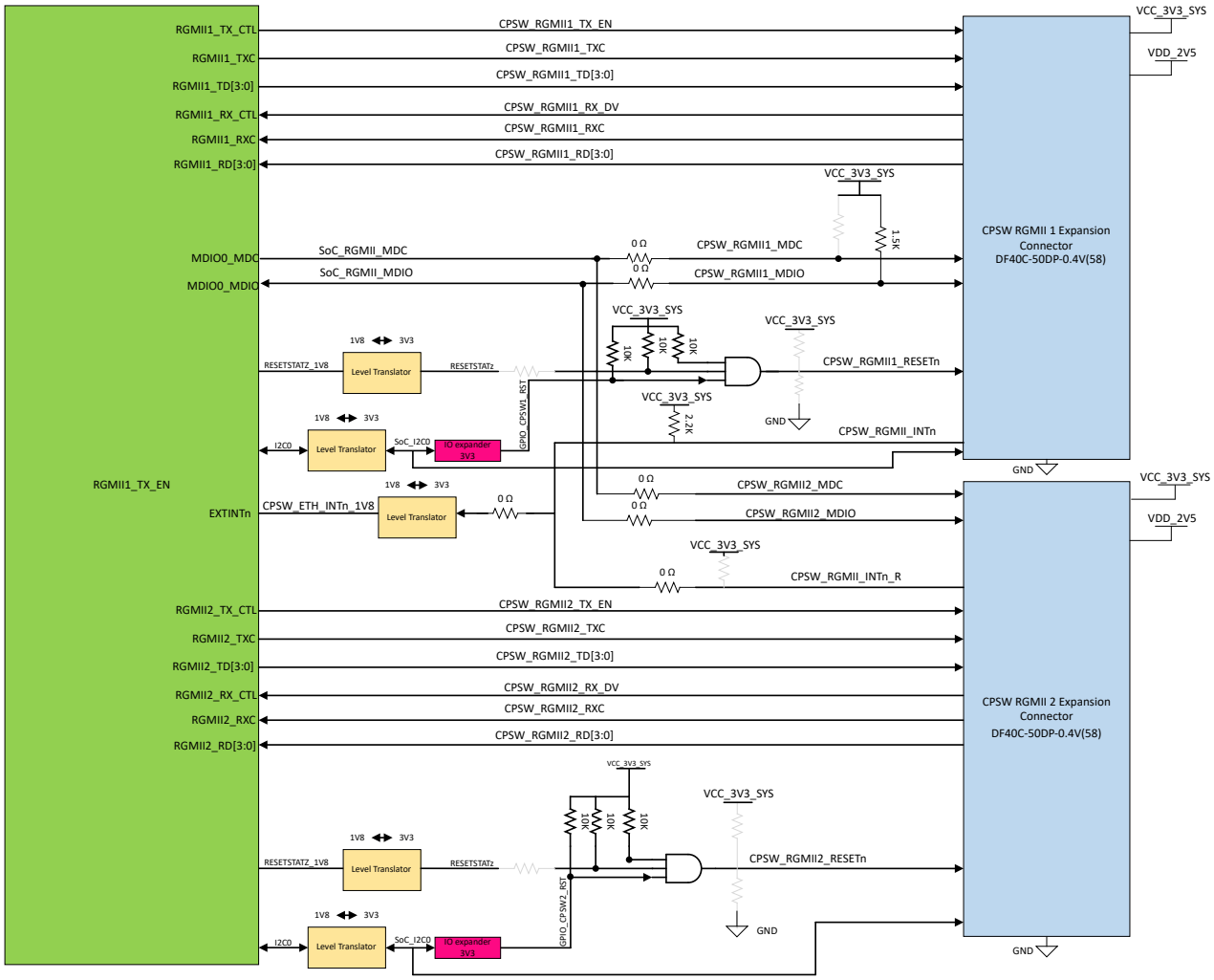


Figure 2-26. Ethernet Interface Block Diagram

2.10.2.1 Ethernet Add-on Connectors

The AM275x EVM features two Common Platform Switch (CPSW) RGMII Ethernet Expansion Connectors.

Table 2-16 lists the pinouts for the Ethernet expansion connectors:

Note

I/O direction refers to the direction from the Ethernet Expansion connector perspective.

Table 2-16. CPSW RGMII Ethernet Expansion Connector 1 Pinout

Pin Number	Net Name/Signal	I/O Direction	Pin Number	Net Name/Signal	I/O Direction
1	DGND	POWER	2	EXT_VMON2_1	POWER
3	CPSW_RGMII1_TXC	INPUT	4	VDD_2V5	POWER
5	DGND	POWER	6	VDD_2V5	POWER
7	CPSW_RGMII1_TD0	INPUT	8	DGND	POWER
9	CPSW_RGMII1_TD1	INPUT	10	CPSW_RGMII_INTn	OUTPUT
11	CPSW_RGMII1_TD2	INPUT	12	CPSW_RGMII1_RESETn	INPUT
13	CPSW_RGMII1_TD3	INPUT	14	CPSW_RGMII1_COL	OUTPUT
15	DGND	POWER	16	DGND	POWER
17	DGND	POWER	18	DGND	POWER
19	CPSW_RGMII1_RXC	OUTPUT	20	CPSW_RGMII1_MDC	INPUT
21	DGND	POWER	22	CPSW_RGMII1_MDIO	BIDIRECTIONAL
23	CPSW_RGMII1_RD0	OUTPUT	24	DGND	POWER
25	CPSW_RGMII1_RD1	OUTPUT	26	RGMII1_INH_3V3	OUTPUT
27	CPSW_RGMII1_RD2	OUTPUT	28	CPSW_RGMII1_ETH1_CLK	INPUT
29	CPSW_RGMII1_RD3	OUTPUT	30	CPSW_RGMII1_CRS	OUTPUT
31	DGND	POWER	32	DGND	POWER
33	DGND	POWER	34	DGND	POWER
35	CPSW_RGMII1_TX_EN	INPUT	36	CPSW_RGMII1_BRD_CONN_DET	OUTPUT
37	I2C_ADDR0_A2	INPUT	38	SYNC1_OUT_ETH1	INPUT
39	RGMII1_RX_ER	OUTPUT	40	SoC_I2C0_SCL	INPUT
41	DGND	POWER	42	SoC_I2C0_SDA	BIDIRECTIONAL
43	RGMII1_RX_LINK	OUTPUT	44	VCC_3V3_SYS	POWER
45	CPSW_RGMII1_RX_DV	OUTPUT	46	VCC_3V3_SYS	POWER
47	I2C_ADDR0_A0	INPUT	48	CPSW_RGMII1_BCLK	OUTPUT

Table 2-17. CPSW RGMII Ethernet Expansion Connector 2 Pinouts

Pin Number	Net Name/Signal	I/O Direction	Pin Number	Net Name/Signal	I/O Direction
1	DGND	POWER	2	EXT_VMON2_2	POWER
3	CPSW_RGMII1_TXC	INPUT	4	VDD_2V5	POWER
5	DGND	POWER	6	VDD_2V5	POWER
7	CPSW_RGMII2_TD0	INPUT	8	DGND	POWER
9	CPSW_RGMII2_TD1	INPUT	10	CPSW_RGMII_INTn_R	OUTPUT
11	CPSW_RGMII2_TD2	INPUT	12	CPSW_RGMII2_RSTn	INPUT
13	CPSW_RGMII2_TD3	INPUT	14	CPSW_RGMII2_COL	OUTPUT
15	DGND	POWER	16	DGND	POWER
17	DGND	POWER	18	DGND	POWER
19	CPSW_RGMII2_RXC	OUTPUT	20	CPSW_RGMII2_MDC	INPUT
21	DGND	POWER	22	CPSW_RGMII2_MDIO	BIDIRECTIONAL
23	CPSW_RGMII2_RD0	OUTPUT	24	DGND	POWER

Table 2-17. CPSW RGMII Ethernet Expansion Connector 2 Pinouts (continued)

Pin Number	Net Name/Signal	I/O Direction	Pin Number	Net Name/Signal	I/O Direction
25	CPSW_RGMII2_RD1	OUTPUT	26	RGMII2_INH_3V3	OUTPUT
27	CPSW_RGMII2_RD2	OUTPUT	28	CPSW_RGMII2_ETH2_CLK	INPUT
29	CPSW_RGMII2_RD3	OUTPUT	30	CPSW_RGMII2_CRS	OUTPUT
31	DGND	POWER	32	DGND	POWER
33	DGND	POWER	34	DGND	POWER
35	CPSW_RGMII2_TX_EN	INPUT	36	CPSW_RGMII2_BRD_CONN_DET	OUTPUT
37	I2C_ADDR0_A2	INPUT	38	SYNC1_OUT_ETH2	INPUT
39	RGMII2_RX_ER	OUTPUT	40	SoC_I2C0_SCL	INPUT
41	DGND	POWER	42	SoC_I2C0_SDA	BIDIRECTIONAL
43	RGMII2_RX_LINK	OUTPUT	44	VCC_3V3_SYS	POWER
45	CPSW_RGMII2_RX_DV	OUTPUT	46	VCC_3V3_SYS	POWER
47	I2C_ADDR0_A0	INPUT	48	CPSW_RGMII2_BCLK	OUTPUT

2.10.3 Audio Interfaces

2.10.3.1 Audio Clocking

The AM275x EVM features two options for an audio clock reference on each MCASP Transmit(X) and Receive(R).

- An internally generated audio reference clock using the 24.576MHz crystal input on OSC1

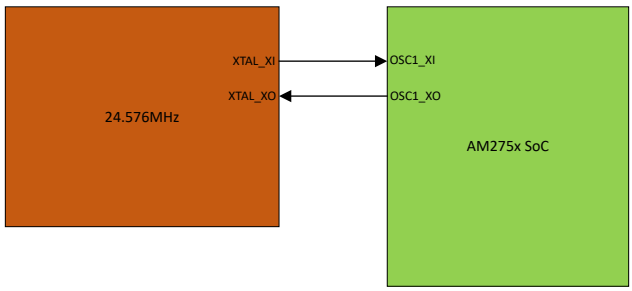


Figure 2-27. Internal Audio Reference Clock

- An externally generated audio reference clock from three options:
  - External Audio reference clock generated from clock generator(CDCE6214) to AUDIO_EXT_REFCLK2
  - External Audio reference clock generated from Audio expansion connectors AEC1 and AEC2 via AUDIO_EXT_REFCLK0 and AUDIO_EXT_REFCLK1, respectively.

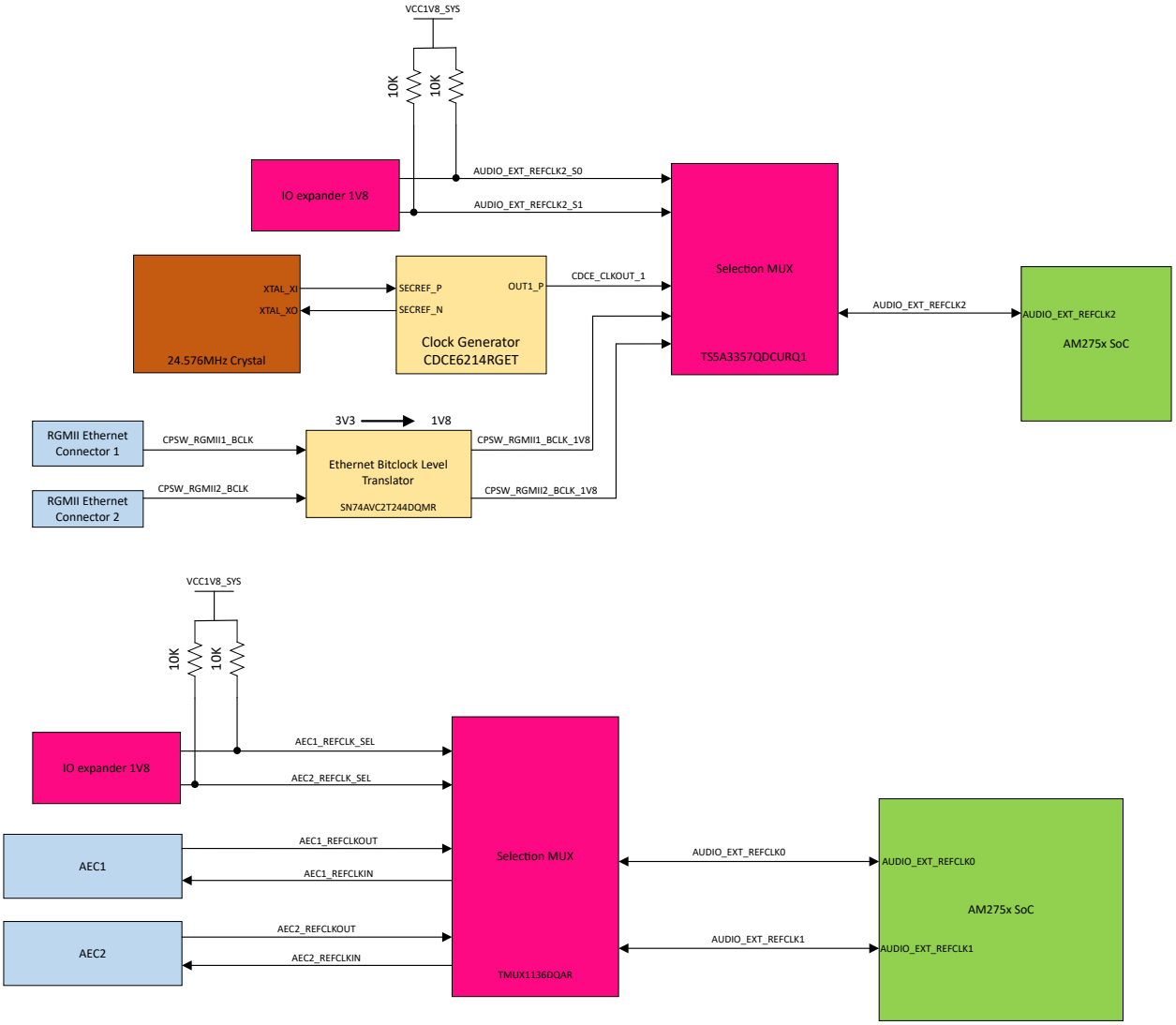


Figure 2-28. External Audio Reference Clocks

2.10.3.2 McASP

The AM275x features five Multichanel Audio Serial Ports (McASP), McASP[0:4]. Each McASP features independent clock zones for transmit and receive.

McASP1 is used for AM275x EVM on-board ADC/DAC Input and Outputs.

The ADC/DAC Input and Outputs featured on the AM275x EVM consist of:

- Four output 3.5mm TRS Audio Jack connectors for Eight Stereo Channel DAC Line AC-coupled outputs. Each individual TRS Audio Jack Connector is connected to a two-channel Stereo Audio DAC(TAD5212) device (four DACs in total).
- Four input 3.5mm TRS Audio Jack connectors for Eight Stereo Channel Microphone/Line AC-coupled inputs. Each Pair of the TRS Audio Jack Connectors are connected to a four-channel Audio ADC(PCM6240) device (two ADCs in total).

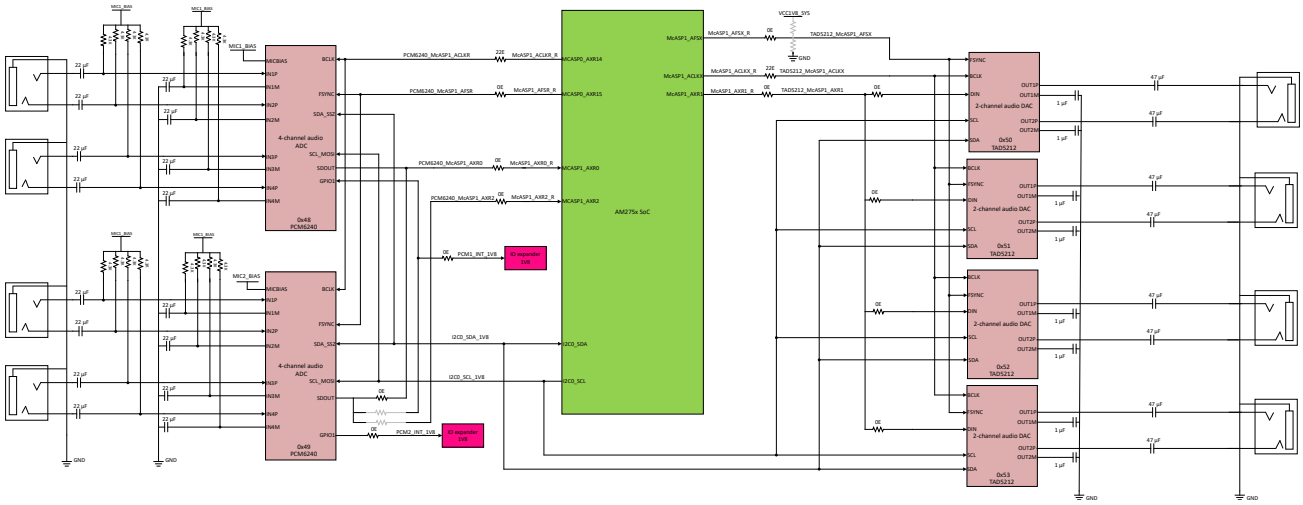


Figure 2-29. McASP1

McASP0 is used as the primary McASP interface for Audio Expansion Connector 1 (AEC1). McASP0 has Eight Audio Transmit/Receive channels(McASP0_AXR[0:7]) .

McASP4 is used as the secondary McASP interface for Audio Expansion Connector 1 (AEC1). McASP4 has Four Transmit/Receive channels (McASP4_AXR0, McASP4_AXR[3:5]). McASP4 can be routed to the McASP4/MLB Header through a 1:2 MUX (SN74CBTLV). Routing McASP4 to MLB Header requires population jumper J29 to define I/O Voltage level on MLB Header.

McASP2 is used as the primary McASP interface for Audio Expansion Connector 2 (AEC2). McASP2 has Six Audio Transmit/Receive channels (McASP2_AXR[0:5]).

McASP3 is used as the primary McASP interface for Audio Expansion Connector 2 (AEC2). McASP3 has Four Audio Transmit/Receive channels (McASP3_AXR[0:3]).

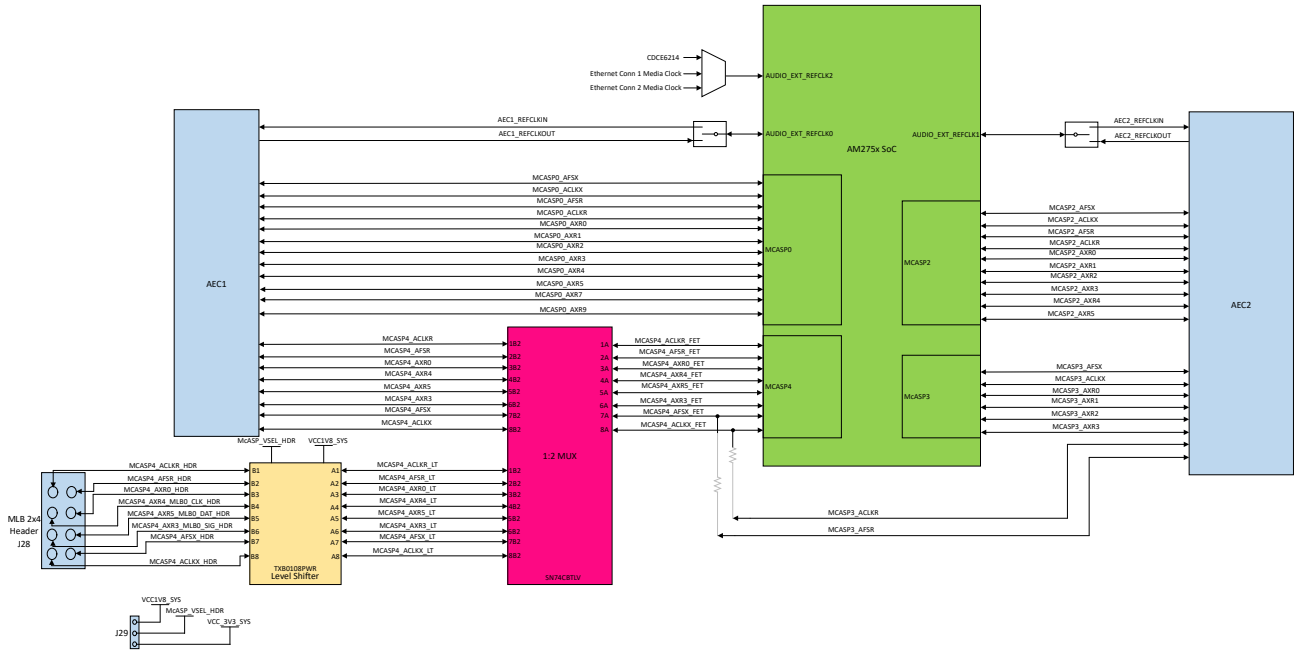


Figure 2-30. McASP0, McASP2, McASP3, McASP4

Note

For additional Information on McASP features and configuration, go to *McASP Design Guide*.

2.10.3.3 MLB

The AM275x EVM features a Media Local Bus (MLB) Header option. A 1:2 Switch MUX (SN74CBTLV) selects the AM275x SoC Audio signals between the MLB header or AEC1. The McASP_FET_SEL signal is the selection bit for this MUX. The MLB header option goes through a Level Shifter (TXB0108PWR) that has the voltage level defined by header J29.

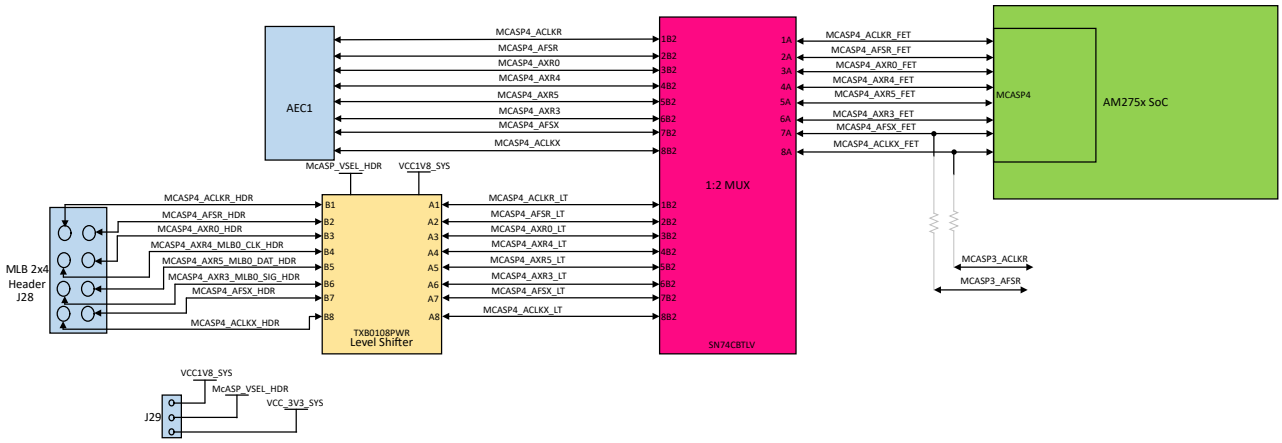


Figure 2-31. MLB Header

2.10.4 I2C Interface

The AM275x EVM Features four I2C Interfaces from the AM275x SoC:

- I2C0 Interface: The I2C0 Port of the AM275x SoC is mapped to the Board ID EEPROM, USB PD Controller, PCM6240 (x2) , TAD5212 (x4), CDCE6214, Current Monitors (x7), Temperature Sensor, CPSW RGMII Expansion Connectors (x2) and GPIO Expanders (x2)
- I2C3 Interface: The I2C3 Port of the AM275x SoC is mapped to the Audio Expansion Connector 1 (AEC 1)
- I2C5 Interface: The I2C5 Port of the AM275x SoC is mapped to the Audio Expansion Connector 2 (AEC 2)
- WKUP_I2C0 Interface: The WKUP_I2C0 Port of the AM275x SoC is mapped to the PMIC for Q&A Watchdog.

The Bootmode IO Expander I2C pins are mapped to the I2C1 port of the XDS110 Debugger through the BOOTMODE_I2C signals.

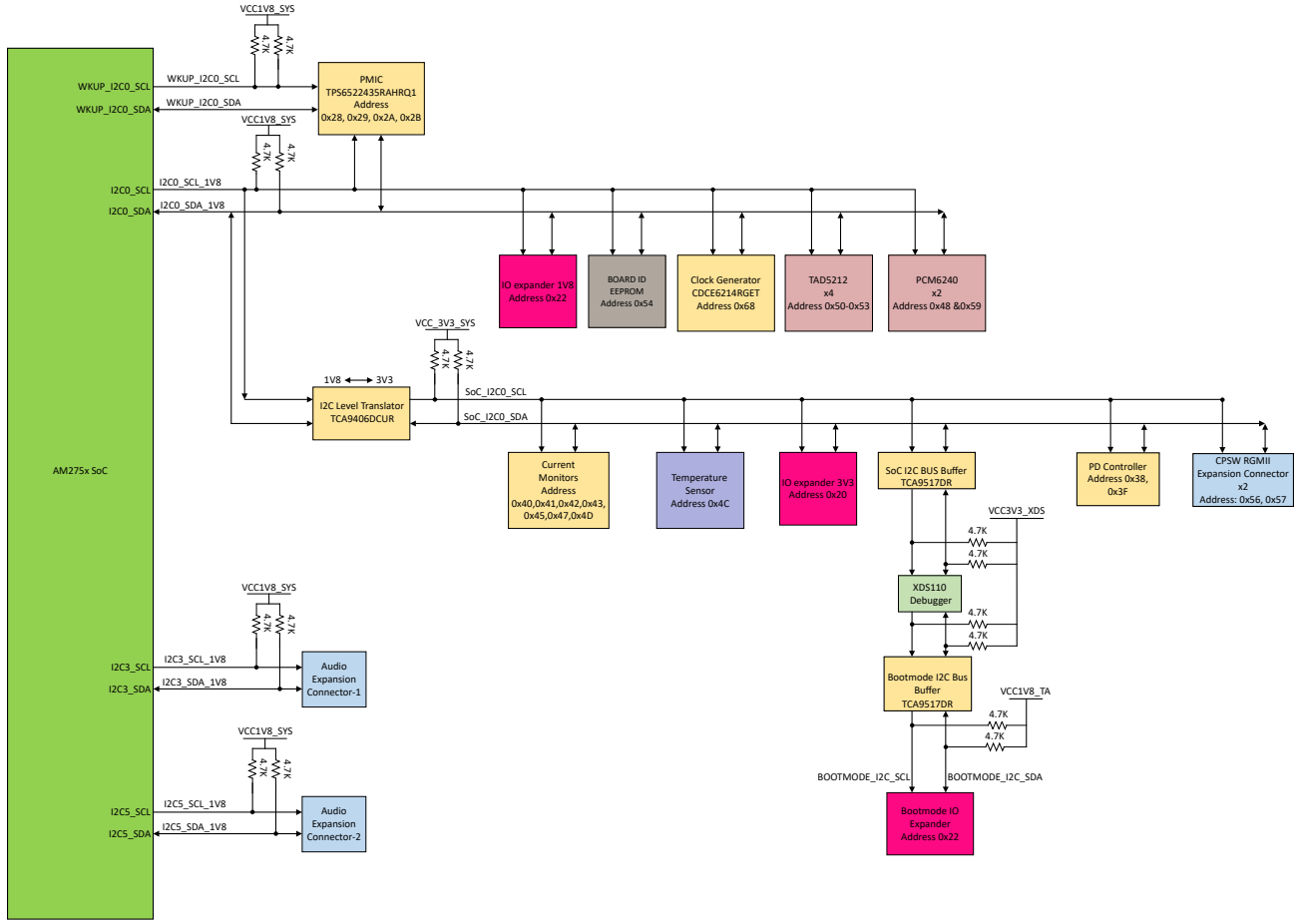


Figure 2-32. I2C Interface Tree

Table 2-18. I2C Mapping Table

I2C Port	Device	Part Number	I2C Address
I2C0	Board ID EEPROM	CAT24M01WI-GT3	0x54
I2C0	Ethernet Expansion Connector 1	DF40C-50DP-0.4V(58)	0x57
I2C0	Ethernet Expansion Connector 2	DF40C-50DP-0.4V(58)	0x56
I2C0	USB PD Controller	TPS65988DHRSHR	0x38, 0x3F
I2C0	4-channel Audio ADCs	PCM6240QRTVRQ1	0x48, 0x49
I2C0	2-Channel Audio DACs	TAD5212IRGER	0x50, 0x51, 0x52, 0x53
I2C0	Clock Generator	CDCE6214RGET	0x68
I2C0	Current Monitors	INA228AIDGSR	0x40, 0x41, 0x42, 0x43, 0x45, 0x47, 0x4D
I2C0	Temperature Sensors	TMP411ADR	0x4C
I2C0	GPIO Expander 1V8	TCA6424ARGJR	0x22
I2C0	GPIO Expander 3V3	TCA6416ARTWR	0x20
I2C0	PMIC	TPS6522435RAHRQ1	0x28,0x29,0x2A, 0x2B
WKUP_I2C0			0x12
I2C3	Audio Expansion Connector 1	QSE-040-01-L-D-A	
I2C5	Audio Expansion Connector 2	QSE-040-01-L-D-A	
XDS110			
BOOTMODE_I2C	Bootmode I/O Expander	TCA6424ARGJR	0x22

2.10.5 SPI

The AM275x EVM features two SPI Interfaces:

- SPI0 : SPI0 Port is mapped from the AM275x SoC to Audio Expansion connector 1 (AEC1)
- SPI1 : SPI1 Port is mapped from the AM275x SoC to Audio Expansion connector 2 (AEC2)

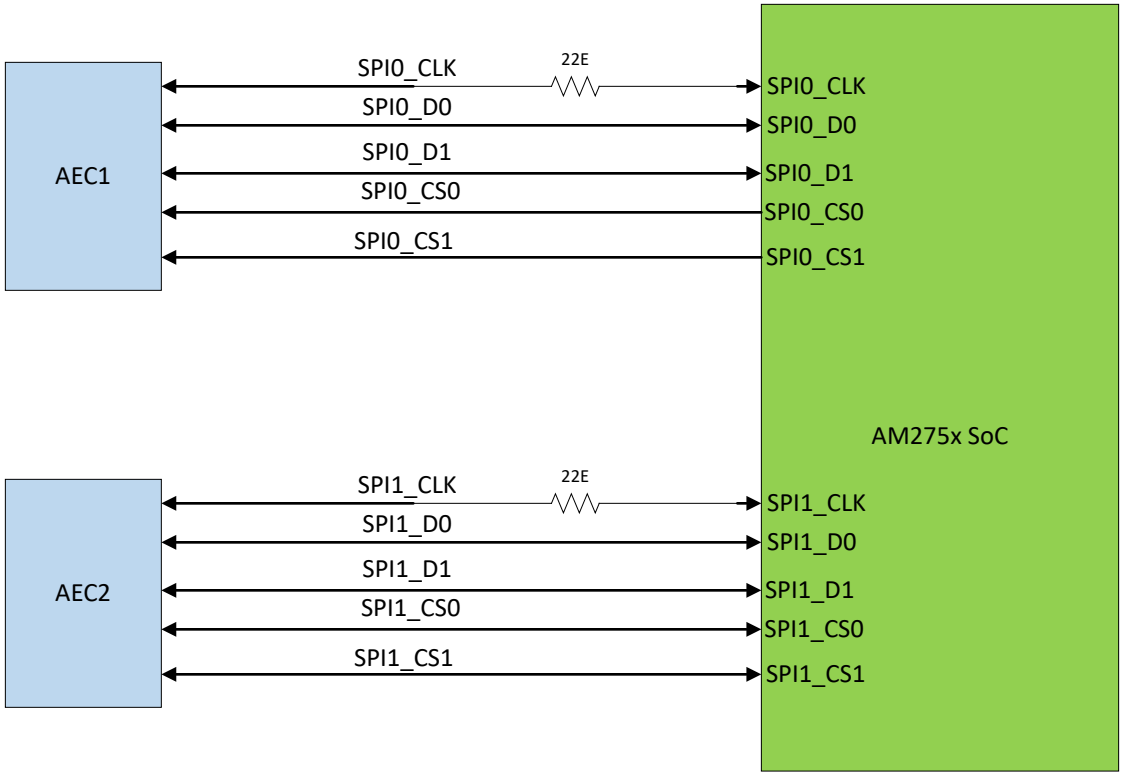


Figure 2-33. SPI Interface Block Diagram

2.10.6 UART

The AM275x EVM features four UART Ports:

- WKUP_UART0
- UART2
- UART3
- UART0

The WKUP_UART0, UART2, and UART3 ports are routed from the AM275x SoC to a FDTI Bridge (FT4232HL) for USB to UART conversion. The FDTI Bridge routes to a Micro-B USB Connector (J22).

The UART0 port is routed from the AM275x SoC to the XDS110 debugger (TM4C1294). The XDS110 Debugger routes to another Micro-B USB Connector (J17).

When the AM275x EVM is connected to a host via a USB cable on either of these Micro-B USB connectors, the host can establish a Virtual COM Port, allowing communication through any terminal emulation application.

Both the FT4232HL and TM4C1294 devices are bus powered. Because both devices are powered through the USB BUS, the connection to the COM port is not lost when the AM275x EVM power is removed.

Table 2-19. UART Mapping Table

UART Port	USB to UART Bridge	USB Connector	COM Port (1)
UART0	TM4C1294	J17	XDS110 User UART
UART2	FT4232HL	J22	FT4232 Serial Bus A
UART3			FT4232 Serial Bus B
WKUP_UART0			FT4232 Serial Bus C

(1) FT4232 Serial Bus D is left NC

The FT4232 Bridge is configured to operate in 'Single chip USB to four channel UART' mode using the configuration file from an external SPI EEPROM (93LC46B) connected to it. The EEPROM supports a 1 Mbit/s clock rate. The EEPROM is programmable in-circuit over USB using a utility program called FT_PROG available from FTDI's web site. FT_PROG is also used for programming the board's serial number for users to identify the connected COM port with board serial number when one or more boards are connected to the computer.

Instead of the FTDI Bridge, UART2 and UART3 ports can be routed from the AM275x SoC to AEC1 and AEC2, respectively, by selection MUXes (TMUX1136DQAR), through the UART2_FET_SEL and UART3_FET_SEL signals.

Table 2-20. UART2 Select Truth Table

UART2_FET_SEL	UART2_TXD_FET	UART2_RXD_FET
0 (DEFAULT)	FT4232_UART2_TXD_1V8	FT4232_UART2_RXD_1V8
1	UART2_TXD	UART2_RXD

Table 2-21. UART3 Select Truth Table

UART3_FET_SEL	UART3_TXD_FET	UART3_RXD_FET
0 (DEFAULT)	FT4232_UART3_TXD_1V8	FT4232_UART3_RXD_1V8
1	UART3_TXD	UART3_RXD

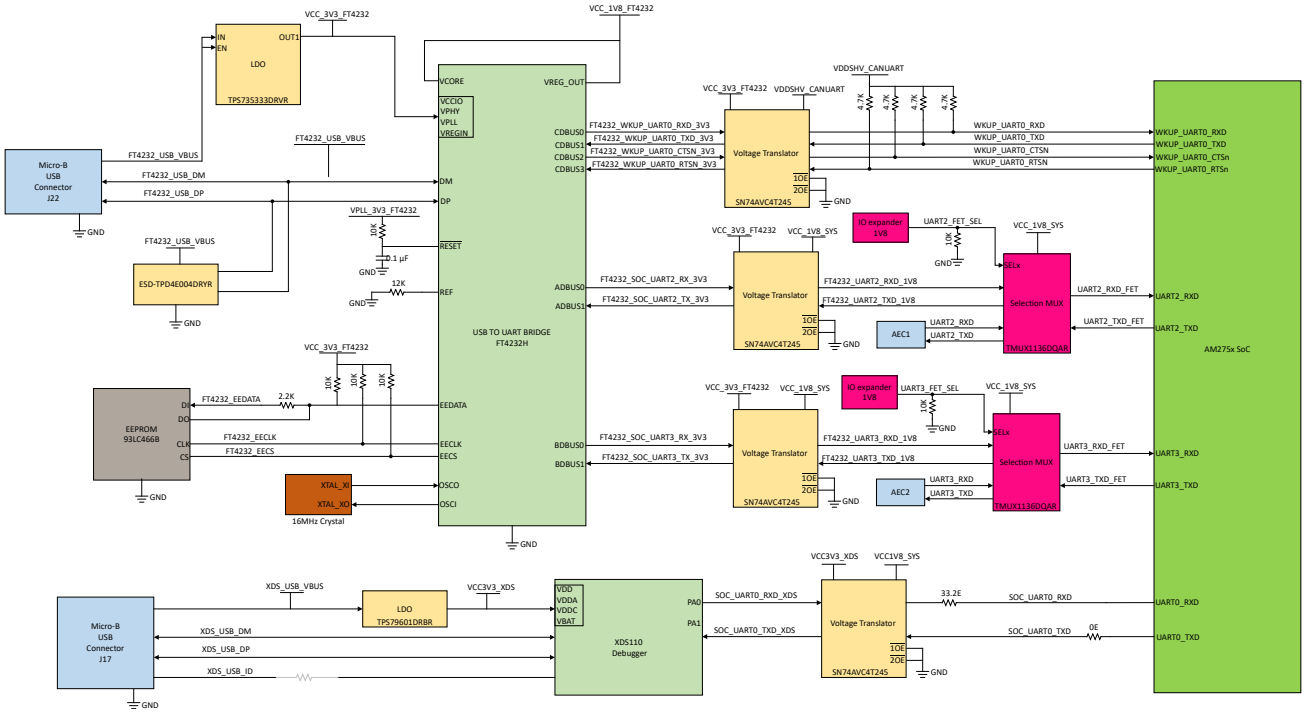


Figure 2-34. UART Interface Block Diagram

2.10.7 MCAN

The AM275x EVM features a single MCAN Transceiver (TCAN1043ADYYRQ1) that is mapped to the MCAN0 Interface of the AM275x SoC. The MCAN Transceiver has three independent power inputs: VIO, VCC and VSUP. VIO is the transceiver 1.8V system level supply voltage, VCC is the CAN transceiver 5V supply voltage, and VSUP provides the supply to the internal regulators that support the digital core and the low power CAN receiver.

A 120Ω split termination on the MCAN0_CAN_H and MCAN0_CAN_L signals is provided to improve Electromagnetic Interference (EMI) performance. Split termination improves the electromagnetic emission's behavior of the network by eliminating fluctuations in the bus common-mode voltages at the start and end of message transmissions.

The WAKE pin of the Transceiver provides local wake-up (LWU) function. A local Wake-up event occurs when the state of the WAKE pin transitions from high-to-low or low-to-high. When a LWU event occurs, the device comes out of sleep-mode.

The INH Pin enables the transceiver to Enable/Disable the EVM's peripheral power supply buck regulator (LM61460AASQRJRRQ1).

The EN pin of the transceiver provides an input for transceiver mode control in conjunction with the nSTB pin.

The nSTB pin of the transceiver provides an input for transceiver stand-by mode control.

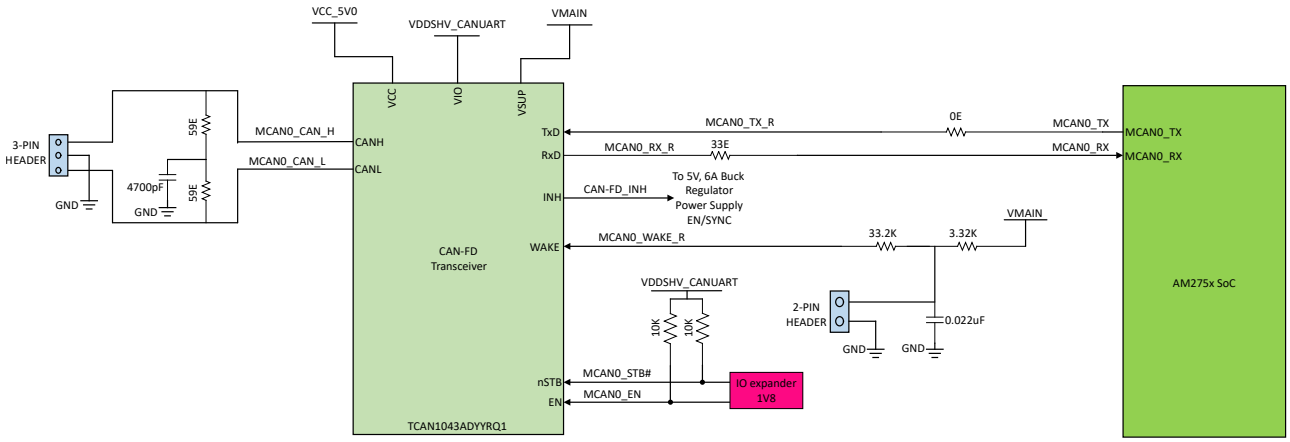


Figure 2-35. MCAN Interface Block Diagram

2.10.8 JTAG

The AM275x EVM features an XDS110 class on-board JTAG emulation IC (TM4C1294NCPDTT3R). The XDS110 class on-board JTAG emulator connects to a Micro-B USB 2.0 Connector (J17). The XDS_USB_VBUS signal from the USB connector powers the XDS110 such that connection to the XDS110 JTAG emulator is not lost when the AM275x EVM Power is removed. Voltage translation buffers are used to isolate the XDS110 JTAG emulator from the rest of the EVM.

Optionally, The AM275x EVM features a 20-pin Standard JTAG cTI Header (J19). This gives the option to connect the AM275x EVM to an external JTAG emulator through a JTAG emulator cable. Voltage translation buffers are used to isolate the JTAG signals of cTI header from the rest of the AM275x EVM.

Table 2-22. cTI JTAG Header Pinout

Pin Number	Signal
1	JTAG_TMS
2	JTAG_TRST#
3	JTAG_TDI
4	JTAG_TDIS
5	VCC_3V3_SYS
6	NC
7	JTAG_TDO
8	SEL_XDS110_INV
9	JTAG_cTI_RTCK
10	DGND
11	JTAG_cTI_TCK
12	DGND
13	JTAG_EMU0
14	JTAG_EMU1
15	JTAG_EMU_RSTn
16	DGND
17	NC
18	NC
19	NC
20	DGND

The JTAG signal outputs of the translation buffers from the XDS110 Section and the cTI Header Section are muxed and connected to the AM275x SoC JTAG Port. If a connection to the cTI 20 Pin JTAG connector is sensed using an automatic presence-detect circuit, the MUX routes the 20 pin signals from the cTI connector to the AM275x SoC in place of the on-board JTAG emulator.

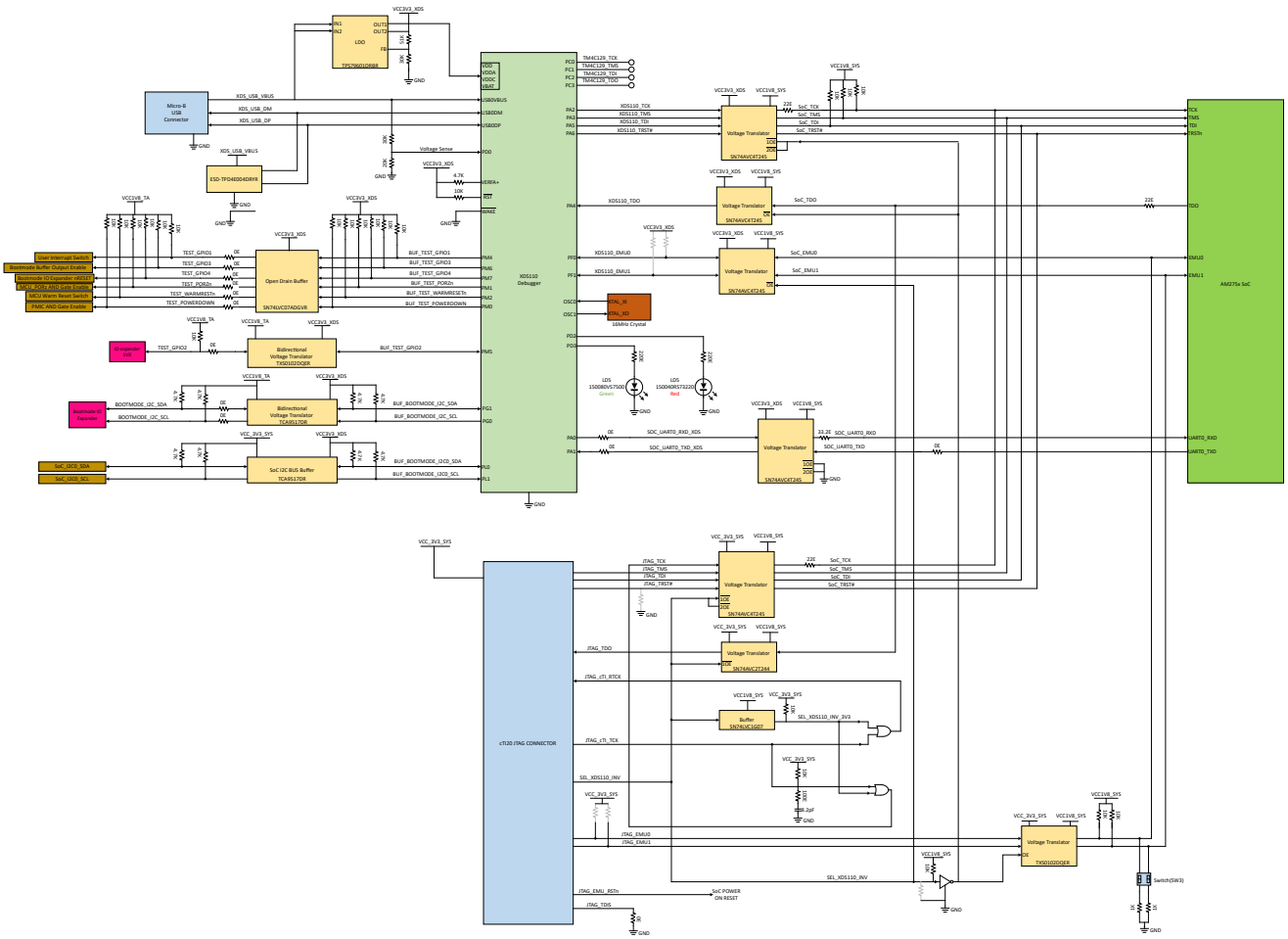


Figure 2-36. JTAG Interface Block Diagram

2.10.9 USB

The AM275x EVM features a USB 2.0 Interface through a USB Type-C connector (J25) that supports data rates up to 480Mbps. USB Type-C connector 2 (J25) can be used for data communication and/or a power supply connector to the AM275x EVM. The USB Type-C port is configured as a dual role port (DRP) port using the Dual PD controller (TPS65988DHRSHR), which means it can act either as a Host or a Device. The role of the port depends on the type of device getting connected to the EVM through the connector, and its ability to either sink or source. When the port is acting as a Downstream-Facing Port (DFP), it can source up to 5V at 500mA.

USB 2.0 Type-C connector 2 (J25) data lines, USBC_CONN2_DP and USBC_CONN2_DM are provided with a choke and an ESD protection device. VBUS_TYPEC2 to the Am275x SoC's USB0_VBUS is provided through a resistor divider network to support (5V-30V) VBUS operation.

A Common Mode Choke (DLW21SZ900HQ2B) is provided on USB Data lines for EMI/ EMC reduction. An ESD protection device (ESD122DMXR) is included to dissipate ESD strikes on USB2.0 DP/DM signals. ESD protection devices (TPD1E01B04DPLT) are included on CC signals for both USB-C connectors 1 and 2 (J24 and J25). A surge protection device (TVS2200DRVR) is included on the VBUS rail of Type-C Connector 2 (J25) to dissipate ESD strikes.

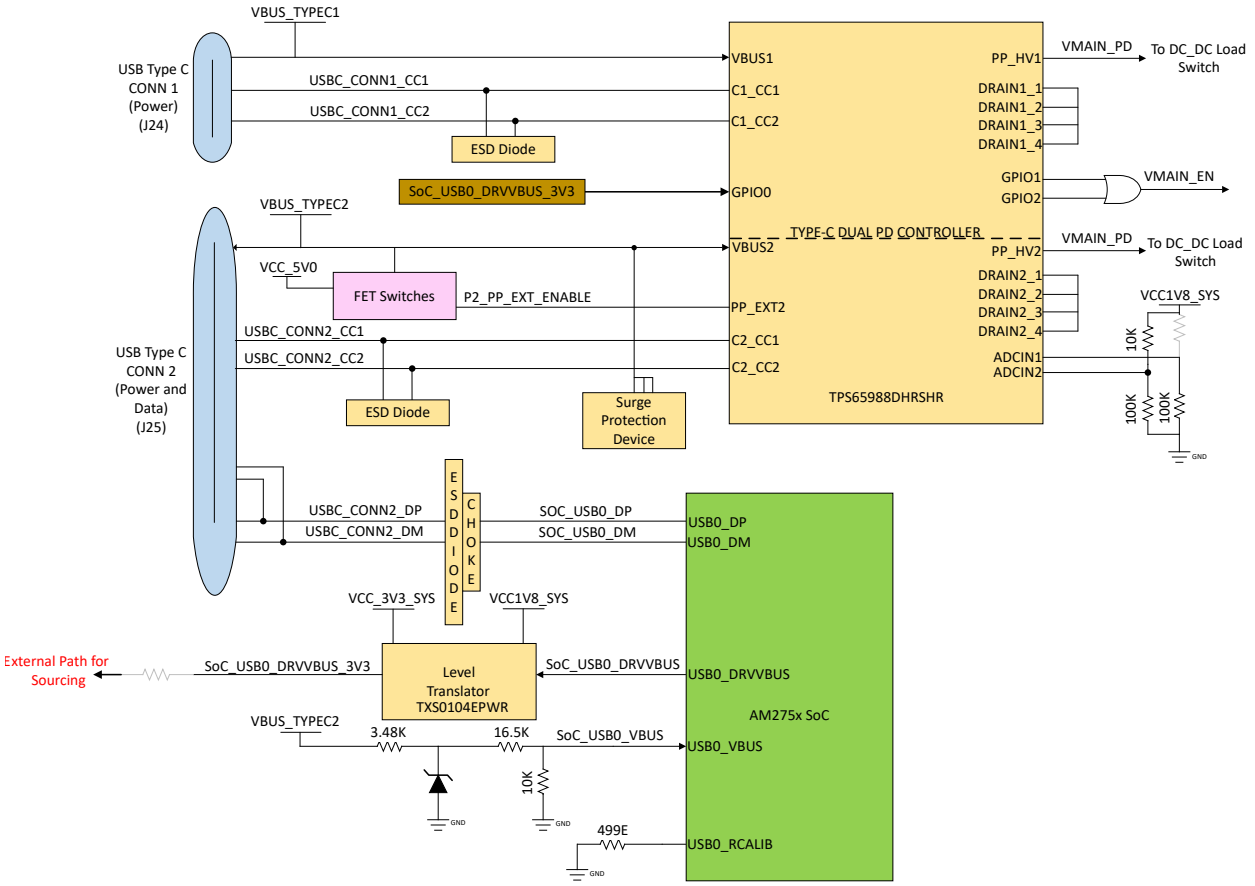


Figure 2-37. USB 2.0 Interface Block Diagram

2.10.10 ADC

The Am275x EVM features Eight ADC Analog input channels that are mapped to a 6X2 Header (J31). All ADC signals are ESD protected by an ESD protection device (TPD4E02B04DQAR).

A single pole, double-throw switch (SW11) dictates which 1.8V reference voltage source the AM275x ADC0 uses: VDDA_1V8 PMIC analog output, or an external 1.8V reference from ADC Header J31(Pin 2).

Table 2-23. ADC0_REFP Voltage Reference Switch

SW11 Position	Reference Selection
Position 1-2	On board 1.8V Reference (VDDA_1V8)
Position 3-2	External header Vref (ADC0_REFP_HDR)

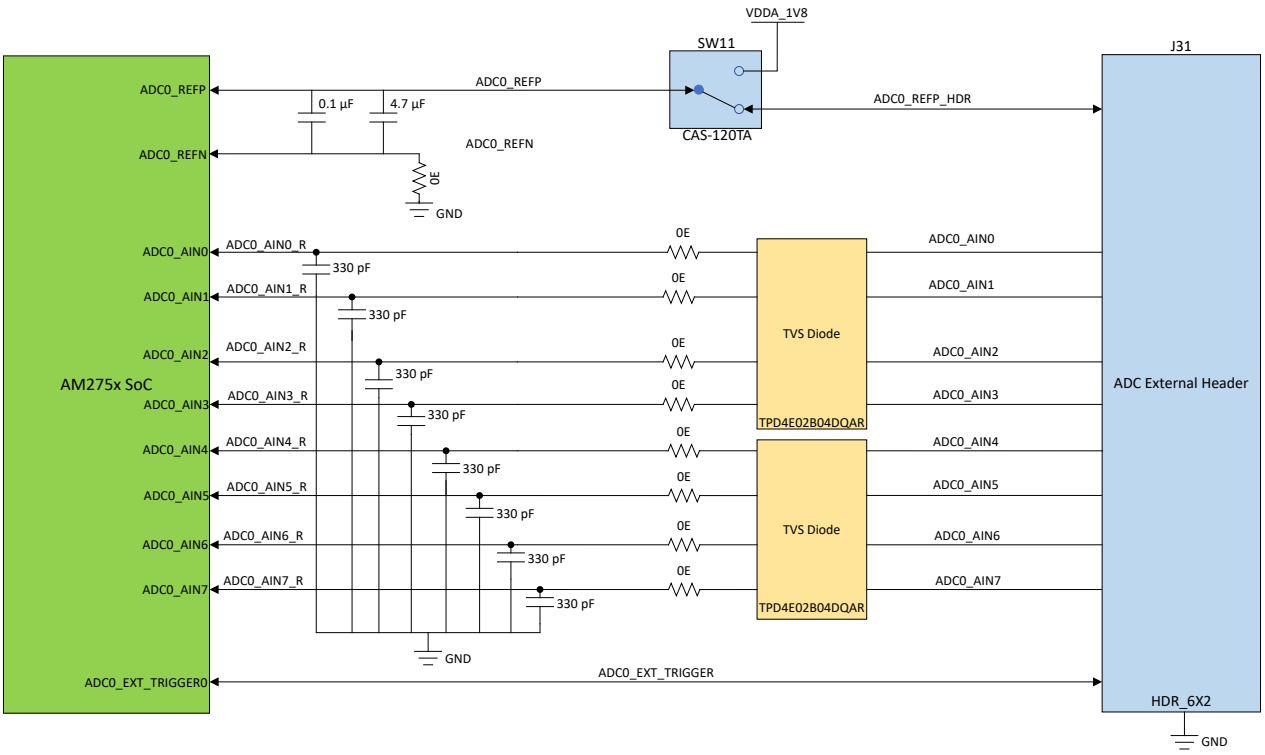


Figure 2-38. ADC Interface Block Diagram

2.11 AEC Mapping

2.11.1 Audio Expansion Connector 1

The following interfaces and IOs are included on Audio Expansion Connector 1 (AEC1):

- 1 x SPI : SPI0 with two chip selects (SPI0_CS0 and SPI0_CS1)
- 1 x I2C : I2C3
- 1 x UART : UART2
- 2 x PWM: EPWM0_A and EPWM0_B
- 1 x Reference Clock Input: AEC1_REFCLKIN
- 1 x Reference Clock Output: AEC1_REFCLKOUT
- 1 x MCAN: MCAN4
- 2 x eCAP: ECAP1 and ECAP2
- 2 x McASP : McASP0 and McASP4
- 2 x GPIO: AEC1_GPIO_0 and AEC1_GPIO_1
- 5V and 1.8V supply voltages (Current limited to 150mA and 250mA)

Table 2-24 lists all the AM275 EVM signals routed to AEC1.

Table 2-24. AEC1 Pinout

Pin Number	Net Name	Pin Number	Net Name
1	MCU_PORz	2	VCC_5V0
3	EPWM0_A	4	VCC_5V0
5	EPWM0_B	6	VCC_5V0
7	DGND	8	DGND
9	ECAP1_IN_APWM_OUT	10	VCC1V8_SYS
11	ECAP2_IN_APWM_OUT	12	VCC1V8_SYS
13	NC	14	NC

Table 2-24. AEC1 Pinout (continued)

Pin Number	Net Name	Pin Number	Net Name
15	DGND	16	DGND
17	SPI0_CLK	18	I2C3_SCL_1V8
19	SPI0_D0	20	I2C3_SDA_1V8
21	SPI0_D1	22	DGND
23	SPI0_CS0	24	SPI0_CS1
25	DGND	26	DGND
27	MCASP0_AXR0	28	MCASP0_AXR2
29	MCASP0_AXR1	30	MCASP0_AXR3
31	DGND	32	MCASP0_AXR4
33	AEC1_REFCLKIN	34	MCASP0_AXR5
35	DGND	36	DGND
37	MCASP0_ACLKX	38	MCASP0_AXR7
39	MCASP0_AFSX	40	MCASP0_AXR9
41	MCASP0_AFSR	42	AEC1_GPIO0_0
43	MCASP0_ACLKR	44	AEC1_GPIO0_1
45	DGND	46	DGND
47	AEC1_REFCLKOUT	48	NC
49	DGND	50	DGND
51	MCAN4_TX	52	NC
53	MCAN4_RX_R	54	NC
55	RESETSTATZ_1V8	56	NC
57	DGND	58	DGND
59	NC	60	UART2_TXD
61	NC	62	UART2_RXD
63	NC	64	NC
65	DGND	66	DGND
67	MCASP4_AXR0	68	NC
69	MCASP4_AXR3	70	NC
71	MCASP4_AXR4	72	NC
73	MCASP4_AXR5	74	NC
75	DGND	76	DGND
77	MCASP4_ACLKX	78	MCASP4_ACLKR
79	MCASP4_AFSX	80	MCASP4_AFSR

2.11.2 Audio Expansion Connector 2

The following interfaces and IOs are included on Audio Expansion Connector 2 (AEC2):

- 1 x SPI : SPI1 with two chip selects (SPI1_CS0 and SPI1_CS1)
- 1 x I2C : I2C5
- 1 x UART : UART3
- 1 x PWM: EPWM1_A
- 1 x Reference Clock Input: AEC2_REFCLKIN
- 1 x Reference Clock Output: AEC2_REFCLKOUT
- 1 x MCAN: MCAN1
- 2 x eCAP: ECAP0 and ECAP3
- 2 x McASP : McASP2 and McASP3
- 2 x GPIO: AEC2_GPIO_0 and AEC2_GPIO_1
- 5V and 1.8V supply voltages (Current limited to 150mA and 250mA)

Table 2-25 lists all the AM275 EVM signals routed to AEC1.

Table 2-25. AEC2 Pinout

Pin Number	NET NAME	Pin Number	NET NAME
1	MCU_PORz	2	VCC_5V0
3	EPWM1_A	4	VCC_5V0
5	NC	6	VCC_5V0
7	DGND	8	DGND
9	ECAP3_IN_APWM_OUT	10	VCC1V8_SYS
11	ECAP0_IN_APWM_OUT	12	VCC1V8_SYS
13	NC	14	NC
15	DGND	16	DGND
17	SPI1_CLK	18	I2C5_SCL_1V8
19	SPI1_D0	20	I2C5_SDA_1V8
21	SPI1_D1	22	DGND
23	SPI1_CS0	24	SPI1_CS1
25	DGND	26	DGND
27	MCASP2_AXR0	28	MCASP2_AXR2
29	MCASP2_AXR1	30	MCASP2_AXR3
31	DGND	32	MCASP2_AXR4
33	AEC2_REFCLKIN	34	MCASP2_AXR5
35	DGND	36	DGND
37	MCASP2_ACLKX	38	NC
39	MCASP2_AFSX	40	NC
41	MCASP2_AFSR	42	AEC2_GPIO0_0
43	MCASP2_ACLKR	44	AEC2_GPIO0_1
45	DGND	46	DGND
47	AEC2_REFCLKOUT	48	NC
49	DGND	50	DGND
51	MCAN1_TX	52	NC
53	MCAN1_RX_R	54	NC
55	RESETSTATZ_1V8	56	NC
57	DGND	58	DGND
59	NC	60	UART3_TXD
61	NC	62	UART3_RXD
63	NC	64	NC
65	DGND	66	DGND
67	MCASP3_AXR0	68	NC
69	MCASP3_AXR1	70	NC
71	MCASP3_AXR2	72	NC
73	MCASP3_AXR3	74	NC
75	DGND	76	DGND
77	MCASP3_ACLKX	78	MCASP3_ACLKR
79	MCASP3_AFSX	80	MCASP3_AFSR

2.12 Test Points

The AM275 EVM features multiple test points for power, ground, and critical signals.

Table 2-26 outlines test points for each power output on the AM275x EVM.

Table 2-26. Test Points

Test Point	Power Supply	Voltage
TP107	VBUS_TYPEC1	5V/9V/15V
TP108	VBUS_TYPEC2	5V/9V/15V
TP104	VMAIN	5V/9V/15V
TP96	FT4232_USB_VBUS	5V
TP86	SOC_DVDD1V8	1.8V
TP83	SOC_DVDD3V3	3.3V
TP103	VCC_5V0	5V
TP79	VDDA_1V8	1.8V
TP53	VDD_CORE	0.85V/0.75V
TP60	VDDR_CORE	0.85V
TP92	VDD_2V5	2.5V
TP69	VPP_1V8	1.8V
TP68	VCC3V3_XDS	3.3V
TP21	VDD_MMC0_SD	3.3V
TP78	XDS_USB_VBUS	5V
TP74	VINT_LDO	1.8V
J29.3	VCC_3V3_SYS	3.3V
J29.1	VCC1V8_SYS	1.8V
TP80	VDDSHV_CANUART	1.8V
TP52	VDD_CANUART	0.85V
TP75	PMIC_LPM_EN0	1.8V
TP81	PMIC_EN	1.8V
TP54	MCU_ERRORn	1.8V
TP50	MCU_RESETz	1.8V
TP592	RESETSTATz	1.8V
TP100	RESETSTATz_1V8	1.8V
TP586	WKUP_CLKOUT0	1.8V
TP49	MCU_PORz	1.8V
TP587	OSBCLK0	1.8V
J34.2, J9.2, TP1, J7.2, TP40, TP44, TP42, TP41, TP85, J32.2, TP106, J2.2, J21.2, J21.10, J31.12, TP2	DGND	0V

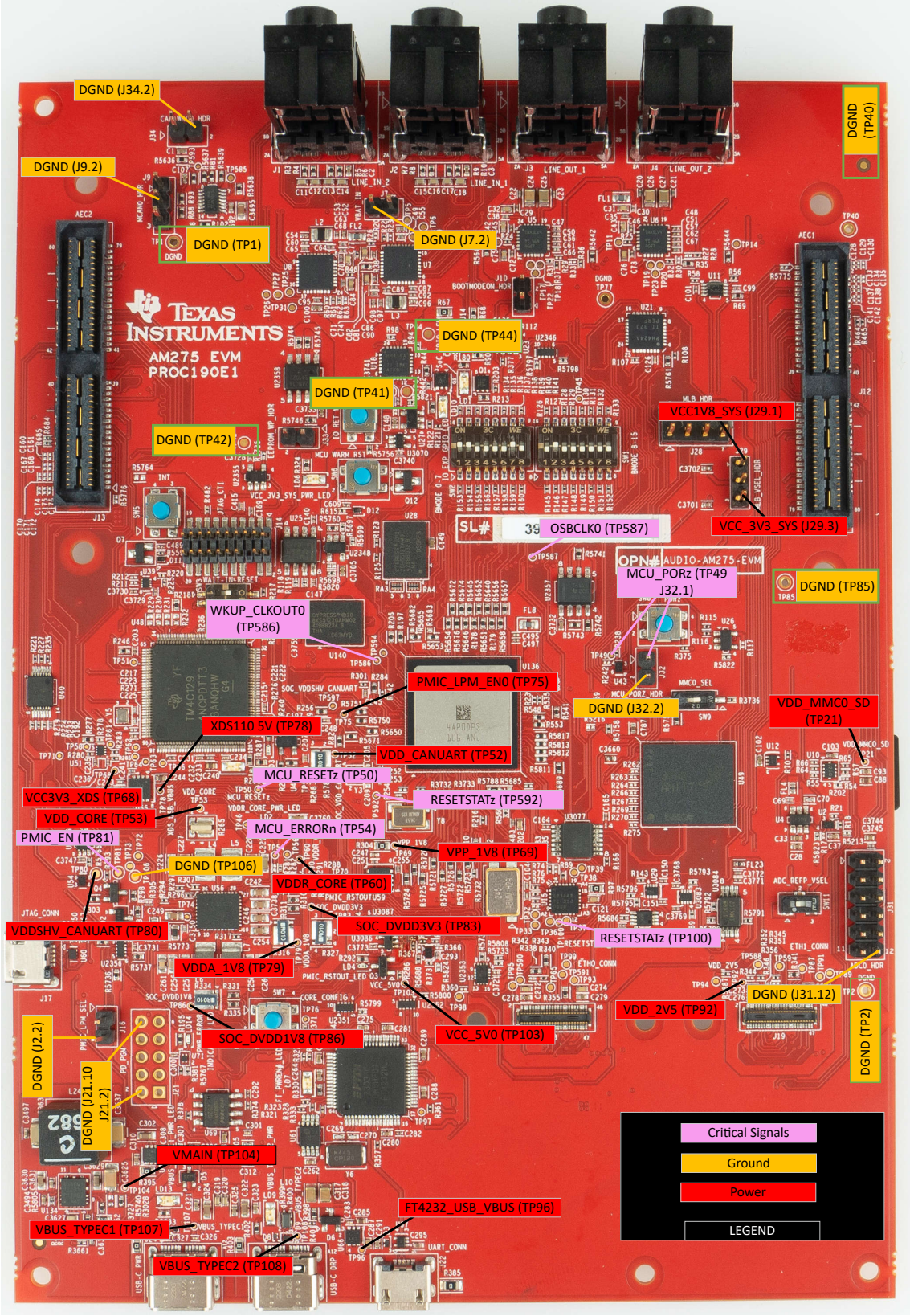


Figure 2-39. Test Points

3 Hardware Design Files

To download the zip file containing the latest design files for the EVM, click the following *link*

4 Additional Information

4.1 If You need Assistance

If you have any feedback or questions, support for the AM275x EVM is provided by the TI Product Information Center (PIC) and the TI E2E™ Forum. Contact information for the PIC can be found on the TI website. Additional device-specific information can be found in Section 5.1.

4.2 Trademarks

Ethernet™ is a trademark of ODVA, Inc.
Code Composer Studio™ is a trademark of Texas Instruments.
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All trademarks are the property of their respective owners.

4.3 Rev. E2 Design Changes

The AM275x EVM had various design changes for Revision E2 of the board. The changes are listed below:

- Replaced C640 with a 1uF Capacitor, and replaced R680 and R677 with 1 kilo-ohm resistors to remove undesired leakage on VCC_5V0 rail.
- Replaced C213 and C216 with 18pf capacitor for load capacitance increase.
- Replaced GPIO_eMMC_RSTn pull-up resistor R115 with 10 kilo-ohm resistor.
- Replaced eMMC data[D7-D0] & CMD pin pull-up resistors with 47 kilo-ohm resistors.
- Replace the uSD connector signals' pull-up resistors with 47 kilo-ohm resistors.
- Changed named net names in the schematic for UART0 TX and RX for appropriate routing to/from XDS110 debug IC.
- Added a 1 kilo-ohm pull-down resistor on VSEL_SD_SOC to prevent floating state input to buffer.
- Added buffer between SAFETY_ERRORn output and PMIC WD_DISABLE (GPIO6) to make sure the PMIC watchdog remains disabled without interference from the SoC until the entire power sequence is completed.
- Made the output enable logic of FT4232 UART buffers to be driven by the inverse of Resetstatz such that UART2 RX can only drive the BOOTMODE8 line when the device is out of reset.
- Replace eMMC chip (MTFC32GAZAQHD-IT) with the new alternate MTFC32GBCAQTC-AAT from Micron.
- Change net name of SoC_GPIO1_49 to SoC_GPIO0_38 and GPIO1_23_INTn to MCU_GPIO0_1_INTn to align with corresponding SoC instance names in GPIO mode.

5 References

5.1 Reference Documents

In addition to this document, the following references are available for download at www.ti.com.

- *AM275x Signal Processing Microcontrollers*
- *AM275x Signal Processing Microcontrollers Data Sheet*
- *AM275x Signal Processing Microcontrollers Technical Reference Manual*
- *Texas Instruments Code Composer Studio*
- *Updating XDS110 Firmware*

5.2 Other TI Components Used This Design

This EVM uses various other TI components for the functions. A consolidated list of these components with links to the TI product datasheets is shown below.

- *TPS65224-Q1 PMIC*
- *TPS746 Low Dropout Regulator*
- *TLV7589P Low Dropout Regulator*
- *TPS7A21-Q1 Low Dropout Regulator*
- *TPS22810 Load Switch*
- *TPS65988 Power Delivery Controller*
- *LM61460-Q1 Step-Down Converter*
- *TMUX154E 2:1 Analog Switch*
- *LMK6C LVCMOS Oscillator*
- *LMK1C1103 Clock Buffer*
- *TMC1294NCPDT XDS110 Controller*
- *TMP411 Temperature Sensor*
- *TAD5212 stereo audio DAC*
- *PCM6240 Audio ADC*
- *CDCE6214 Clock Generator*
- *TS5A3357-Q1 3:1 Analog Switch Multiplexer*
- *TPS22919 Load Switch*
- *TPS22918 Load Switch*
- *TPS62824 Load Switch*
- *TS3DDR3812 1:2 Switch Multiplexer*
- *TMUX1136 2:1 Analog Switch*
- *TXB0108 Voltage-Level Translator*
- *INA228 Current Monitor with I2C Interface*
- *TCAN1043A-Q1 CAN Transceiver*
- *TCA6424A I/O Expander*
- *SN74AVC8T245 Boot Buffer*

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (March 2025) to Revision C (June 2025)	Page
• Added note: Rev E2 of the AM275 EVM is the same as Rev A of the AM275 EVM	3

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NOTE:

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3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

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3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

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If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

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