Technical White Paper

The Impact of Lead Overhang on SMT for QFN Packages

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ABSTRACT

Wire bonded chip-on-lead QFN packages require a minimum amount of support of the die on the lead frame to maintain stable processing at wire bond. However, as die shrink with improved silicon capability, supporting smaller die sizes in existing package footprints has become more challenging. One support option is to extend the exposed metal of leads on the lead frame. However, the implications of this type of footprint change have not been evaluated for compatibility with existing PCBs. Therefore, this study assesses the potential impact on solder joint quality and reliability when leads overhang the land pads on a PCB in the SMT process.

During this study, a test vehicle was selected for the design of PCBs which simulate varying levels of lead overhang, and a representative sample of units were soldered onto each board. Measurements of the solder joint thickness were taken before subjecting the units to temperature cycling board-level reliability testing. Results show that up to 200µm of lead overhang can be supported with adequate solder joint formation, without concern on board-level performance. This adjustment can also allow for maintaining the same package designator in chip-on-lead QFN packages, which is important for customer continuity.

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Trademarks

1 Introduction

This study examines the potential impact to solder joint quality and solder joint reliability for leads overhanging the land pad on a PCB during the SMT process when the exposed metal of the lead is extended on a QFN package without changing the PCB. A chip-on-lead test vehicle was selected and PCBs designed to simulate varying levels of overhang were used. For each overhang amount, a representative sample size underwent temperature cycling board-level reliability testing to assess solder joint reliability. Data on the solder joint thickness and cross-sectional images of the solder joints were taken for quantitative and qualitative assessments of solder joint formation and performance when subjected to extended stress.

This type of assessment has not been previously performed for non-leaded packages. This study was prompted by a need to extend the exposed metal of leads for better die support in chip-on-lead QFN packages—changing the package footprint—while still maintaining a given package designator for customer continuity.

2 Background

Compared to standard wire bonded QFN packages, wire bonded chip-on-lead (COL) QFN packages enable pin counts to be supported in smaller package body sizes. A non-conductive die attach is used to isolate the die, which sits directly on the package leads, as shown in Figure 2-1.

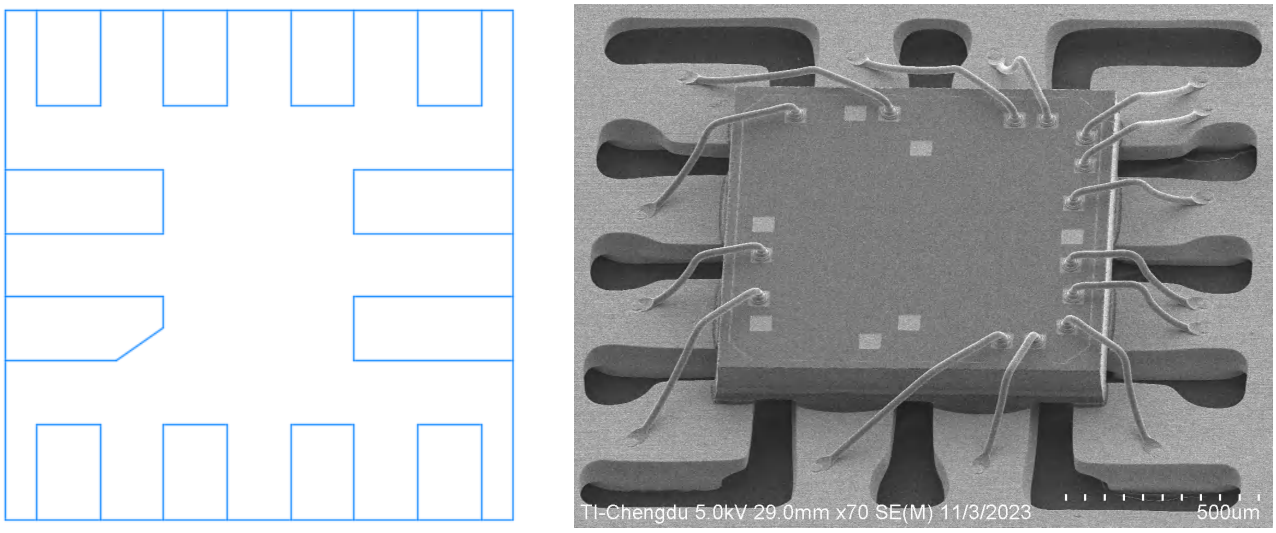

Figure 2-1. Example of a COL QFN Footprint (Left) and SEM Image of a COL Device Prior to Mold (Right)

The die must have adequate support on the leads to prevent failures during the wire bond process. These failures can include:

- Non-stick on the pad (NSOP), where the wire bond machine stops when the machine detects that the wire has not made correct contact with the bond pad.
- Malformed ball, where the ball bond is not well-formed.
- Low mean time between assists (MTBA), where the wire bond machine must be restarted frequently.

Thus, a minimum die size is necessary to wire bond based on the specific exposed lead dimensions and layout of a given COL QFN. However, as die shrink with improved silicon capability, the challenge of keeping the same package designator (needed for customer continuity) has increased.

To support smaller die in COL QFN packages, one option is to modify the lead frame and extend the exposed metal of the leads visible on the exterior of the package. This adjustment reduces the distance between leads, meaning, a smaller die can be supported between the leads. However, the implications of this type of change to the package footprint on SMT (when a customer solders the package to their PCB) has not been previously evaluated.

Unless new boards are designed, the extended leads overhang an existing PCB land pad to some extent, as visualized in Figure 2-2. However, a new PCB design is time-consuming and expensive, so reusing an existing PCB and stencil without concern for impacts to SMT (for example, solder joint abnormalities or solder volume thickness) is desirable for customers. Temperature cycle board-level reliability (BLR) testing was chosen as the assessment method to evaluate the effects on solder joint reliability and fatigue when the leads are extended and soldered without changing the PCB.

Figure 2-2. Concept of Lead Overhang

In terms of the amount of overhang that is permissible, a maximum of 25% of side overhang is recommended (along the lead width) for robustness, but makes no comment regarding overhang along the lead length; the only guidance comes from IPC-A-610 [1].

3 Procedure

A 16-pin WQFN package was selected as the test vehicle. The 16-pin WQFN package includes preplated NiPdAu leads, nominally dimensioned at 0.2mm in width and 0.6mm in length, with a 0.4mm pitch (see dimensioned footprint in Figure 3-1). First, daisy-chain units with a die resulting in a die-area-to-package-area ratio of 42% were assembled for in situ event monitoring.

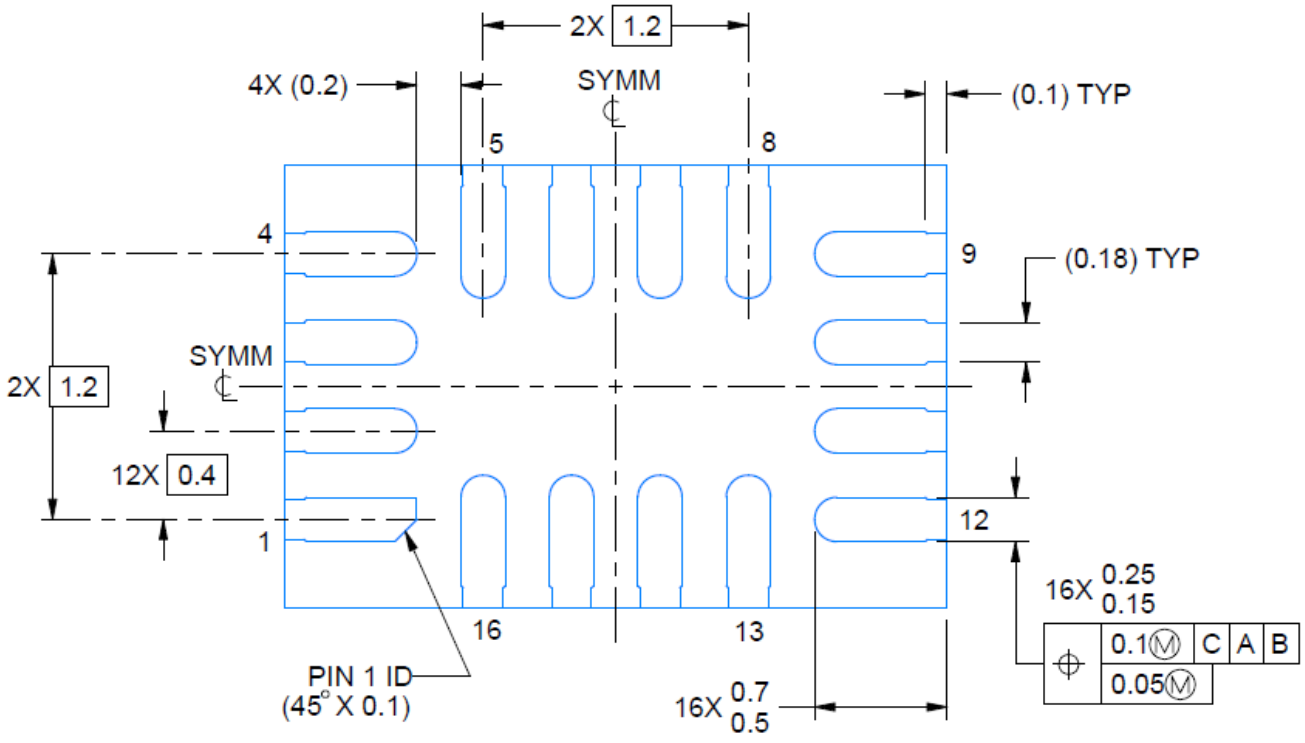

Figure 3-1. Test Vehicle Footprint

Next, two sets of PCBs were designed for the test vehicle. The first PCB was designed to be 1.6mm-thick with eight metal layers and with leads that overhang the PCB land pads by 100µm. The second PCB was designed to be 1.6mm-thick with eight metal layers and with leads that overhang the PCB land pads by 200µm (visualized from the top in Figure 3-2). The assembled units were then soldered onto the PCBs using SAC305 in two configurations:

- Configuration 1: Only two sides are soldered (on the west and east) to simulate a SON configuration
- Configuration 2: All four sides are soldered as is typical of a QFN configuration

A sample of the units with only the two sides soldered had optical exterior images taken, along with cross-section images of the soldered leads and measurements of the solder joint thickness prior to starting any testing.

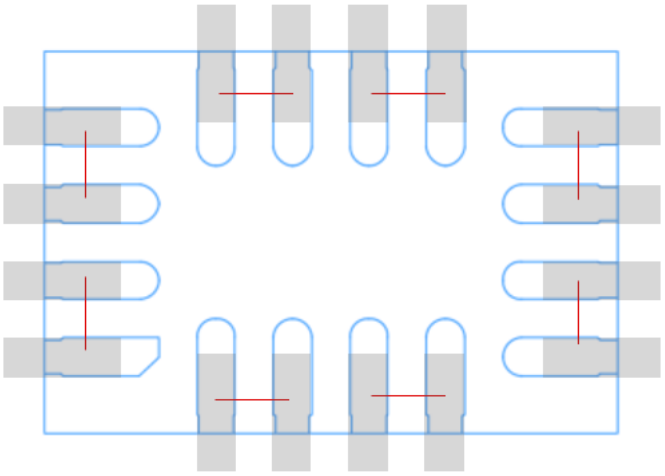

Figure 3-2. Leads Overhanging Land Pads (in Gray) and Daisy-Chain Connections (in Red) Shown With Test Vehicle Footprint (in Blue)

Thirty-two units with four sides soldered on each PCB set (100µm overhang and 200µm overhang) then underwent temperature cycling according to the JEDEC standard, JESD22-A104D. The chosen temperature profile took the units between –40 and +125 C over the course of a 60-minute cycle, common in automotive applications [2, 3].

An additional twenty-four units on each PCB set that had only the two sides soldered also underwent the same temperature cycling profile but were not monitored for continuity. After 1000 cycles, eight units were removed. Cross-section images of the soldered leads and measurements of the solder joint thickness of these units were taken for comparison to the units prior to starting the BLR test. This was repeated for eight additional units removed after 2000 cycles and eight additional units removed after 3000 cycles.

A summary of the evaluation splits is provided in Table 3-1 and Table 3-2.

Table 3-1. Summary of Evaluation Done on the Units With All Four Sides Soldered

Overhang Amount	Test
100µm	BLR, in situ monitoring – 32 units
200µm	BLR, in situ monitoring – 32 units

Table 3-2. Summary of Evaluation Done on the Units With Two Sides Soldered

Overhang Amount	Test	Pull-Out Cycles
100µm	None	8 units – 0 cycles
	BLR, without in situ monitoring – 24 units	8 units – 1000 cycles
		8 units – 2000 cycles
		8 units – 3000 cycles
200µm	None	8 units – 0 cycles
	BLR, without in situ monitoring – 24 units	8 units – 1000 cycles
		8 units – 2000 cycles
		8 units – 3000 cycles

For reference, a BLR temperature cycle test without overhang using the same test vehicle was previously conducted. This previous test had no electrical failure even after 9740 cycles. Figure 3-3 pictures a cross-section of the corner leads after the completion of this previous test. The cracking seen in the solder joints is due to the extent of testing but demonstrates the integrity of the solder joint in this *base case* when the overhang is not present.

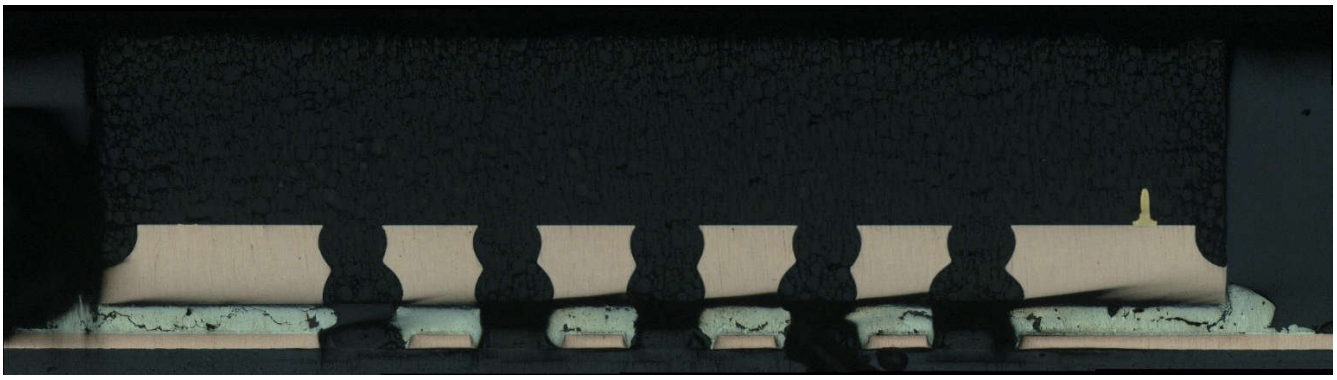

Figure 3-3. Cross Sections of Leads Soldered Without Overhang After Nearly 10000 Cycles of BLR

4 Assessment Methods and Results

4.1 Initial Data Collection

After being soldered to PCBs, three of the units in the SON style of configuration were cross-sectioned to measure the solder joint thickness and SEM images were taken to examine the solder fillet formation. The solder joint measurements are summarized in Figure 4-1. All the solder joint thickness values for a given unit averaged 50µm or greater, which is in line with guidance from IPC-7351 on preferable and reliable solder joint thickness [4].

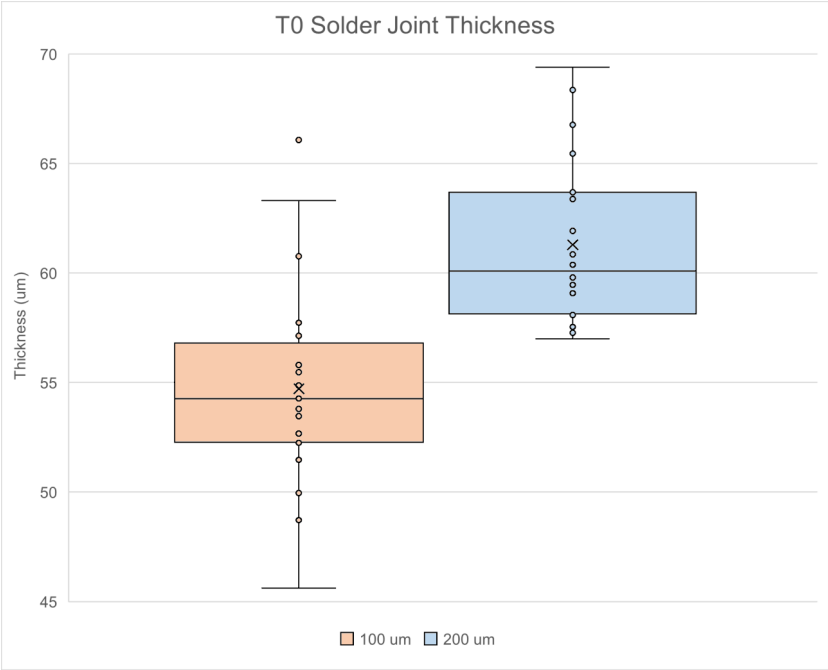

Figure 4-1. T0 Solder Joint Measurements of Units In the SON Style of Configuration Without Any Stress Testing

The solder joints in Figure 4-2 and Figure 4-3 show no anomalies and are representative cross-sectional images for 100µm and 200µm overhangs.

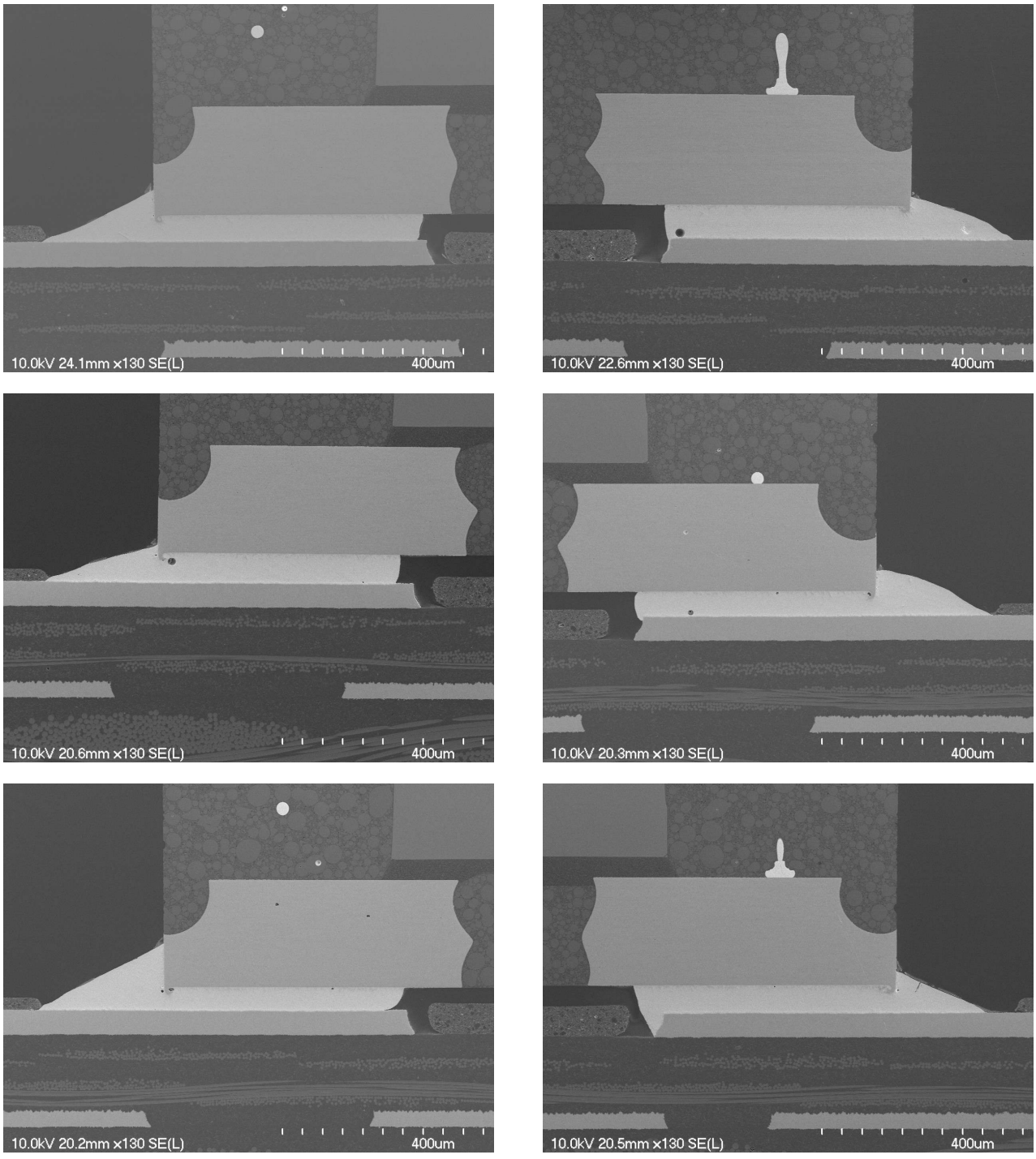

Figure 4-2. Cross Sections of Leads Soldered With a 100µm Overhang Without Any Stress Testing

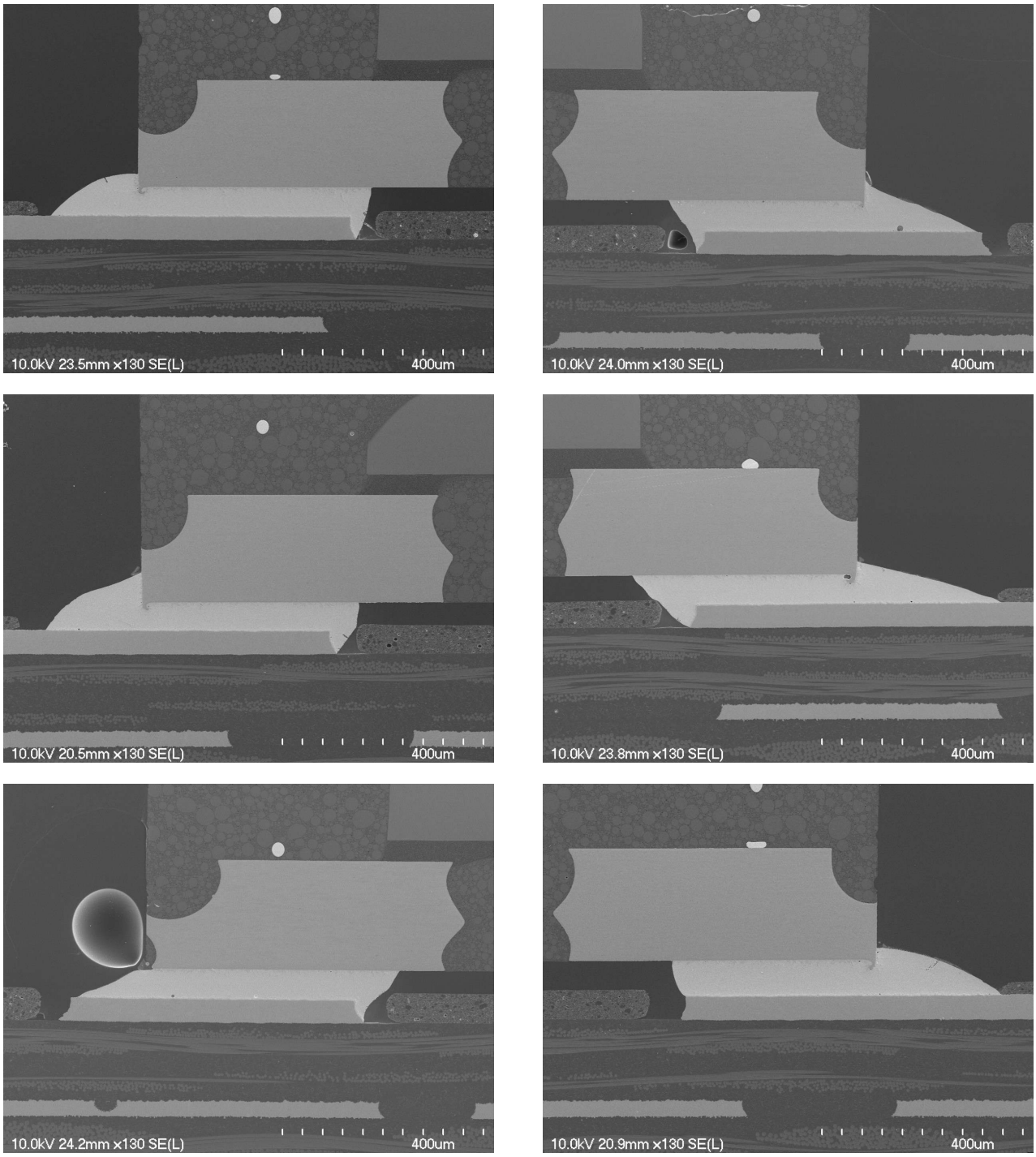

Figure 4-3. Cross Sections of Leads Soldered With a 200µm Overhang Without Any Stress Testing

Partial fillets and low to no side-wetting angles were commonly seen in the solder joints. However, these appearances do not necessarily indicate inferior performance. More information on this concept is discussed in the following section where board-level reliability is assessed.

4.2 BLR With In Situ Monitoring

Units that were soldered on all four sides underwent temperature cycling and were monitored for event detection. In general, board-level reliability testing is an accelerated test, which can be used to correlate the actual field life of solder joints with test performance based on acceleration factors dependent on the device application. According to IPC-9701A (which provides guidance on temperature cycle testing), the requirement is that a minimum of 1000 cycles must pass without electrical failure for acceptance [3]. The units in this study showed no failure even after 6870 cycles for both the 100µm and 200µm overhang, suggesting good board-level reliability.

4.3 BLR Without In Situ Monitoring

Additional units that were soldered on only two sides were subject to temperature cycling, but were not monitored for event detection. Instead, after 1000 cycles, eight units were removed. Cross-section images of the soldered leads and measurements of the solder joint thickness of these units were taken for comparison to the units prior to starting the BLR test. This was repeated for eight additional units removed after 2000 cycles and eight additional units removed after 3000 cycles. Again, all solder joint thickness values for a given unit averaged 50µm or greater. Gross abnormalities or stresses in the individual solder joints were not witnessed. Voiding and cracking is more visible in the units after 3000 cycles of BLR, which is expected as the units have undergone more stress, but this damage is not expected to lead to an electrical or mechanical failure.

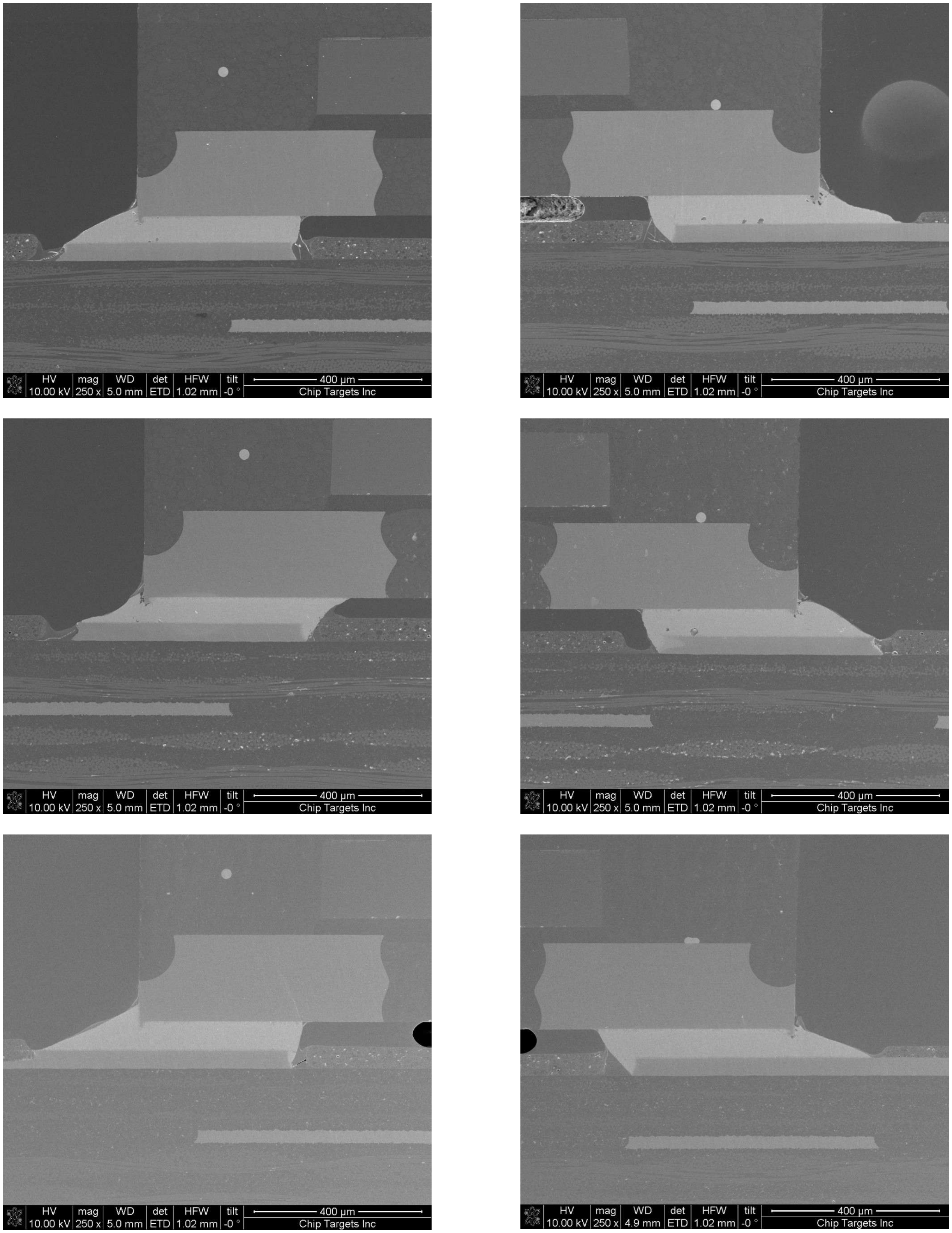

Figure 4-4. Cross Sections of Leads Soldered With a 200µm Overhang After 1000 Cycles of BLR

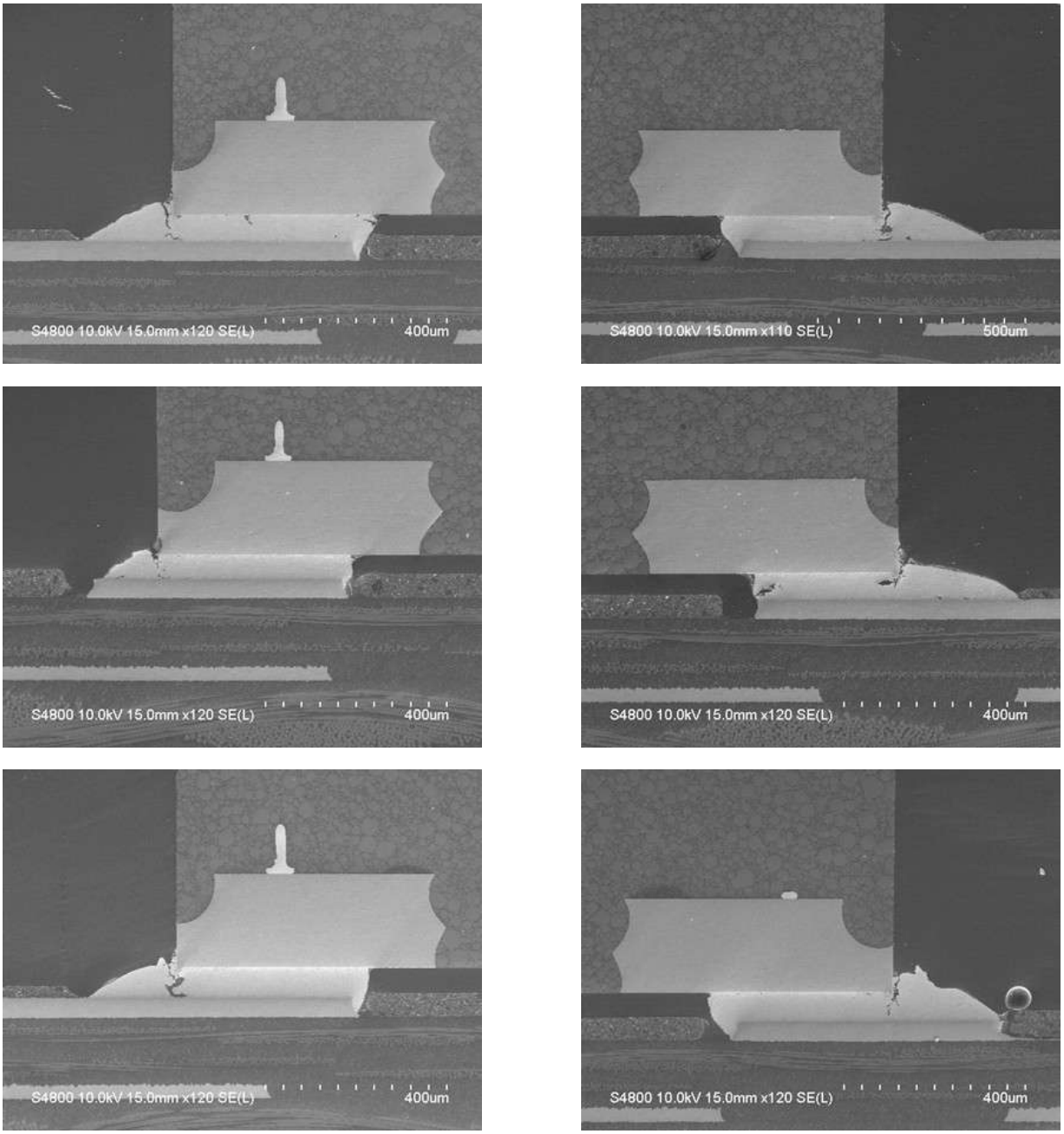

Figure 4-5. Cross Sections of Leads Soldered With a 200µm Overhang After 3000 Cycles of BLR

5 Summary of Results

- Measurements of the solder joint thicknesses at T0 were acceptable for both the 100µm and 200µm overhang units.
- Cross-section images of the units on the PCBs showed partial fillets and low to no side-wetting angles for both the 100µm and 200µm overhang.
- All units for both the 100µm and 200µm overhang passed temperature cycle BLR testing well beyond 1000 cycles without failure.
- Gross anomalies were not witnessed in the solder joint fillets, even after 3000 cycles of temperature cycle BLR testing, for the 200µm overhang. Voiding and cracking is not expected to cause an electrical or mechanical failure.

6 Conclusion

The T0 solder joint measurements and cross-section images in this study demonstrate that leads overhanging the land pattern of a PCB do not result in an impact to solder joint reliability and solder joint quality in the SMT process for leads. This conclusion is further supported by the results of board-level reliability testing; where no failures were recorded in testing well beyond 1000 cycles, and the cross-sections of the stressed units did not show abnormalities. Based on these results, customers can consider a change in the lead length of the package footprint up to 200µm without impacting compatibility with existing PCBs.

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- Peter Nguyen of *Chip Targets Inc*, Dallas, for package imaging and solder joint measurements.

8 References

1. IPC-A-610E-2010, *Acceptability of Electronic Assemblies,* April 2010.
2. JESD22-A104D, *Temperature Cycling*, March 2009.
3. IPC-9701A, *Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments*, February 2006.
4. IPC-7351, *Generic Requirements for Surface Mount Design and Land Pattern Standard*, February 2005.

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