TI Designs

Current Sensing With <1-µs Settling for 1-, 2-, and 3-Shunt FOC Inverter Reference Design

Description

The TIDA-00778 design demonstrates fast and accurate current sensing for a three-phase motor driven with sensorless field-oriented control (FOC). Drives with lower audible noise require faster and accurate current sensing. The most common low-cost current-sensing methods use a single shunt on the DC bus return path or two to three shunts in the inverter legs. The major challenge in motor control is to enable accurate current sensing even with the lowest active vector duration. TIDA-00778 demonstrates sub-microsecond settling and accurate current sensing in such scenarios. The reference design is applicable to major appliances, especially in compressor motors, and the inverter power stage can work up to 2 kW.

Resources

TIDA-00778	Design Folder
OPA835	Product Folder
INA303	Product Folder
UCC27714	Product Folder
TMS320F28027	Product Folder
TLV1701	Product Folder
TLV6001	Product Folder
TLV704	Product Folder

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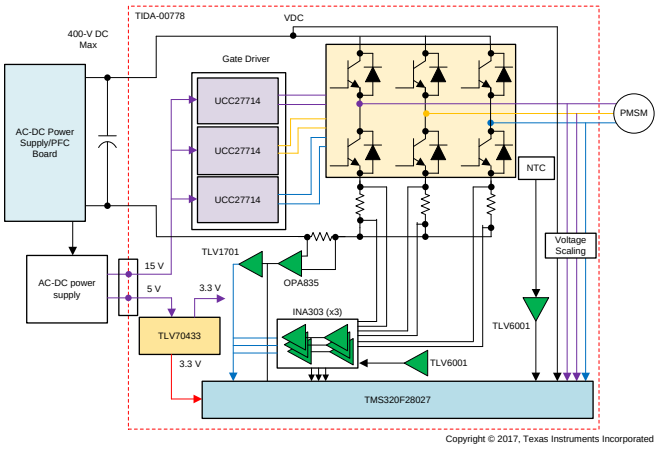
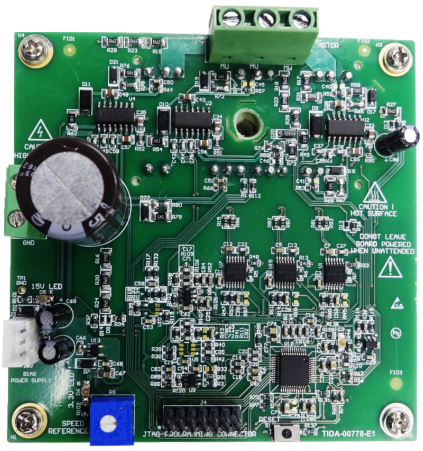
Features

- Fast and Accurate Current Sensing for Sensorless FOC With Single-, Dual-, and Triple-Shunt Topologies to Minimize Torque Ripple and Audible Noise in Motor Drives
- Single-Shunt Current Sensing With Minimum Settling Time and Gate Driver With Lowest Propagation Delay Enable Active Voltage Vector Duration < 1 µs
- Single-Shunt DC Bus Current Sensing With < 0.15% Calibrated Accuracy
- Dual- and Triple-Shunt Current Sensing With < 1.5-µs Settling Time and < 0.04% Calibrated Accuracy Enabling Accurate Current Sensing at Extreme Duty Cycles
- Overcurrent Detection With Response Time < 1.5 µs
- Input Voltage 270-V to 390-V DC (Rectified From 195-V to 265-V AC)
- Protection Features: Motor Overcurrent and Overtemperature

Applications

- Air Conditioners
- Washing Machines
- Refrigerators





1 System Overview

1.1 System Description

Fast and precise current sensing is required in motor control applications to have the minimum torque ripple and thus minimum audible noise. Accurate current sensing is also important to have the best dynamic motor control. The delay in a current sensing can lead to incorrect current estimates and hence distorted current waveform in a motor. The motor drive applications in major appliances such as a compressor motor control in air conditioners and refrigerators require accurate torque control to have the best dynamic performance and low acoustic. An inaccurate current sensing leads to distorted current waveform in the motor winding and thus produces torque ripple, which, in turn, results in inefficient and noisy performance.

The most common motors used in compressor motor drives include a single-phase or three-phase induction motor, a three-phase brushless DC (BLDC) motor or permanent-magnet synchronous motor (PMSM), an interior permanent magnet motor, or so forth. The three-phase motor uses a three-phase inverter to control the motor and meet the dynamic torque requirement in compressor motors with high efficiency.

Control of the inverter system, and thereby the compressor motor drive system, requires knowing the motor current information. For a three-phase motor, the designer must know all the phase currents to be able to control the motor torque. The motor-phase winding current can be sensed by using different methods, for which the commonly-used methods are:

- Inline current sensing
- Inverter leg current sensing
- DC bus current sensing using a single shunt

Figure 1 shows the placement of current sensor in the previously-mentioned sensing methods.

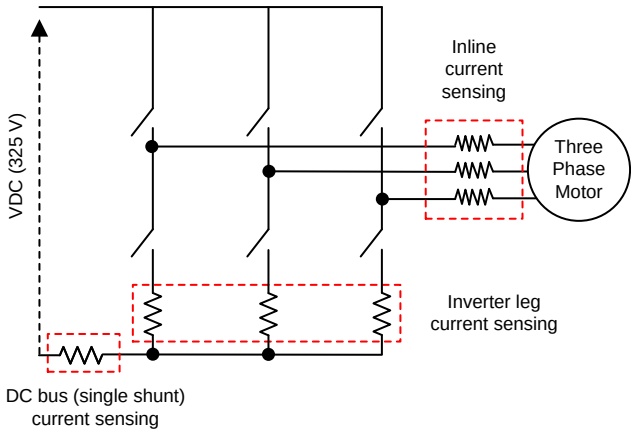


Figure 1. Different Current Sensing Methods Used in Three-Phase Inverter

The simplest method of obtaining motor winding current is by measuring each of phases current directly at the phase node by placing a current sensor in line with the phase connection. Depending on the motor winding connections, this measurement requires at least two sensors to be applied directly to the individual motor phases. The common-mode voltage existing in the in-line sensing is equal to the DC bus voltage, which makes non-isolated shunt-based sensing difficult. Isolated sensors are normally used in these lines and are usually sophisticated and expensive. Use of a non-isolated shunt-based solution is preferable in applications where the common-mode voltage is typically less than 100 V.

Another method is to measure the inverter leg currents as Figure 1 shows. In this case, the common-mode voltage is close to zero and a low-cost shunt and an operational amplifier (op amp) can be used to sense the inverter current. The current sampling has to be done when the low-side switch is ON and the current sampling point must be synchronized with the pulse-width modulation (PWM). The ideal method is to use three-leg inverter current sensing. Two-leg inverter current sensing must be performed at the minimum to obtain accurate information on each of the three winding currents.

Another method, which is more complex, is to measure only the DC line current and then identify each of the three-phase currents sequentially in the different inverter switching states. Because the switching state of the inverter is controlled by the digital signal processor (DSP), the designer can determine the exact electrical route taken by the input current through the inverter, which allows the designer to directly relate the DC bus currents to the motor phase current. The phase currents obtained are the result of a real measurement of the current and are not the result of a simulation that requires a model of the circuit.

The field-oriented control (FOC) is commonly used in compressor invertor drives to obtain better dynamic performance. The FOC uses space vector modulation (SVM) to switch the inverter. The TIDA-00778 evaluates the single-, dual- and three-shunt current sensing. The TIDA-00778 shows fast and accurate current sensing for a three-phase, sensorless, FOC-driven motor.

Section 1.1.1 provides a detailed analysis of the different types of low-side current sensing performed.

1.1.1 Low-Side Current Sensing Topologies

The low-side current-sensing topologies use a resistor located at the base of the phase or at the DC bus return path to measure current that is flowing through a phase. Regardless of the resistor configuration used (one-, two-, or three-shunt), current can only be measured when a lower switch is ON. The current signal must be clean to properly sample the current. A clean current signal or representation of the current signal must have no ringing or noise. The following subsections detail different current measuring techniques for resistor shunts that are used in the field.

1.1.1.1 Three-Shunt Current Sensing

Figure 2 shows three-shunt inverter leg current sensing. Three-shunt current sensing has some advantages. Contrary to the three-shunt technique, the use of a single- or two-shunt setup proves difficult to achieve circuit overmodulation. Additionally, the use of a low-bandwidth op amp is sufficient. The three-shunt technique can bounce sampling between current signals, selecting two out of three phases each period, which allows long time periods for the current signals to settle. If large current measurement windows are possible, then much slower and cheaper op amps can be used. For example, Figure 3 shows three PWM switching signals and the corresponding shunt resistor to be sampled. As the Figure 3 shows, the current signal has plenty of time to stabilize.

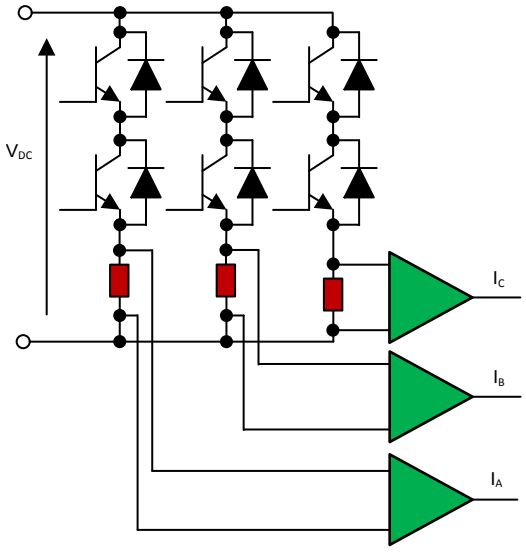


Figure 2. Three-Shunt Current Measurement Circuit With Inverter

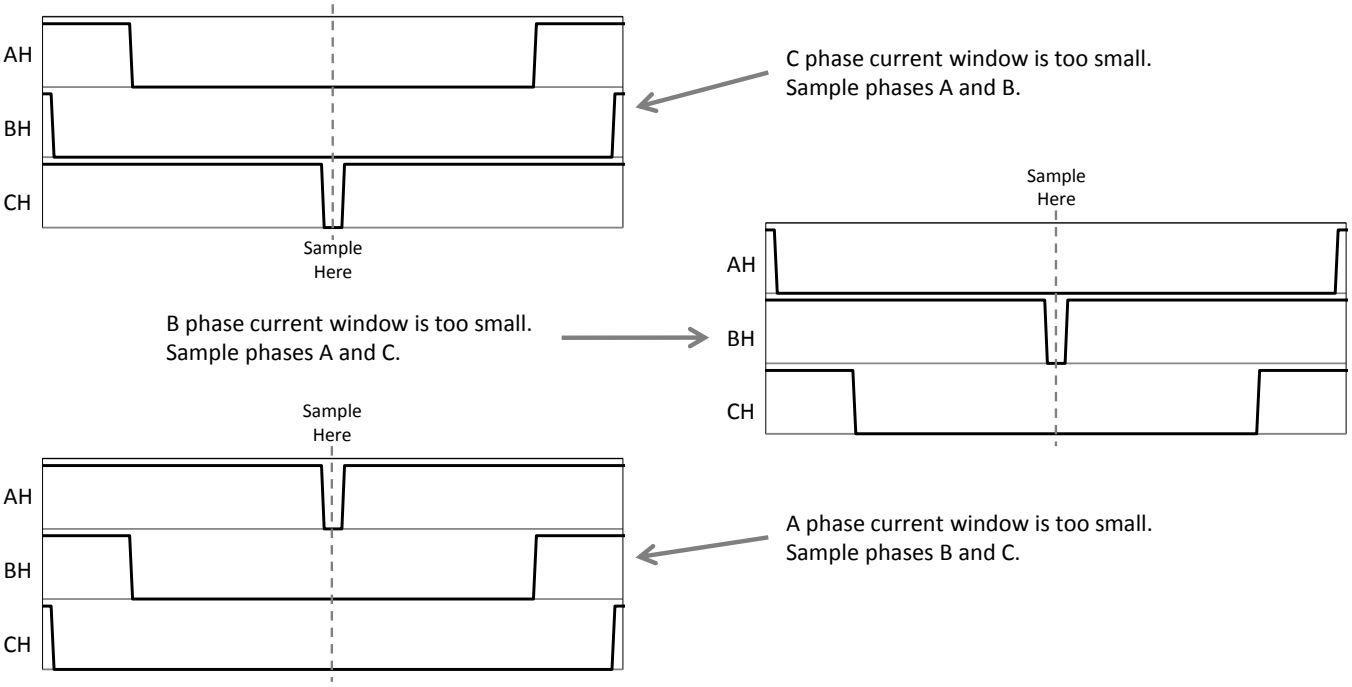


Figure 3. Using Three-Shunt Current Sampling Technique

1.1.1.2 Dual-Shunt Current Sensing

The two-shunt current measurement technique uses the principle of Kirchhoff's current law (KCL), which is that the sum of the currents into a single node equals zero. By measuring only two-phase currents, the third is calculated with KCL. Figure 4 shows a circuit for the two-shunt current measurement technique.

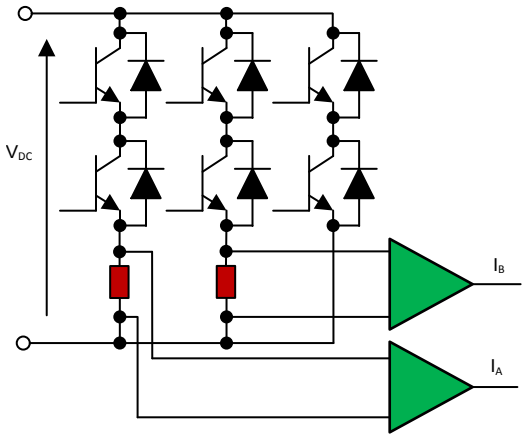


Figure 4. Dual-Shunt Current Measurement Circuit With Inverter

The two- and three-shunt measurement circuit has an advantage over the single-shunt circuit in that it can detect circulating currents. Figure 5 shows an example of a switching waveform and where the analog-to-digital converter (ADC) samples the current. The PWM duty cycle for I_A is almost 100% in this example, which causes the I_A current to rise. The PWM for I_B is about 50% duty cycle and its current stays at approximately 0 A for this period. Phase current can only be measured when the lower switch of that particular phase is conducting. In the example, I_A is measurable for a very short time while I_B has a long time to measure. The inherent problem of using the two-shunt technique is when the measured phase is operating at PWMs near 100%. For example, when sampling I_A, the measured current signal has not yet stabilized, which gives an incorrect representation of the current signal.

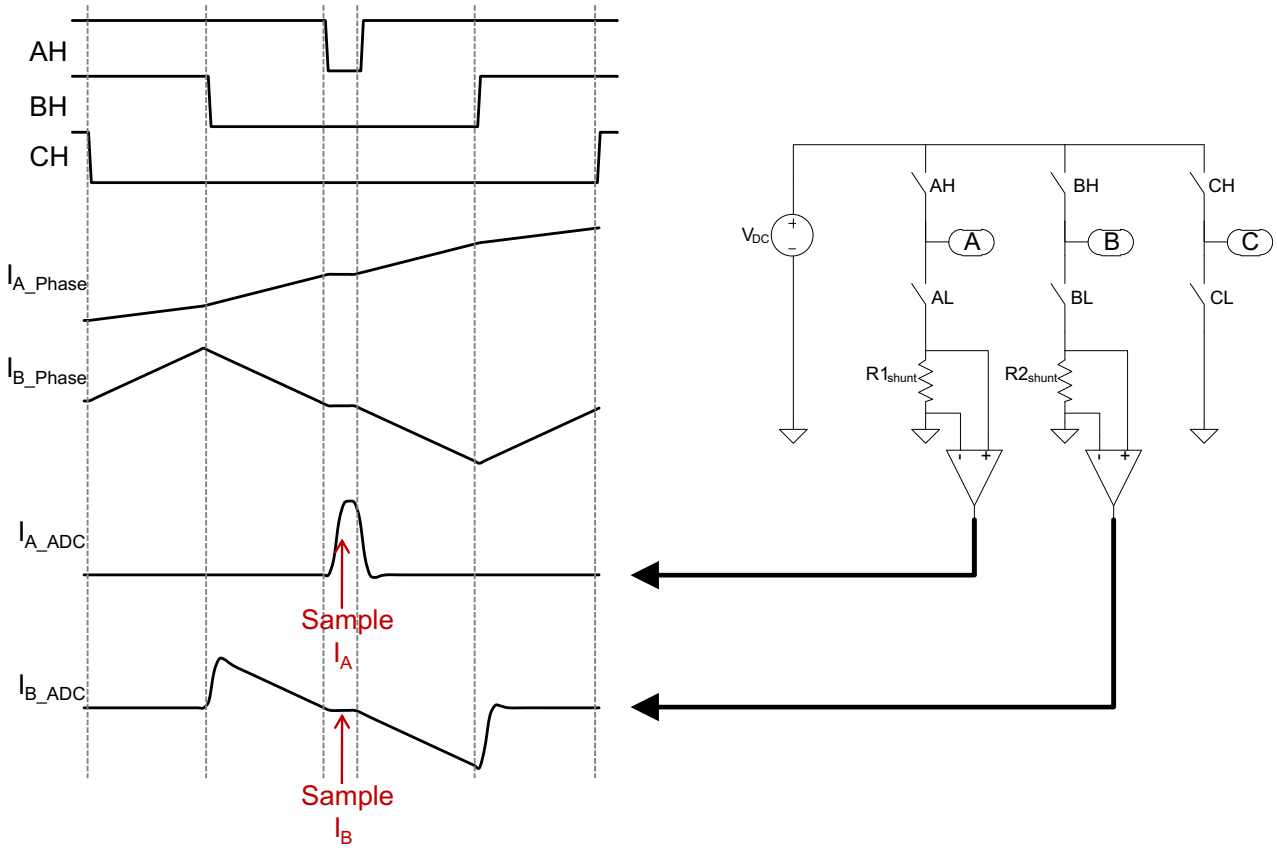


Figure 5. Sampling Current When Using Two-Shunt Measurement Technique

As the duty cycle increases, the time to measure voltage across the shunt resistor for the phase decreases and the current measurement must be quicker. As the duty cycle increases even more, the slew rate must be increased to properly capture the signal. Although the two-shunt current measurement technique lessens the speed requirement of the op amp as compared to the single-shunt measurement, there is a duty cycle where the slew rate has to be very large, but still less than the requirement for a single shunt.

For two- and three-shunt techniques, the current being measured is bipolar. So, 0 A is now represented as half of the ADC full scale and the quantization step size doubles.

1.1.1.3 Single-Shunt Current Sensing

The single-shunt current measurement technique measures the power supply current and, with knowledge of the switching states, recreates each of the three-phase currents of the motor. Figure 6 shows the single-shunt location in the inverter circuit.

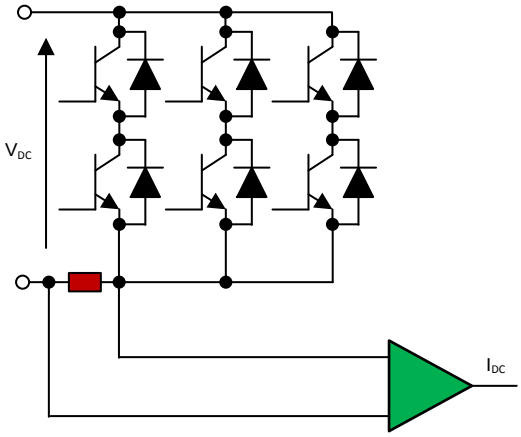


Figure 6. Single-Shunt Current Measurement Circuit With Inverter

For a better understanding of the measurement process and to represent the switching state of the inverter, this reference design defines a switching function Sa for phase A as follows: Sa = 1 when the upper transistor of phase A is ON, and Sa = 0 when the lower transistor of phase A is ON. Similar definitions can be made for phases B and C.

The explanation of the process is based on the assumption that the inverter is fed in complementary mode. The signals in this mode, which control the lower transistors, are the opposite of Sa, Sb, and Sc, which control the upper transistors.

As previously stated, the measurement method in single-shunt current sensing depends on the switching states of the inverter switches. An example case is explained in Figure 7 and Figure 8. In Figure 7, the top-side switch of phase A is conducting and the bottom-side switches of phase B and C are conducting. In this switching state, the DC bus current measurement gives the phase A current and is positive ($+I_A$). The direction of current in phase A is toward the motor winding (see Figure 7).

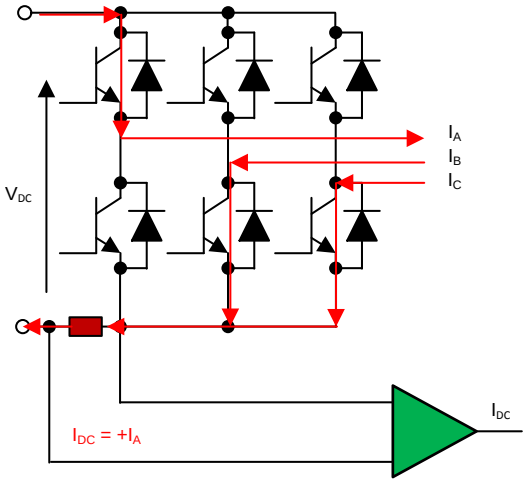


Figure 7. Switching State Sa, Sb, Sc: 100

In Figure 8, the top-side switches of phase A and phase B are conducting and the bottom-side switch of phase C is conducting. In this switching state, the DC bus current measurement gives the phase-C current and is negative ($-I_C$). The direction of current in phase C is toward the inverter from the motor winding (see Figure 8).

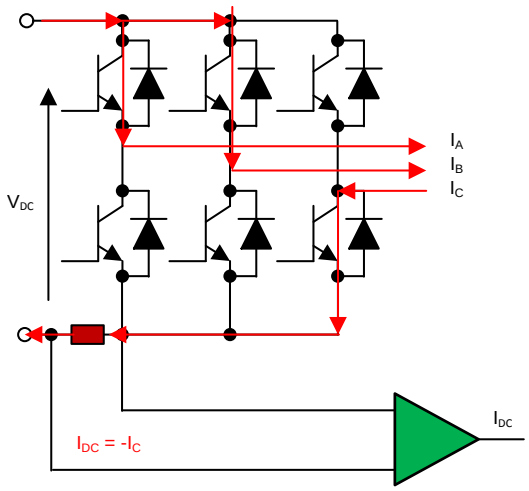


Figure 8. Switching State Sa, Sb, Sc: 100

Similar to the preceding explanation, there are eight different switching options in SVM PWM. Table 1 explains the switches conducting in each space vector switching state and which phase current can be measured in that state. With the switches in states 0 and 7, only circulating current is present and measuring current with the single-shunt technique is impossible. The six switching states from 1 to 6 are known as active vector or active voltage vector. The current measurement and switching state must both be considered to properly measure current with the single-shunt technique.

Table 1. SVM Switching States

SWITCH STATE	AH	BH	CH	MEASURE
0	0	0	0	Offsets
1	1	0	0	I_A
2	1	1	0	$-I_C$
3	0	1	0	I_B
4	0	1	1	$-I_A$
5	0	0	1	I_C
6	1	0	1	$-I_B$
7	1	1	1	Offsets

Figure 9 shows an SVM PWM waveform and the DC bus current measurement signal that resulted from the applied switching state. In this case the current conduction times for each switching state are long enough to allow enough time for the whole measurement system to settle and for the ADC to have enough time to sample the current.

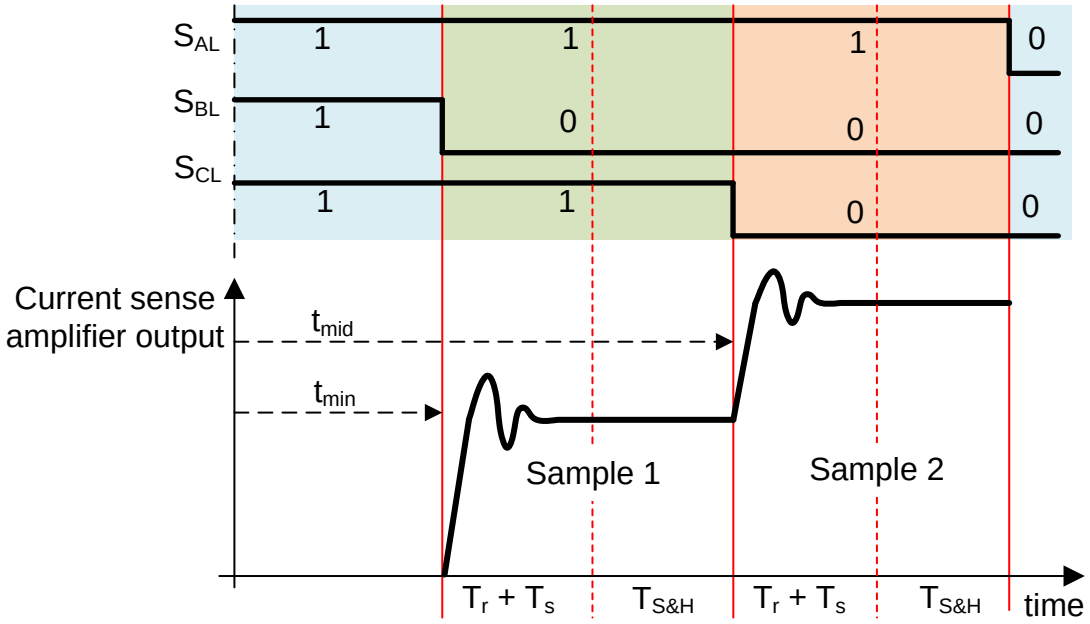


Figure 9. Single-Shunt Current Measurement When Sampling Times Are Sufficient

When using the single-shunt technique, the ability to measure current in the least amount of time possible is mandatory. This requirement highlights the importance of ensuring that the minimum pulse width (minimum active vector duration) and pulse transition period are maintained for a valid sample. Understanding the delays in the measurement is necessary to understand the minimum vector duration required. Figure 10 shows the delay components in the measurement path.

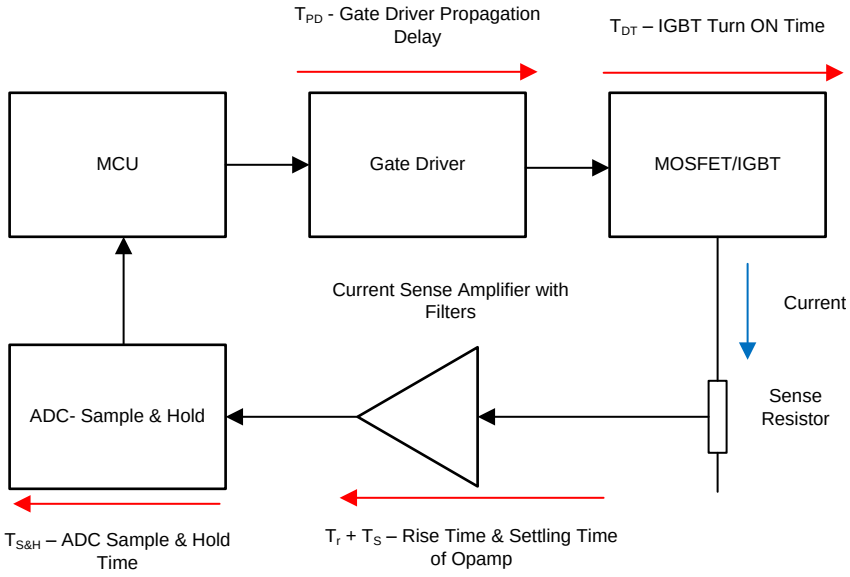


Figure 10. Delay in Current Censing Loop

The minimum active vector duration must be more than the total delay in the current sensing path. From Figure 10, use Equation 1 to determine the minimum active vector duration to derive a valid current sample.

$$t_{av\_dur} > T_r + T_s + T_{S\&H} + T_{PD} + T_{DT} \quad (1)$$

where,

- T_r = Rise time of amplifier (dependent on the amplifier slew rate)
- T_s = Settling time of amplifier (dependent on amplifier GBW, gain, accuracy, and sensing circuit filters)
- T_{PD} = Gate driver propagation delay
- $T_{S\&H}$ = Sample and hold time (ADC)
- T_{DT} = Insulated-gate bipolar transistor (IGBT) turnon time – dead time.

Ideally, to have an undistorted current in the motor winding, the minimum active vector duration would be zero. Having a minimum active vector duration of zero is difficult to achieve practically because of the sensing and loop delay. A non-zero, minimum-vector duration creates distortion in the current waveform, unless it is compensated in the software algorithm (which is very complex and difficult to achieve). Figure 11 shows the space vector hexagon. As the space vector points toward the corners of the hexagon, the time window for sampling current completely disappears. There are zones located at 0º, 60º, 120º, 180º, 240º, and 300º where only one current can be measured and the other two currents must be found in another fashion. Refer to the *Space-Vector PWM With TMS320C24x/F24x Using Hardware and Software Determined Switching Patterns* application report for a detailed study on the space-vector PWM technique[3].

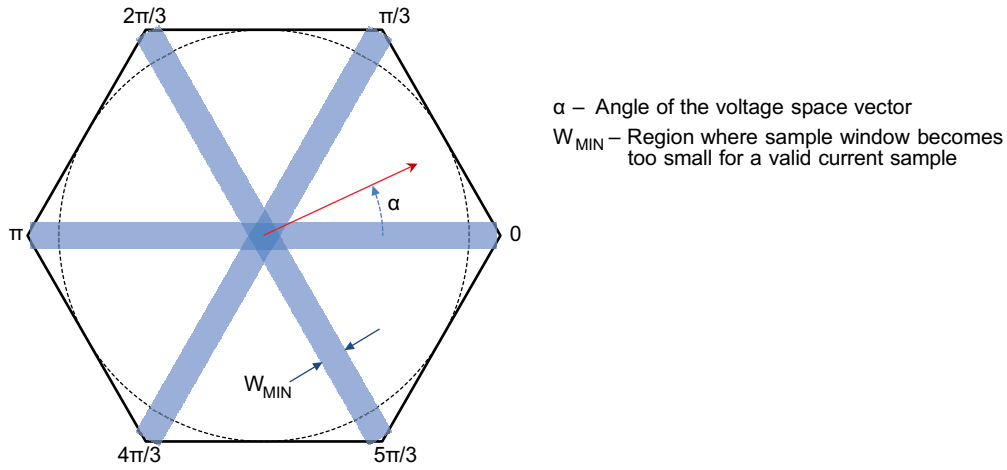


Figure 11. SVM and Regions Where Current Measurement is Not Allowed

Figure 12 and Figure 13 show the active vector durations (U1 and U2) during zero-crossing and 60º sector changes. In Figure 12, the sector duration U1 is too small to have a valid sample. In Figure 13, the sector durations of U1 and U2 are too small to have a valid sample of current.

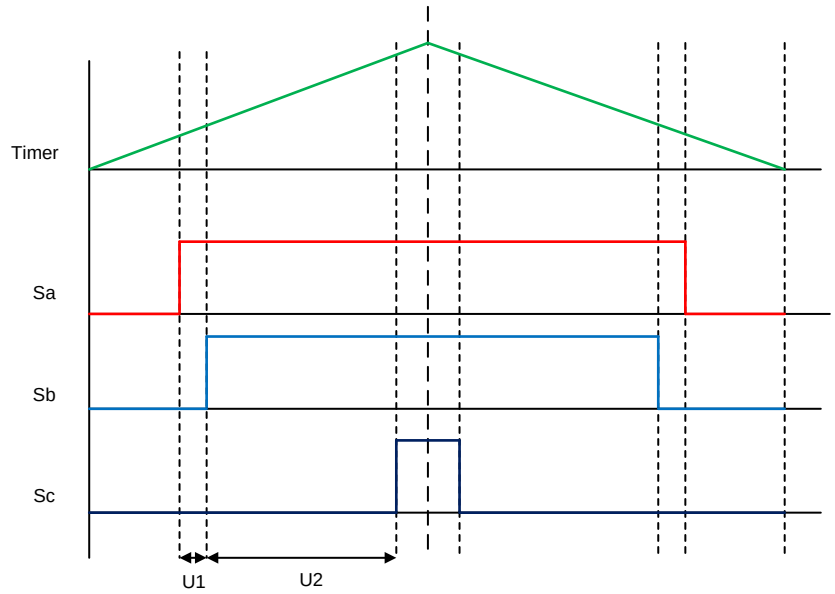


Figure 12. Active Vector Durations During 60º Sector Changes

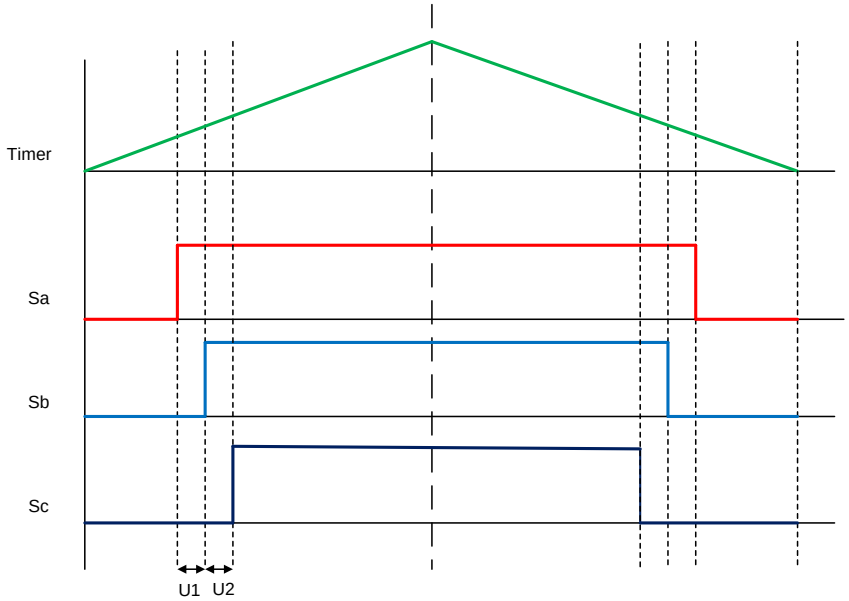


Figure 13. Active Vector Durations During Zero Crossing

Designers ideally prefer to have an accurate and fast-settling current sensing to enable the very minimum active vector duration, which offers the following advantages:

- Reduces the current sensing complexity and hence reduces actual current distortion at zero-crossing and sector changes (every 60° interval)
- Reduces the software overhead in determining the winding currents during the lower active vector duration; the software algorithm may use mathematical prediction or PWM phase advancing or delaying in such scenarios.

To achieve very minimum vector duration requires reducing the overall delay in the current sensing path. This task can be achieved by using a fast current sensing (using a fast amplifier), using a gate driver with minimum propagation delay, using minimum sample and hold time, and by optimizing the dead time.

The TIDA-00778 reference design shows the single-shunt current sensing using OPA835 (which has a GBW of 56 MHz) to sense the DC bus current, which enables fast ramp-up and settling time. The UCC27714 gate driver is used to have the minimum propagation delay. The fast current sensing circuit allows the designer to achieve a minimum active vector duration as low as 1 µs, as given in Equation 2.

$$T_r + T_s + T_{PD} < 1\,\mu s \quad (2)$$

NOTE: The S&H time of the ADC (TIDA-00778 uses the successive-approximation register (SAR) ADC of TMS320F28027) is much lower (a couple of clock cycles of the MCU) compared to other delays. The dead time depends on the IGBT turnon and turnoff time and depends on the selected switching device. The effect of dead time can be easily compensated using an algorithm. The gate driver propagation delay and delay mismatch is difficult to compensate and must be considered while defining the minimum active vector duration.

1.2 Key System Specifications

Table 2 shows key parameters considered in the design of TIDA-00778.

Table 2. Key System Specifications

PARAMETER	SPECIFICATIONS	DETAILS
Input voltage	270- to 390-V DC	The DC voltage derived from the 195- to 265-V AC input with and without power factor correction
Maximum output power	2 kW	The IGBT module is selected to support a maximum 2 kW
RMS winding current	5.58 A	At 325-V DC delivering 2 kW at a power factor of 0.9 with space vector PWM
Peak winding current	7.89 A	At 325-V DC delivering 2 kW at a power factor of 0.9 with space vector PWM
Control method	Sensorless FOC	Designed to support InstaSPIN-FOC™ solution
Inverter switching frequency	15 kHz (adjustable from 5 k to 20 k)	Selection based on the motor inductance and desired current ripple
Feedback signals	DC bus voltage, three winding voltages, inverter leg currents, DC bus return current	The feedback signals are required for sensorless control
Current shunt resistors used	10-mΩ shunt for DC bus current sensing using OPA835 5-mΩ shunt and INA303 in inverter leg current sensing	See Section 1.4.2 for design aspects
Inverter leg current sensing maximum range	±16.5 A	Scaled to 0 V to 3.3 V, level-shifted with 1.65-V bias
DC bus current sensing maximum range	13.2 A	Scaled to 0 V to 3.3 V, with 0-V bias; the design has an option to use 1.65-V bias
Inverter leg current sensing accuracy (calibrated)	< 0.04%	See Section 2.2.2.9 for the accuracy measurement
DC bus current sensing accuracy (calibrated)	< 0.15%	See Section 2.2.2.6 for the accuracy measurement
Protections	Overcurrent, overtemperature	See Section 2.2.2.10 for the overcurrent protection measurement
Cooling	With external heat sink	—
Operating ambient	–20°C to 85°C	—
Board specification	95 mm × 95 mm, two-layer, 1-oz copper	—
15-V supply current for gate driver	50 mA (max)	See Section 1.4.3.1 for the power requirement in gate driver
5-V and 3.3-V supply current	300 mA	The 3.3 V is used for the MCU and amplifiers

1.3 Block Diagram

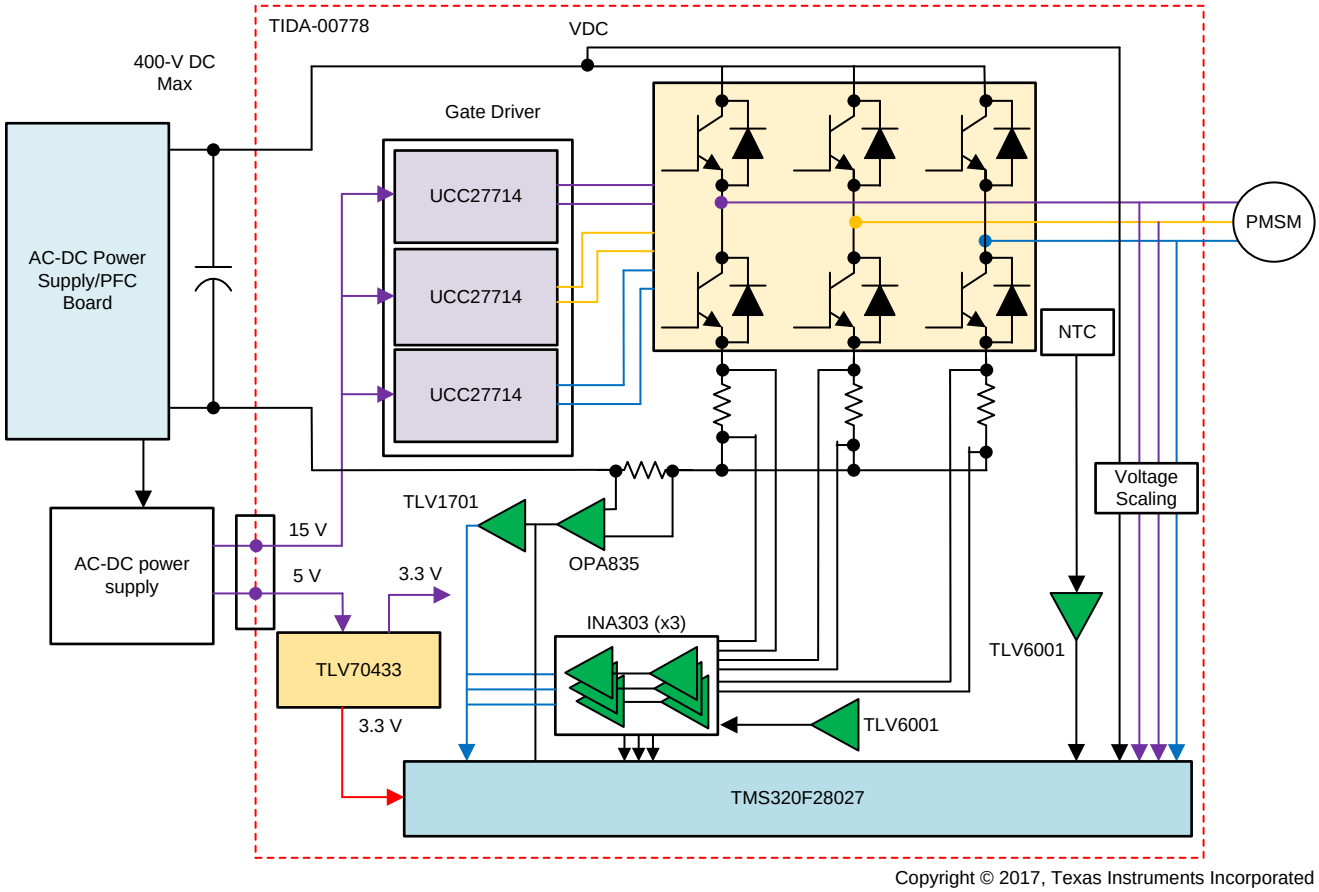


Figure 14. TIDA-00778 Block Diagram

1.4 Design Considerations

1.4.1 Three-Phase Inverter

The three-phase inverter is designed to operate from the DC bus voltage up to 390 V. This design uses an IGBT module.

This reference design is intended to support various makes of IGBT modules. The designer has to adjust the footprint in the layout to fit their IGBT module. The power stage is designed to deliver up to 2 kW output power. The power stage is supplied with 390-V DC maximum and by considering the safety factor, switching spikes, and voltage build-up during regeneration, the IGBT module is selected with the voltage rating equal to 600 V. The current rating of the IGBT depends on the peak winding current. The three-phase inverter bridge is switched using SVM PWM so that sinusoidal current is injected into the motor windings. The peak winding current can be calculated from the system specifications.

Inverter rated output power (P_{OUT}) = 2 kW

DC bus voltage = 325 V (rated), 270 V (minimum) – 390 V (maximum)

Power factor = 0.9 (assumed, for a low-inductance PMSM)

The nominal current in the IGBT module can be calculated at the rated DC bus voltage. With space vector PWM, the maximum RMS line-to-line voltage can be 0.707 times the available DC bus voltage. Refer to the *Space-Vector PWM With TMS320C24x/F24x Using Hardware and Software Determined Switching Patterns* application report for a detailed calculation[3].

$V_{LL\_RMS\ (nom)}$ = 0.707 × 325 = 229.8 V

The rated winding current can be calculated using Equation 3:

$$I_{L(nom)} = \frac{P_{OUT}}{\sqrt{3} \times V_{LL(nom)} \times \cos\varphi} = \frac{2000}{\sqrt{3} \times 229.8 \times 0.9} = 5.58 \text{ A} \quad (3)$$

The peak line current can be calculated using Equation 4:

$$I_{L\_PEAK} = \sqrt{2} \times 5.58 = 7.89 \text{ A} \quad (4)$$

The maximum current in the IGBT module must be calculated at the minimum DC bus voltage (see Equation 5).

$$V_{LL\_RMS(min)} = 0.707 \times 270 = 190.9 \text{ V}$$

$$I_L = \frac{P_{OUT}}{\sqrt{3} \times V_L \times \cos\varphi} = \frac{2000}{\sqrt{3} \times 190.9 \times 0.9} = 6.72 \text{ A} \quad (5)$$

The peak line current is $I_{L\_PEAK} = \sqrt{2} \times 6.72 = 9.5 \text{ A}$.

Considering an overloading and design margin of 200%, the maximum peak winding current to design would be ≈19 A. For this reference design, the IGBT module SK30GD066ET is used. The module has a continuous collector-current-carrying capacity of 30 A at T_C = 25°C and a peak current capacity of 60 A. The selected IGBT module has a built-in negative temperature coefficient (NTC) thermistor and this IGBT temperature rise information is routed to the MCU through a proper signal conditioning circuit to take necessary action.

Figure 15 shows the three-phase inverter circuit. The circuit has a provision to measure all three inverter leg currents and the DC bus return current. R83, R84, and R85 are the inverter leg shunt resistors and R55 and R61 are the DC bus current sense resistors. C30, C31, and C32 are the decoupling capacitors connected across each inverter leg.

The invertor receives the DC power supply from the connector J1. C1 is the DC bus capacitor, as Figure 16 shows. R2 and R4 are the bleeder resistors for the capacitor.

NOTE: C1 is designed as the local storage capacitor. The value is not designed to meet the full capacitor requirement for a 2-kW system. The capacitors on the AC-DC power supply which precede the inverter should be high enough, based on the design requirement.

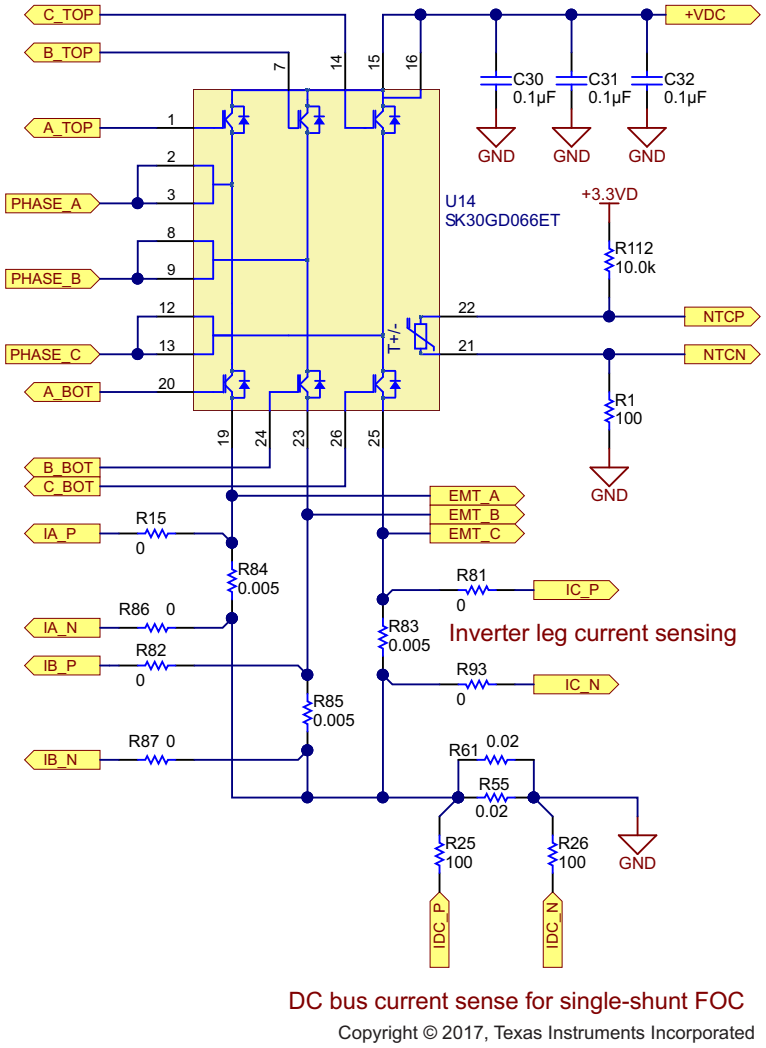


Figure 15. Three-Phase Inverter With Current Sensors

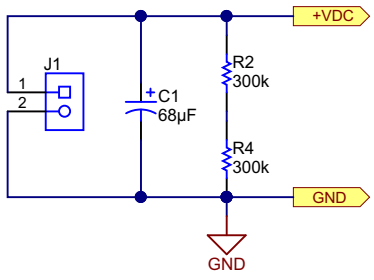


Figure 16. DC Bus Capacitor Placed in Reference Design Board

1.4.2 Current Sense Feedback

The TIDA-00778 design has the option to use one-, two-, and three-shunt current sensing. The following subsection details the design requirements and procedures for each current sensing.

1.4.2.1 Single-Shunt Current Sensing

Figure 17 shows the circuit used to measure the DC bus current for single-shunt current sensing.

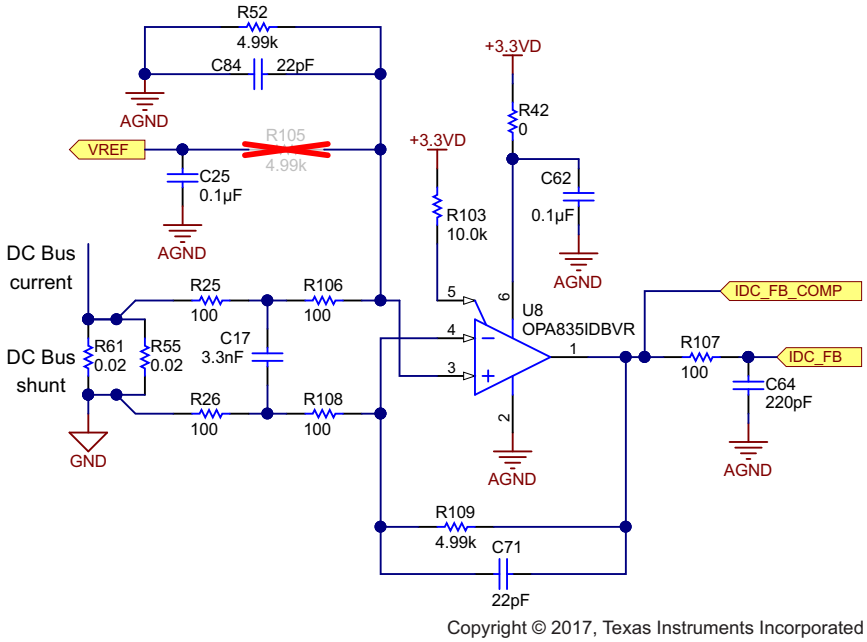


Figure 17. DC Bus Current-Sensing Circuit for Single-Shunt FOC

In the preceding Figure 17, R61 and R55 are the sense resistors and each has a resistance value of 20 mΩ. The voltage drop across the sense resistor can be calculated by using Equation 6:

$$V_{SENSE} = I_{SENSE} \times R_{SENSE} \quad (6)$$

where,

- I_{SENSE} is the current flowing through the sense resistor
- R_{SENSE} is the sense resistor value
- V_{SENSE} is the voltage drop across the sense resistor.

R26, C17, and R25 form the dominant input filter. The input filter cutoff frequency must be selected based on the high-frequency voltage oscillations across the sense resistor during IGBT switching and switching noise from other adjacent switching circuits. By selecting R26 = R25, R106 = R108, and R109 = R52 (with R105 unmounted), the gain of the amplifier stage is given in Equation 7.

$$\text{Gain} = \frac{R109}{(R25 + R106)} \quad (7)$$

The design uses a gain of 24.95V/V. C71 and C84 implements a common-mode noise filter along with R109 and R52. R107 and C64 form an antialiasing filter having a cutoff frequency of 15 MHz. C64 is selected to be greater than 40 times the internal sampling capacitor of the SAR ADC present in the TMS320F28027 MCU to minimize sense voltage dip due to the sampling capacitor current.

NOTE: Mount R105 and unmount R52 if the designer wants to level shift the op amp output voltage. This action may be required in cases where the designer wants to monitor the negative currents in the DC bus, which typically occurs during regenerative breaking and non-unity power factor operation. The reference design uses zero level shift and R105 was unmounted during testing.

1.4.2.1.1 Selecting Sense Resistor for Single-Shunt Current Sensing

Power dissipation in sense resistors and the input-offset error voltage of the op amps are important in selecting the sense-resistance values. A high sense resistance value increases the power loss in the resistors. If the current-sense amplifier is used without offset calibration, select the sense resistor value such that the sense voltage across the resistor is sufficiently higher than the op-amp input offset voltage to reduce the effect of the offset error.

The DC bus sense resistors carry a nominal RMS current of 6.15 A (at 2000 W, 325-V DC). The maximum DC bus current at a minimum DC bus voltage of 270 V is 7.4 A (at 2000 W, 270-V DC). The design uses two 20-mΩ, 3-W resistors connected in parallel in the DC bus return path. Paralleling the two sense resistors increases the power rating and decreases equivalent inductance. The equivalent sense resistance of 10 mΩ allows sensing up to 13.2 A with an amplifier gain of 24.95. The sense resistor has to be selected with a low temperature drift and minimum parasitic inductance (ideally zero).

The power dissipation in the DC bus resistor at the maximum DC bus current equals:
$I_{RMS}^2 \times R_{SENSE} = 7.4^2 \times 10\ m\Omega = 0.5476\ W$.

1.4.2.2 Two- and Three-Shunt Current Sensing

The INA303 device is used to sense and amplify the inverter leg current. The INA303 series of devices feature a high common-mode, bidirectional, current-sensing amplifier and two high-speed comparators to detect out-of-range current conditions. The INA303 comparators are configured to respond to overcurrent in both positive and negative current conditions in a windowed configuration. The device features an adjustable limit threshold range for each comparator set using an external limit-setting resistor. These current-shunt monitors can measure differential voltage signals on common-mode voltages that can vary from –0.1 V up to 36 V, independent of the supply. Figure 18 shows the schematic of the inverter leg current sensing for the phase C.

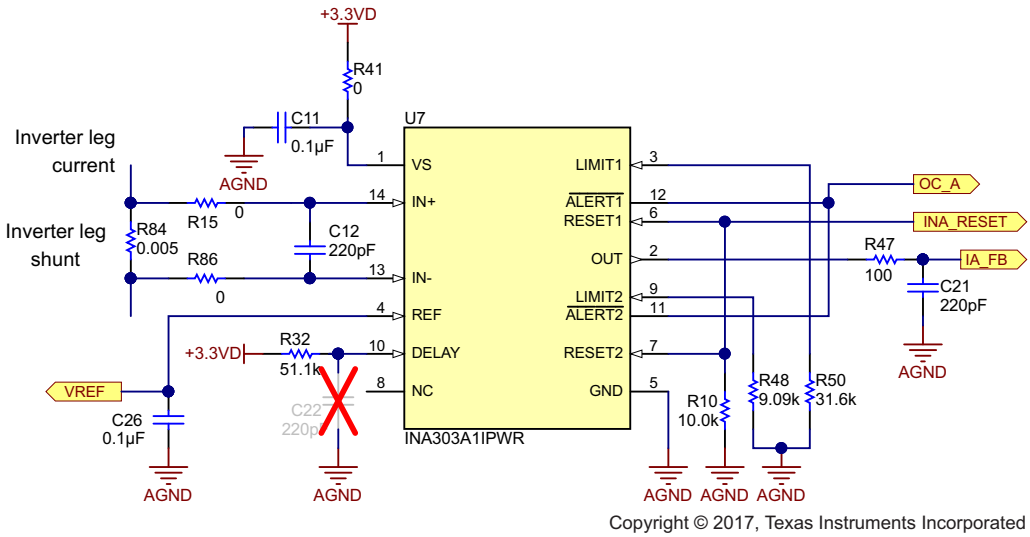


Figure 18. Inverter Leg Current-Sensing Circuit for Two- and Three-Shunt FOC

The INA303 can sense current flow through a sense resistor in both directions. The bidirectional current-sensing capability is achieved by applying a voltage at the REF pin to offset the output voltage. A positive differential voltage sensed at the inputs results in an output voltage that is above the applied reference voltage; likewise, a negative differential voltage at the inputs results in output voltage that is below the applied reference voltage. The calculation for the output voltage of the current-sense amplifier is shown in Equation 8.

$$V_{OUT} = (I_{SENSE} \times R_{SENSE} \times GAIN) + V_{REF} \quad (8)$$

where,

- I_{SENSE} is the current through the sense resistor
- R_{SENSE} is the current sense resistor
- GAIN is the gain option of the device selected
- V_{REF} is the voltage applied to the REF pin.

The reference design uses the following configuration:

- V_{REF} = 1.65 V
- R_{SENSE} = 5 mΩ
- GAIN = 20 (TIDA-00778 design uses INA303A1)

V_{REF} is generated using a voltage follower circuit using the TLV6001 op amp as shown in Figure 19.

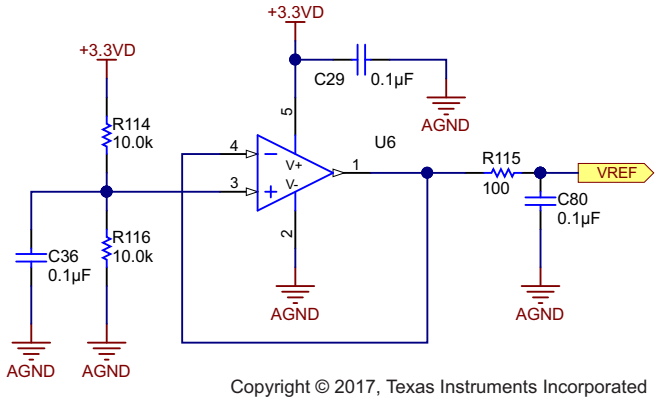


Figure 19. Level-Shift Reference Voltage Generation Using Voltage Follower

Internal comparator of INA303

The internal comparators of the INA303 gives ALERT output for both positive and negative currents. Both ALERTx pins are active-low, open-drain outputs that pull low when the sensed current has been detected to be out of range. Both open-drain ALERTx pins require an external pullup resistor to an external supply. The external supply for the pullup voltage can exceed the supply voltage, V_S, but must not exceed 5.5 V. The pullup resistance is selected based on the capacitive load and required rise time; however, a 10-kΩ resistor value is typically sufficient for most applications. The response time of the ALERT1 output to an out-of-range event is less than 1 µs and the response time of the ALERT2 output is proportional to the value of the external C_{DELAY} capacitor. The equation to calculate the delay time for the ALERT2 output is given in Equation 9:

$$T_{DELAY} = \begin{cases} 1.5\ \mu s & \text{if DELAY is connected with 49.9 k}\Omega \\ \dfrac{C_{DELAY} \times V_{TH}}{I_D} + 2.5\ \mu s & \text{if } C_{DELAY} \geq 47\ pF \end{cases} \quad (9)$$

where,

- C_{DELAY} is the external delay capacitor
- V_{TH} is the delay threshold voltage
- I_D is the DELAY pin current for comparator 2.

If additional delay time on the ALERT2 output is not required, the C_{DELAY} capacitor can be omitted. To achieve minimum delay on the ALERT2 output, TI recommends connecting a resistor DELAY pin to the VS pin. The values for this resistor can vary from 49.9 kΩ to 100 kΩ, based on the required response time versus current consumption trade-off. Both comparators in the INA303 have hysteresis to avoid oscillations in the ALERTx outputs; therefore, tripping a fault threshold moves the recovery threshold in the opposite direction from the initial trip threshold by the value of the hysteresis.

1.4.2.2.1 Selecting Sense Resistor for Two- and Three-Shunt Current Sensing

Power dissipation in sense resistors and the input-offset error voltage of the op amps are important when selecting the sense-resistance values. A high sense resistance value increases the power loss in the resistors. The very-low input offset voltage of INA303 allows the designer to use a very-low sense resistor value, even without offset calibration.

The nominal RMS winding current is 5.58 A (using Equation 3). The inverter leg shunt can only carry current while the low-side switch is ON; therefore, the RMS current in the inverter leg shunt will be smaller than the RMS winding current and the value depends on the duty cycle. However, for the simplification of analysis, the winding current is considered when calculating the shunt resistor power requirement. The peak winding current is 9.5 A (6.72-A_{RMS}) as calculated in Equation 5. The TIDA-00778 uses a 5-mΩ, 3-W sense resistor which allows sensing up to ±16.5 A with an amplifier gain of 20. The sense resistor must be selected with a low temperature drift and minimum parasitic inductance (ideally zero).

The maximum power dissipation in a single-inverter leg current sense shunt resistor equals: $I_{RMS}^2 \times R_{SENSE} = 6.72^2 \times 5\ m\Omega = 0.225$ W.

1.4.3 Gate Driver Using UCC27714

The gate driver UCC27714 has the following features that make the device a good choice for this application:

- High-side, low-side configuration with independent inputs
- Fully operational up to 600 V (HS pin)
- Floating channel designed for bootstrap operation
- Peak output current capability of a 4-A sink and source at V_{DD} = 15 V
- Best-in-class propagation delay (90 ns typically, 125 ns max)
- Best-in-class delay matching (20 ns max)
- Transistor-transistor logic TTL and CMOS-compatible logic input thresholds independent of supply voltage with hysteresis
- V_{DD} bias supply range of 10 V to 20 V
- Undervoltage lockout (UVLO) protection feature on the supply circuit blocks between VDD and VSS pins, as well as between HB and HS pins; the rail-to-rail drive with outputs is held low when inputs are floating
- Robust operation under negative voltage transients (logic operational up to –8 V on HS pin for V_{DD} = 12 V); parasitic inductance in the circuit can cause negative voltage at HS relative to COM, which can cause a logic error on HO if the driver cannot handle the negative voltage of HS
- Separated grounds for logic (VSS) and driver (COM) with the capability to sustain voltage difference
- Optional enable function EN pin

1.4.3.1 Gate Drive Circuit Design

Figure 20 shows the circuit diagram for a half-bridge gate drive using the UCC27714 device.

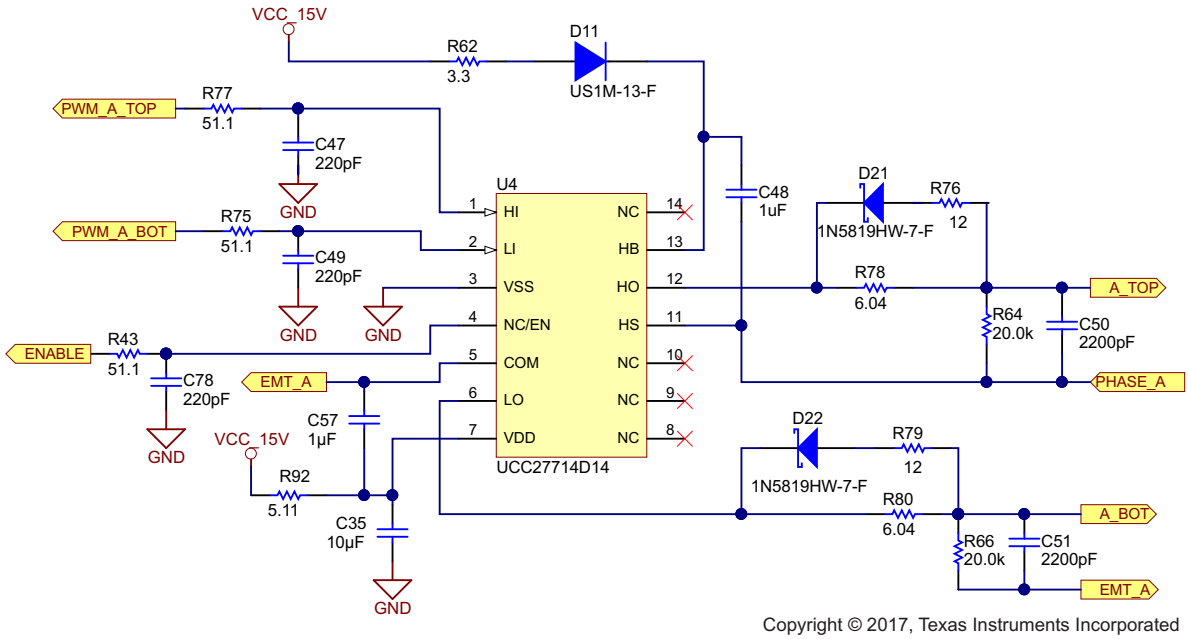


Figure 20. Gate Drive Schematic for Half Bridge

Selecting HI and LI low-pass filter components:

An RC filter should be added between the PWM controller and input pin of UCC27714 to filter the high-frequency noise. The recommended value of the RC filter is R77 = R75 = 51.1 Ω and C47 = C49 = 220 pF.

Selecting bootstrap capacitor (C_{BOOT}):

The bootstrap capacitor must be sized to have more than enough energy to drive the gate of the IGBT high without depleting the bootstrap capacitor more than 10%. A good guideline is to size C_{BOOT} to be at least ten times as large as the equivalent IGBT gate capacitance (C_g). C_g must be calculated based on the voltage driving the high-side gate of the IGBT (V_{GE}) and the gate charge of the IGBT (Q_g). V_{GE} is approximately the bias voltage supplied to V_{DD} after subtracting the forward-voltage drop of the bootstrap diode D11 (V_{DBOOT}). In this design example, the estimated V_{GE} is approximately 14.4 V, as Equation 10 shows.

$$V_{GE} \approx V_{DD} - V_{DBOOT} = 15\ V - 0.6\ V = 14.4\ V \tag{10}$$

The IGBT in this reference design has a specified Q_g of 275 nC. The equivalent gate capacitance of the IGBT can be calculated as Equation 11 shows.

$$C_g = \frac{Q_g}{V_{GE}} = \frac{275\ nC}{14.4} \approx 19.1\ nF \tag{11}$$

After estimating the value for C_g, C_{BOOT} must be sized to at least ten times larger than C_g, as Equation 12 shows.

$$C_{BOOT} \geq 10 \times C_G = 191\ nF \tag{12}$$

For this reference design, a 1-uF capacitor has been chosen for the bootstrap capacitor, as Equation 13 shows.

$$C_{BOOT} = C_{48} = 1\ \mu F \tag{13}$$

Selecting V_{DD} bypass holdup capacitor (C_{VDD}), and R_{BIAS}:

The V_{DD} capacitor (C_{VDD}) must be chosen to be at least ten times larger than C_{BOOT}. For this reference design, a 10-µF capacitor has been selected (see Equation 14). C35 is the V_{DD} capacitor.

$$C_{VDD} \geq 10 \times C_{BOOT} = 10\ \mu F \quad (14)$$

TI recommends selecting a 5-Ω resistor R_{BIAS} series with bias supply and VDD pin to increase the V_{DD} ramp-up time to larger than 50 µs. Refer to the UCC27714 datasheet for more details[1]. The preceding Figure 20 shows how the resistor R92 is used as the R_{BIAS} resistor.

Selecting the bootstrap resistor (R_{BOOT}):

Select the resistor R_{BOOT} to limit the current in D_{BOOT} and limit the ramp-up slew rate of the voltage across the HB and HS pin. TI recommends selecting an R_{BOOT} resistor between 2 Ω and 10 Ω when using the UCC27714 gate driver. This TIDA-00778 reference design uses a current-limiting resistor of 3.3 Ω. The peak bootstrap diode current ($I_{DBOOTPK}$) is limited to approximately 4.36 A (see Equation 15).

$$R_{BOOT} = R62 = 3.3\ \Omega$$

$$I_{DBOOT_{PK}} = \frac{V_{DD} - V_{DBOOT}}{R_{BOOT}} = \frac{15\ V - 0.6\ V}{3.3\ \Omega} \approx 4.36\ A \quad (15)$$

The power dissipation capability of the bootstrap resistor is important. The bootstrap resistor must be able to withstand the short period of high power dissipation during the initial charging sequence of the bootstrap capacitor. This energy is equivalent to ½ × C_{BOOT} × V^2. This energy is also dissipated during the charging time of the bootstrap capacitor (approximately 3 × R_{BOOT} × C_{BOOT}). The TIDA-0778 reference design uses a 3.3-Ω, 0.125-W resistor.

Selecting the bootstrap diode:

The voltage that the bootstrap diode encounters is the same as the full DC bus voltage (in this case a maximum of 390-V DC). The bootstrap diode voltage rating must be greater than the DC bus rail voltage. The bootstrap diode must be a fast recovery diode to minimize the recovery charge and thereby the charge that feeds from the bootstrap capacitor to the 15-V V_{DD} supply.

The diode must be able to carry a pulsed peak current of 4.36 A. However, the average current is much smaller and depends on the switching frequency and the gate charge requirement of the high-side IGBT. The TIDA-00778 reference design uses a 1000-V, 1-A, fast-recovery diode.

Selecting the gate resistor R_{HO} and R_{LO}:

The gate resistors are sized to reduce the ringing caused by parasitic inductances and capacitances and to limit the output source and sink current of the gate driver.

From the UCC27714 datasheet[1]:

- LO and HO output pulldown resistance, R_{HOL} = R_{LOL} = 1.45 Ω
- LO and HO output pullup resistance, R_{HOH} = R_{LOH} = 3.75 Ω

The TIDA-00778 reference design uses different gate resistors in the turnon and turnoff path of the IGBT.

The external gate resistors used are listed below. The external gate resistance in the turnon path of the high side IGBT is R_{HO_ON} = R78 = 6.04 Ω.

The parallel combination of the resistors R78 and R76 form the turn OFF equivalent resistance:

- The external gate resistance in the turnoff path of the high side IGBT, R_{HO_OFF} = 4.02 Ω (6.04 Ω and 12 Ω in parallel)
- The external gate resistance in the turnon path of the low side IGBT, R_{LO_ON} = R80 = 6.04 Ω
- The external gate resistance in the turnoff path of low side IGBT, R_{LO_OFF} = 4.02 Ω (R80 and R79 in parallel)

The following Equation 16 calculates the maximum HO drive current (I_{HO_DR}):

$$I_{HO\_DR} = \frac{V_{DD} - V_{DBOOT}}{R_{HO\_ON} + R_{HOH}} = \frac{15\ V - 0.6\ V}{6.04\ \Omega + 3.75\ \Omega} \approx 1.47\ A \quad (16)$$

The following Equation 17 calculates the maximum HO sink current (I_{HO_SK}):

$$I_{HO\_SK} = \frac{V_{DD} - V_{DBOOT}}{R_{HO\_OFF} + R_{HOL}} = \frac{15\ V - 0.6\ V}{4.02\ \Omega + 1.45\ \Omega} \approx 2.63\ A \quad (17)$$

The following Equation 18 calculates the maximum LO drive current (I_{LO_DR}):

$$I_{LO\_DR} = \frac{V_{DD}}{R_{LO\_ON} + R_{LOH}} = \frac{15\ V}{6.04\ \Omega + 3.75\ \Omega} \approx 1.53\ A \quad (18)$$

The following Equation 19 calculates the maximum LO sink current (I_{LO_SK}):

$$I_{LO\_SK} = \frac{V_{DD}}{R_{LO\_OFF} + R_{LOL}} = \frac{15\ V}{4.02\ \Omega + 1.45\ \Omega} \approx 2.74\ A \quad (19)$$

1.4.3.1.1 Estimating UCC27714 Power Losses (PUCC27714)

Estimate the power losses of UCC27714 ($P_{UCC27714}$) by calculating the losses from several components. The static power losses due to quiescent current (I_{QDD}, I_{QBS}) are calculated in Equation 20:

$$P_{QC} = V_{VDD} \times \left(I_{QDD} + I_{QBS}\right) \quad (20)$$

The power dissipated in the gate driver package during switching (P_{SW}) depends on the following factors:

- Gate charge required for the power device (usually a function of the drive voltage V_G, which is very close to the input bias supply voltage V_{DD} because of the low V_{OH} drop-out)
- Switching frequency
- Use of external gate resistors

To turn on an IGBT, the gate driver must provide the sufficient gate charge. Equation 21 calculates the energy required to supply the gate charge.

$$E_G = Q_G \times V_{GE} \quad (21)$$

where,

- V_{GE} is the gate voltage supplied by the gate driver across the gate and emitter of the IGBT.

If the IGBT is switching at a frequency f_{SW}, then the gate power supplied by the gate driver when the IGBT turns on is calculated in Equation 22:

$$P_{G-ON} = \frac{1}{2} \times Q_G \times V_{GE} \times f_{SW} \quad (22)$$

The same energy also dissipates when the IGBT turns off; therefore, the total gate power required to turn on and turn off one IGBT is calculated in the following Equation 23:

$$P_G = Q_G \times V_{GE} \times f_{SW} \quad (23)$$

Equation 24 calculates the total power loss in a single UCC27714 device:

$$P_{UCC27714} \approx \left(V_{DD} \times \left(I_{QDD} + I_{QBS}\right)\right) + \left(2 \times Q_G \times V_{GE} \times f_{SW}\right)$$

$$P_{UCC27714} \approx \left(15\ V \times \left(750\ \mu A + 120\ \mu A\right)\right) + \left(2 \times 270\ nC \times 15\ V \times 15000\ Hz\right) = 134.55\ mW \quad (24)$$

When external resistors are used in the gate drive circuit, a portion of this power loss is incurred on these external resistors and the power loss in UCC27714 is lower, allowing the device to run at lower temperatures. The TIDA-00778 design utilizes three gate drivers, so the total power loss of the gate drive is 404 mW.

NOTE: The application schematic in Figure 20 shows 20-kΩ resistors across the gate and emitter terminals of the IGBTs. These resistors are a safety precaution and are placed across these nodes to ensure that the IGBTs are not turned on if the UCC27714 device is not in place or not properly soldered to the circuit board. If using a shunt resistor between the COM and VSS pins, then bypass this pin to COM with a 1-uF surface mount device (SMD) capacitor. The TIDA-00778 reference design uses C57 (1 µF) for this purpose. The capacitor C50 and C51 are used to limit induced gate voltage pickup because of the phase node dv/dt. The use of these capacitors depends on the Miller and gate capacitance ratio of the selected IGBT.

1.4.4 Microcontroller Unit

The TMS320F28027F MCU is used in the reference design. The MCUs have special motor control software in execute-only ROM to enable InstaSPIN-FOC™ or InstaSPIN-MOTION™ solutions, with system software support through MotorWare™ Software. The F2802x Piccolo™ family of microcontrollers provides the power of the C28x core coupled with highly-integrated control peripherals in low pin-count devices. Refer to Section 2.1.2 for the peripheral assignments of the MCU. The digital and analog power supplies are provided with adequate decoupling. The analog power supply is decoupled through R40 resistor (the designer can choose a value up to 10 Ω) to isolate the switching currents from the digital power supply, which provides a better power supply noise rejection for the ADC of the MCU.

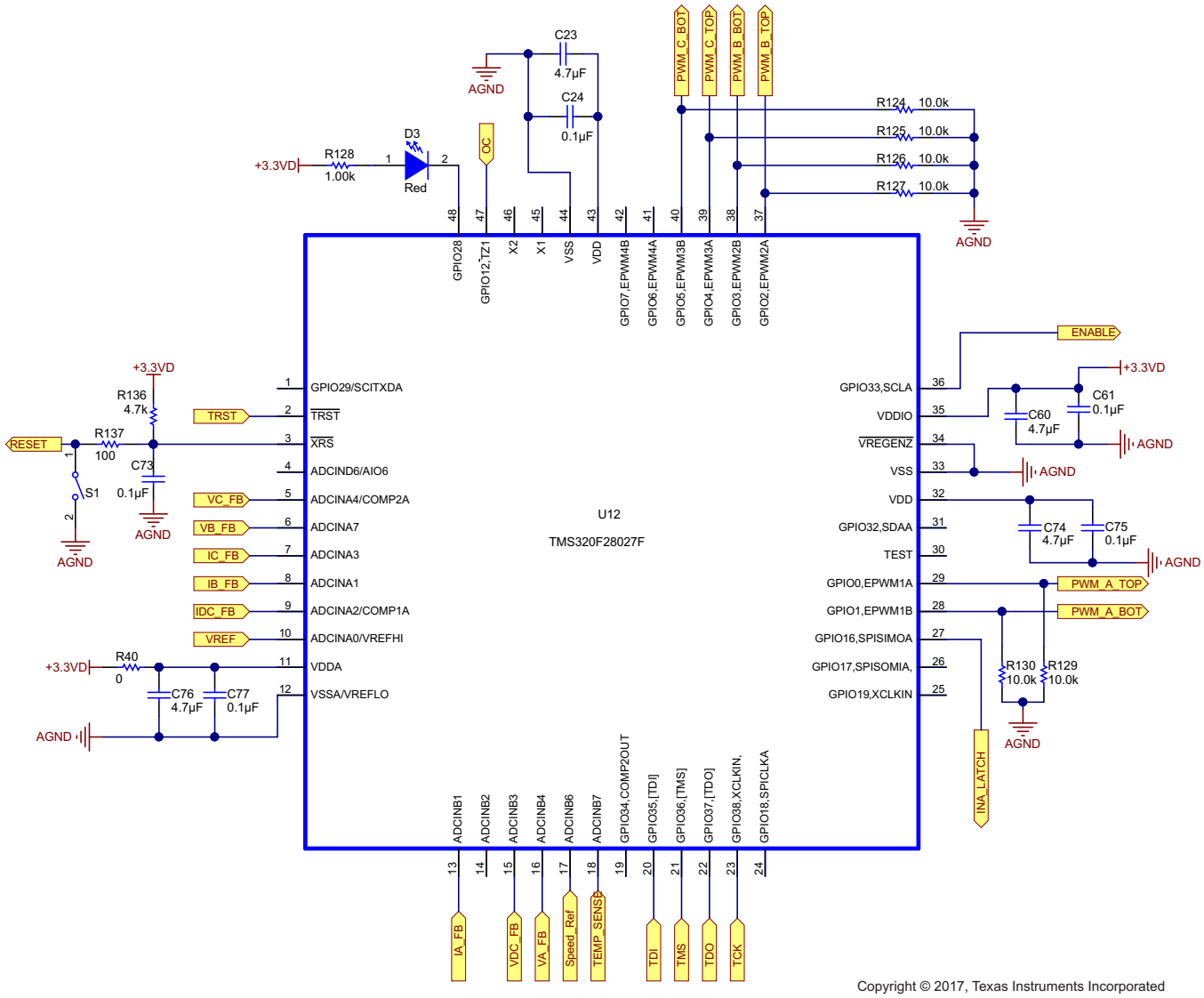


Figure 21. MCU Schematic and Peripheral Connections

1.4.5 Voltage Sensing

The voltage divider circuit that Figure 22 shows is used to measure the winding voltages and DC bus voltage. Voltage feedback is required in the FAST™ software encoder estimator of the InstaSPIN-FOC to allow the best performance at the widest speed range. In FAST, phase voltages are measured directly from the motor phases instead of a software estimate. This software value (USER_ADC_FULL_SCALE_VOLTAGE_V) depends on the voltage divider gain of the circuit, which senses the voltage feedback from the motor phases.

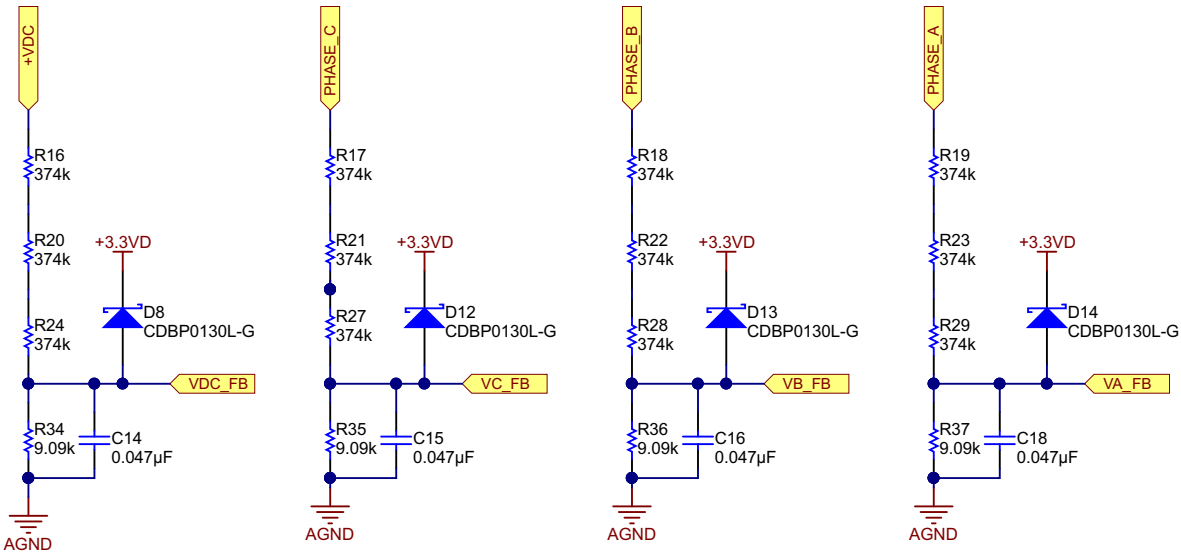


Figure 22. DC Bus and Winding Voltage Sensing

In the preceding Figure 22, PHASE_A, PHASE_B, and PHASE_C are the phase voltages. These voltages are properly scaled and fed to the MCU through VA_FB, VB_FB, and VC_FB. The maximum phase voltage feedback measurable by the MCU can be calculated as Equation 25 shows, considering the maximum voltage for the ADC input is 3.3 V.

$$V_a^{max} = V_{ADC\_a}^{max} \times \frac{(9.09\,k\Omega + 1122\,k\Omega)}{9.09\,k\Omega} = 3.3 \times \frac{(9.09\,k\Omega + 1122\,k\Omega)}{9.09\,k\Omega} = 410.62\ V \quad (25)$$

With that voltage feedback circuit, the following setting is done in *user.h*:

```
//! \brief Defines the maximum voltage at the input to the AD converter
#define USER_ADC_FULL_SCALE_VOLTAGE_V (410.62)
```

For a motor with a maximum operating voltage of 390 V, this voltage feedback resistor divider is ideal. This divider makes sure that the ADC resolution is at the maximum for a motor working from 270-V DC to 390-V DC.

The voltage filter pole is required by the FAST estimator (refer to the *InstaSPIN-FOC™ and InstaSPIN-MOTION™* user's guide) to allow an accurate detection of the voltage feedback. The filter cutoff frequency should be low enough to filter out the PWM signals. As a general guideline, a cutoff frequency of a few hundred Hertz is enough to filter out a PWM frequency of 10 kHz to 20 kHz. The hardware filter should only be changed when ultra-high speed motors are run, which generate phase voltage frequencies in the order of a few kHz. In this reference design, consider the PMSM to have a maximum speed of approximately 3,000 RPM with eight pole pairs. This scenario gives a voltage frequency of: 3000 × 8 / 60 = 400 Hz. The voltage filter of 400 Hz should be enough cutoff frequency for this motor and speed. The filter pole setting can be calculated using Equation 26.

$$F_{filter\_pole} = \frac{1}{2 \times \pi \times R_{parallel} \times C} = \frac{1}{2 \times \pi \times \left(\frac{1122\,k\Omega \times 9.09\,k\Omega}{1122\,k\Omega + 9.09\,k\Omega}\right) \times 0.047\ \mu F} = 375.7\ Hz \quad (26)$$

The following code example shows how this setting is defined in *user.h*:

```
//! \brief Defines the analog voltage filter pole location, Hz
#define USER_VOLTAGE_FILTER_POLE_Hz (375.7)
```

NOTE: The parameter USER_IQ_FULL_SCALE_VOLTAGE_V defines the full-scale value for the IQ30 variable of voltage inside the system. All voltages are converted into per-unit based on the ratio to this value. This value *must* be larger than the maximum value of any voltage calculated inside the control system; otherwise, the value can saturate and roll over, which causes an inaccurate value. This value is *often* greater than the maximum measured ADC value, especially with high back-electromotive force (back-EMF) motors operating at higher than rated speeds. If the value of the back-EMF constant is known, and the designer is operating at higher than rated speed due to field weakening, be sure to set this value higher than the expected back-EMF voltage. Refer to the *InstaSPIN-FOC™ and InstaSPIN-MOTION™* user's guide for more details[2].

1.4.6 External Bias Power Supply and Onboard LDO

The TIDA-00778 reference design board requires external 15-V and 5-V power supplies. The 15 V is used for the gate driver power supply. The TLV70433 low-dropout regulator (LDO) is used to generate the 3.3-V power supply required for the MCU, current sense amplifiers, and the signal conditioning circuits (see Figure 23).

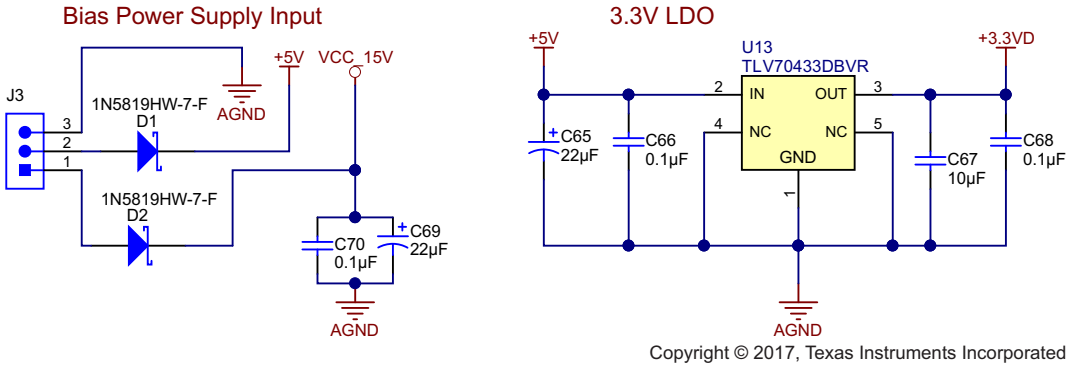


Figure 23. External Bias Power Supply Connection and Onboard LDO

The power supply is designed for the specification as provided in Table 3.

Table 3. Power Supply Specification for 15-V and 5-V Input

DESCRIPTION	VOLTAGE SPECIFICATION			MAXIMUM CURRENT
	MIN	TYP	MAX	
15-V bias power supply (J3)	13.5 V	15 V	16.5 V	50 mA
5-V bias power supply	4.5 V	5 V	5.5 V	300 mA
3.3-V LDO output	—	3.3 V	—	300 mA

1.4.7 IGBT Temperature-Sensing Signal Conditioning Circuit

The IGBT module used in this design has an integrated NTC thermistor. The NTC is biased using one resistor R112 (10 kΩ) to 3.3 V and one resistor R1 (100 Ω) to ground as Figure 15 shows. The 10-k resistor limits the current in the circuit at the minimum temperature sensor resistance. The voltage across the NTC is connected as the differential input to the TLV6001 op amp configured as a differential amplifier.

From the datasheet of IGBT module:

- The resistance of temperature sensor at 25ºC = 5 k
- The resistance of temperature sensor at 100ºC = 493 Ω

$$\text{Voltage across the temperature sensor terminals at } 25^{\circ}\text{C} = 3.3 \times \frac{5\ \text{k}\Omega}{10\ \text{k}\Omega + 5\ \text{k}\Omega + 100\ \Omega} = 1.09\ \text{V}$$

$$\text{Voltage across the temperature sensor terminals at } 100^{\circ}\text{C} = 3.3 \times \frac{493\ \Omega}{10\ \text{k}\Omega + 493\ \Omega + 100\ \Omega} = 0.154\ \text{V}$$

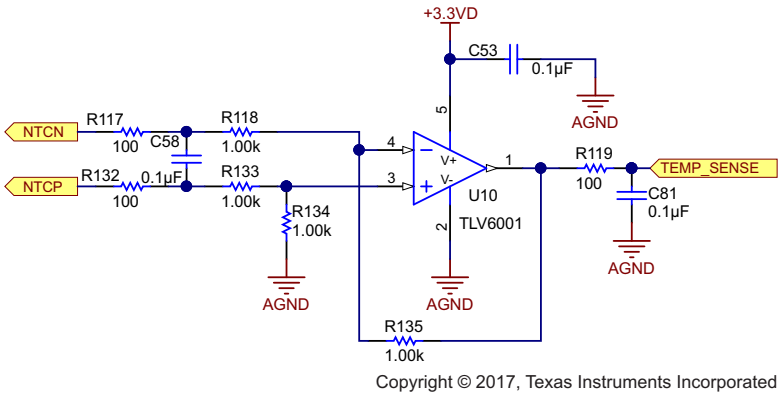


Figure 24. IGBT Temperature-Sensor Signal Conditioning Circuit

The ADC of the MCU reads the output of the temperature sense signal-conditioning circuit and necessary action can be taken for overtemperature protection.

1.4.8 Overcurrent Protection

Figure 25 shows the DC bus overcurrent protection comparator circuit. All the comparators have an open-drain output, which helps in an easy-wired OR structure to create a single-fault output and is connected to the PWM trip-zone (tz) pin of the MCU.

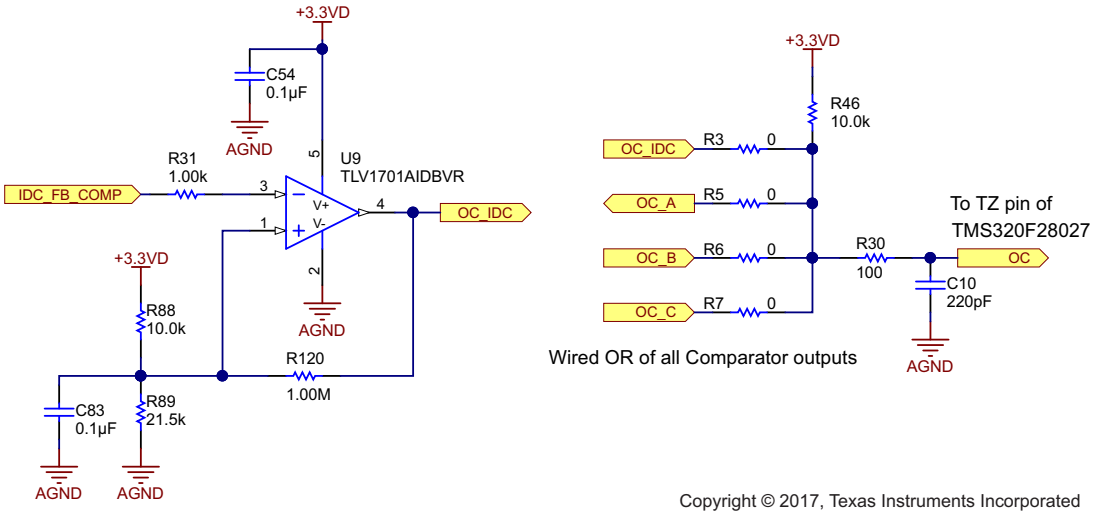


Figure 25. DC Bus Current Sense Overcurrent Protection and Wired OR Structure of All Comparators

1.5 Highlighted Products

1.5.1 OPA835

The OPA835 is an ultra-low-power, rail-to-rail output, negative-rail input, voltage-feedback (VFB) operational amplifier designed to operate over a power supply range of 2.5-V to 5.5-V with a single supply, or ±1.25-V to ±2.75-V with a dual supply. These amplifiers consume only 250 µA per channel and with a unity gain bandwidth of 56 MHz.

The high gain bandwidth and slew rate of an OPA835 allows the designer to use this amplifier in applications like single-shunt FOC, where the fastest settling is required even with high feedback gains. The low offset drift helps to maintain the accuracy across a wide temperature range. The unity gain feature with good phase margin brings the stable operation for a wide range gain required in the application. The OPA835 devices are characterized for operation over the extended industrial temperature range of –40°C to +125°C.

1.5.2 INA303

The INA303 features a high common-mode, bidirectional, current-sensing amplifier and two high-speed comparators to detect out-of-range current conditions. The window comparator in INA303 helps to detect both positive and negative overcurrent peak in bipolar current sensing, which is the case in inverter leg current sensing. The device features an adjustable limit threshold range for each comparator set using an external limit-setting resistor. The open-drain configuration of the comparator output ALERT pin helps in an easy-wired OR structure of multiple faults.

The low offset voltage of 30 uV (maximum), low offset voltage drift (0.25 uV/ºC maximum), and low gain error (0.075 % maximum) allow very accurate current sensing. This device operates from a single 2.7-V to 5.5-V supply. The device is specified over the extended operating temperature range (–40°C to +125°C) (see Figure 26).

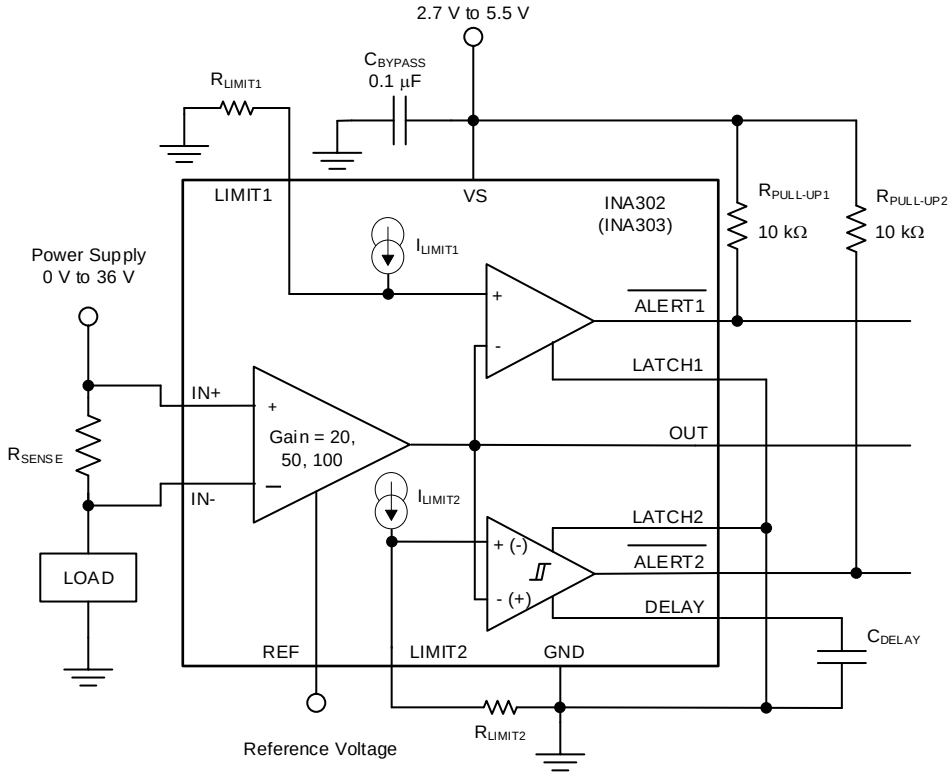


Figure 26. INA303 Functional Block Diagram

Table 4. Features and Benefits of INA303A1

FEATURE	BENEFITS
Low offset voltage (V_{OS} = ±80 μV) and low gain error (0.02%)	Low offset and gain error enables accurate current sensing without calibration
Low offset voltage drift (0.25 μV/°C) and gain error drift (3 ppm/°C)	Ultra-low offset and gain error drift allows high accurate current sensing over entire temperature range without temperature dependent calibration
550-kHz signal bandwidth	High-signal bandwidth supports low-latency inverter leg current measurement enabling faster sensing in two- and three-shunt current sensing
Integrated voltage reference pin	Enables easy bipolar current sensing
Integrated precision gain setting resistors	Better resistor tolerance matching, easier printed-circuit board (PCB) layout, and reduced bill of materials (BOM) cost
Window comparator with independent threshold	Reduced BOM to support overcurrent protection in both the polarity

1.5.3 UCC27714

UCC27714 is a 600-V high-side, low-side gate driver with 4-A source and 4-A sink current capability to drive power MOSFETs or IGBTs. The device comprises one ground-referenced channel (LO) and one floating channel (HO), which is designed for operating with bootstrap supplies. The device features excellent robustness and noise immunity with the capability to maintain operational logic at negative voltages of up to –8-V DC on the HS pin (at V_{DD} = 12 V).

The device features the industry best-in-class input propagation delays and delay matching between both channels, which allows the designer to bring down the pulse-width duration in single-shunt current sensing. The UCC27714 device output stage features a unique architecture on the pullup structure, which delivers the highest peak-source current when it is most required during the Miller plateau region of the power-switch turnon transition (when the power switch drain or collector voltage experiences dv/dt). The COM pin can be used to connect to the emitter or source of the low-side switch to eliminate the ground disturbance due to sense resistors. The device accepts a wide-range bias supply input from 10 V to 20 V and offers UVLO protection for both the VCC and HB bias supply pins. The UCC27714 is available in an SOIC-14 package and rated to operate from –40°C to 125°C.

1.5.4 TMS320F28027F

The F2802x Piccolo family of microcontrollers provides the power of the C28x core coupled with highly-integrated control peripherals in low pin-count devices. This family is code-compatible with previous C28x-based code and also provides a high level of analog integration. An internal voltage regulator allows for single-rail operation. Enhancements have been made to the HRPWM to allow for dual-edge control (frequency modulation). Analog comparators with internal 10-bit references have been added and can be routed directly to control the PWM outputs. The ADC converts from 0- to 3.3-V fixed full-scale range and supports ratio-metric VREFHI and VREFLO references. The ADC interface has been optimized for low overhead and latency.

The TMS320F28027F devices have special motor control software in execute-only ROM to enable InstaSPIN-FOC or InstaSPIN-MOTION solutions, with system software support through MotorWare. While standard C2000™ controlSUITE™ software can be used with these devices, note that this special ROM replaces the standard ROM, which means that certain software functions that controlSUITE projects expect to be in ROM must to be linked into the project. See the *InstaSPIN-FOC and InstaSPIN-MOTION Memory Considerations* section of the *InstaSPIN-FOC™ and InstaSPIN-MOTION™* user's guide[2] or the *Memory* section of the datasheet for more details.

1.5.5 TLV70433

The TLV704 series of low-dropout (LDO) regulators operates over a wide operating input voltage of 2.5 V to 24 V. The TLV704 is available in a 3×3-mm SOT23-5 package, which is ideal for cost-effective board manufacturing.

1.5.6 TLV1701

The TLV170x family of devices offers a wide supply range, rail-to-rail inputs, low quiescent current, and low propagation delay. The open collector output offers the advantage of allowing the output to be pulled to any voltage rail up to +36 V above the negative power supply, regardless of the TLV170x supply voltage, and allows easy-wired OR structure with other fault outputs All devices are specified for operation across the expanded industrial temperature range of –40°C to +125°C.

1.5.7 TLV6001

The TLV600x family of single-, dual-, and quad-channel operational amplifiers features rail-to-rail input and output (RRIO) swings, low quiescent current (75 µA, typical), wide bandwidth (1 MHz), and low noise (28 nV/√Hz at 1 kHz). This family of devices is attractive for a variety of applications that require a good balance between cost and performance, such as white goods.

The robust design of the TLV600x provides ease-of-use to the circuit designer: unity-gain stability with capacitive loads of up to 150 pF, integrated RF/EMI rejection filter, no phase reversal in overdrive conditions, and high electrostatic discharge (ESD) protection (4-kV HBM). The devices are optimized for operation at voltages as low as 1.8 V (±0.9 V) and up to 5.5 V (±2.75 V), and are specified over the extended temperature range of –40°C to +125°C.

2 Hardware, Software, Testing Requirements, and Test Results

2.1 Required Hardware and Software

2.1.1 Hardware

2.1.1.1 Connector Configuration of TIDA-00778

Figure 27 shows the TIDA-00778 connector configuration, which the following list details:

- Two-terminal connector for high voltage DC input (J1): This pin is used to connect the input DC supply from the preceding AC-DC power supply or the power factor correction (PFC) circuit. The positive and negative terminals can be identified as shown in Figure 27. The maximum voltage allowed at this pin is 390-V DC.
- Three-terminal output connector for motor winding connection (J2): The phase output connections for connecting to the three-phase motor winding are shown in Figure 27.
- Three-pin bias power supply connector (J3): This connector is used to provide external power supply to the board. The board requires an external 15-V and 5-V power supply with ±10% tolerance.
- 14-pin JTAG connector (J4): This connector is used for programming the MCU from an external JTAG interface driver.

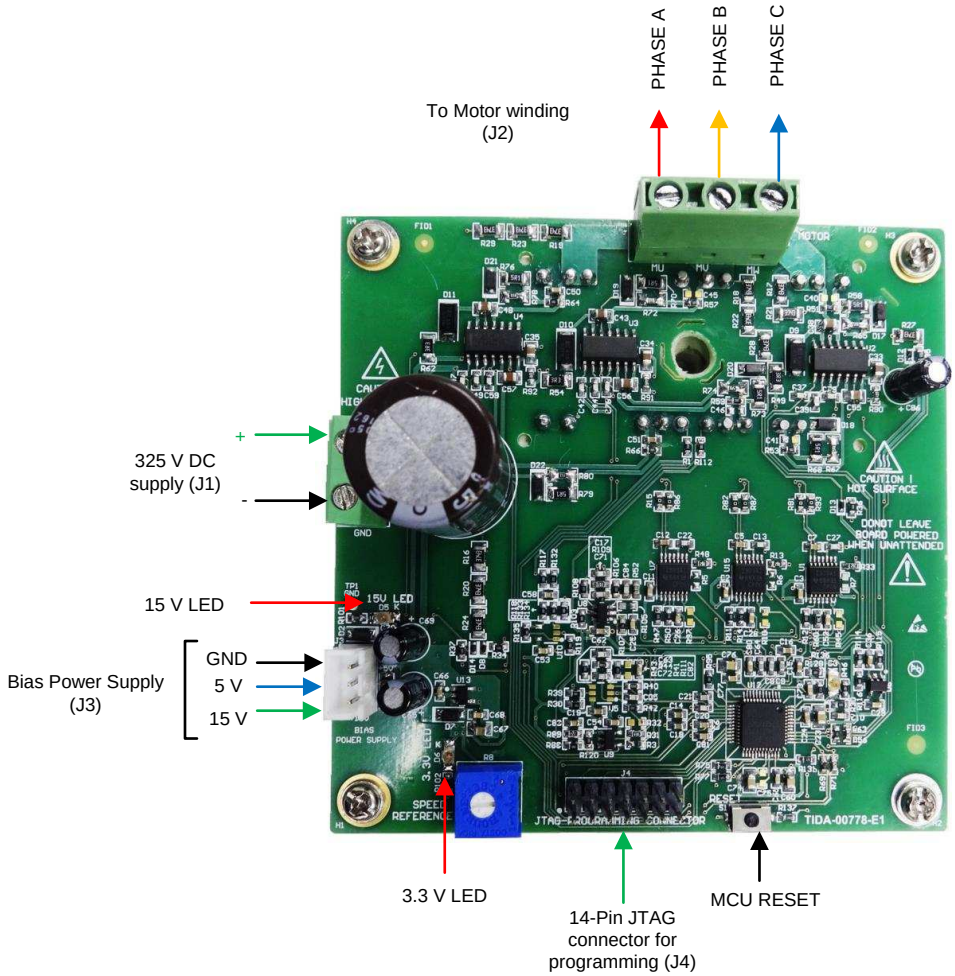


Figure 27. TIDA-00778 PCB Connectors

Table 5 lists the recommended operating voltages on the connectors.

Table 5. Recommended Operating Voltages on Connectors

DESCRIPTION	VOLTAGE SPECIFICATION			MAXIMUM CURRENT
	MIN	TYP	MAX	
High-voltage DC input (J1)	270 V	325 V	390 V	10 A
Motor winding connection (J2)	270 V	325 V	390 V	10 A
15-V bias power supply (J3)	13.5 V	15 V	16.5 V	50 mA
5-V bias power supply	4.5 V	5 V	5.5 V	300 mA

2.1.1.2 Programming of TMS320F28027:

Figure 28 shows the pin details of the 14-pin JTAG connector provided in the board.

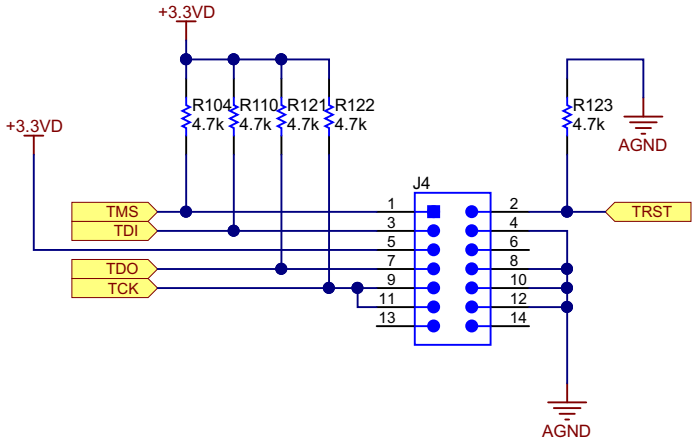


Figure 28. MCU Programming Connector

Refer to http://www.ti.com/product/TMS320F28027F/toolssoftware#devtools for the different programming options of the TMS320F28027.

CAUTION

Use an isolated JTAG interface for programming and real-time debugging of the board, if the board is powered from non-isolated power supplies. The use of a non-isolated JTAG interface is only permitted if all of the power supply to the system is properly isolated with sufficient safety precautions.

2.1.1.3 Procedure for Board Bring-up and Testing Using InstaSPIN-FOC™

The following list details the procedure for board bring-up and testing:

1. Remove the motor connections and high-voltage DC supply input from the board and power on the 5-V supply.
2. Use the power supply from the computer to power the JTAG driver.
3. Program the MCU as detailed in Section 2.1.1.2.
4. Connect the inverter output to the motor winding terminals.
5. Use a current-limited DC source to power up the high-voltage supply input.
6. Refer to the *InstaSPIN-FOC™ and InstaSPIN-MOTION™* user's guide[2]. to understand the detailed procedure for using InstaSPIN-FOC.

2.1.2 Software

2.1.2.1 System Features

The InstaSPIN-FOC is selected as it is easy to work with motors with unknown parameters. The MCU firmware for the C2000™ is taken from MotorWare™ software. MotorWare contains the required projects and libraries to use TI's InstaSPIN-FOC technology. MotorWare can be downloaded from http://www.ti.com/tool/motorware.

This design is similar to the "HVMotorCtrl+PfcKit_v2.1" hardware. Therefore, for Code Composer Studio™ (CCS) projects, use the projects under "hvkit_rev1p1". After installing the MotorWare software, the projects can be found in the folder location: *\motorware\motorware_1_01_00_17\sw\solutions\instaspin_foc\boards\hvkit_rev1p1\f28x\f2802xF\projects\ccs5*.

The pin assignments and ADC channel configuration are defined in the .hal files available at: *motorware\motorware_1_01_00_17\sw\modules\hal\boards\hvkit_rev1p1\f28x\f2802x\src*.

The measurement circuit configurations are defined in: *\motorware\motorware_1_01_00_16\sw\solutions\instaspin_foc\boards\hvkit_rev1p1\f28x\f2802xF\src\user.h*.

The detailed procedure to build and run the lab is provided in the *InstaSPIN-FOC™ and InstaSPIN-MOTION™* user's guide[2].

The following Table 6 shows the hardware assignments in the TIDA-00778 reference design.

Table 6. System Components

SYSTEM COMPONENT		DESCRIPTION
Development and emulation		Code Composer Studio™ software v6.0.1
Target controller		TMS320F28027F
PWM frequency		15 -KHz PWM (default), programmable for higher and lower frequencies
PWM mode		Space vector, complimentary with dead time
Peripherals used	PWM Generation – Timer Configuration	EPWM1A → Phase-A top-switch PWM
		EPWM1B →Phase-A bottom-switch PWM
		EPWM2A → Phase-B top-switch PWM
		EPWM2B → Phase-B bottom-switch PWM
		EPWM3A → Phase-C top-switch PWM
		EPWM3B → Phase-C bottom-switch PWM
	Overcurrent PWM shutoff trip-zone	TZ1 → Overcurrent comparator output (OC)
	ADC channel assignment	ADCINB1 → Phase-A inverter leg current sense feedback
		ADCINA1 → Phase-B inverter leg current sense feedback
		ADCINA3 → Phase-C inverter leg current sense feedback
		ADCINB4 → Phase-A motor voltage sense feedback
		ADCINA7 → Phase-B motor voltage sense feedback
		ADCINA4 → Phase-C motor voltage sense feedback
		ADCINB3 → DC bus voltage sense feedback
		ADCINA2 → DC bus current sense feedback
		ADCINB7 → Temperature sense feedback
		ADCINB6 → Potentiometer voltage feedback
	GPIO	GPIO28 → LED Indication
		GPIO33 → Gate driver ENABLE
		GPIO16 → INA303LATCH signal

2.2 Testing and Results

2.2.1 Test Setup

Figure 29 shows the load setup used to test the motor. The load is an electrodynamometer-type load by which the load torque applied to the motor can be controlled.

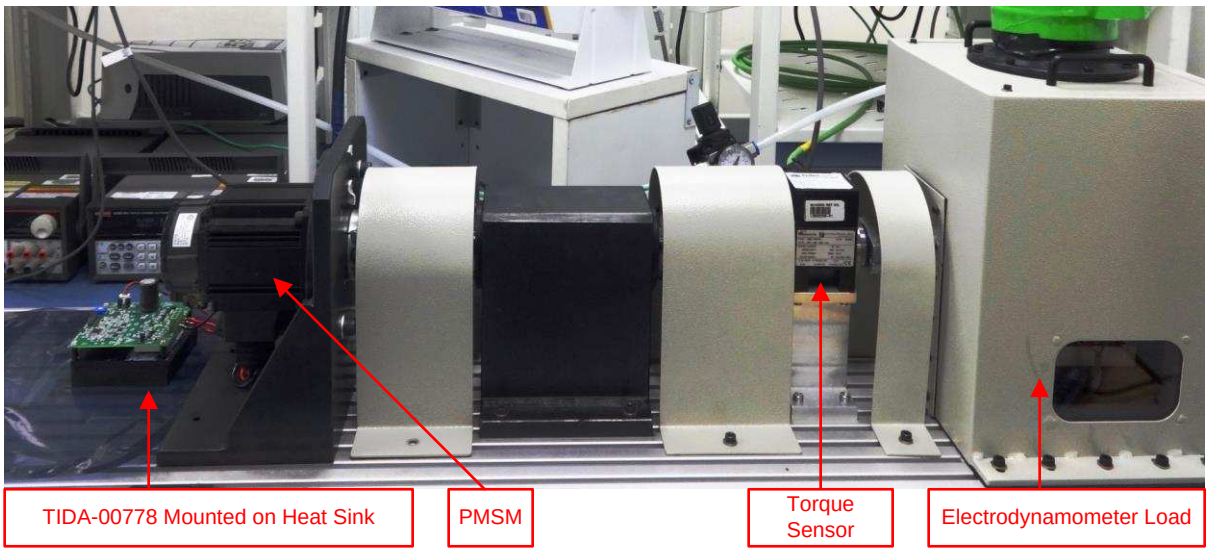


Figure 29. Board and Motor Test Setup

2.2.2 Test Results

2.2.2.1 3.3-V Power Supply Generated by TLV70433 LDO

Figure 30 shows the 3.3 V generated from the TLV70433 LDO. The ripple in the 3.3-V rail is also shown in Figure 30.

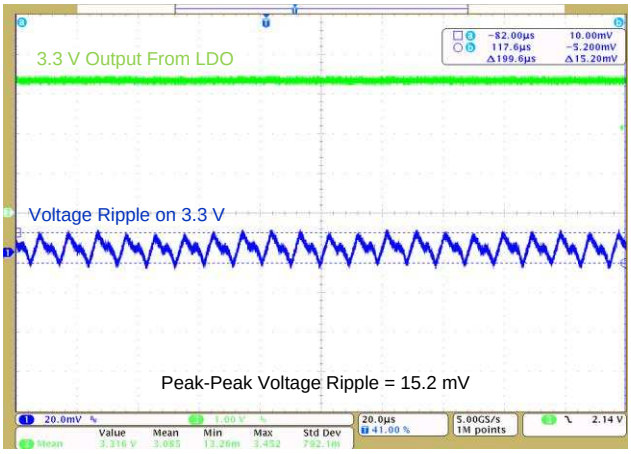


Figure 30. Output Voltage of 3.3 V and Voltage Ripple From TLV70433 LDO

2.2.2.2 Functional Evaluation of UCC27714 Gate Driver

The UCC27714 gate driver receives the PWM signals from the MCU and the corresponding gate drive voltages are generated. Figure 31 shows the low-side and high-side PWM input of the UCC27714 device and the corresponding low-side and high-side output of the UCC27714 device measured across the gate to the emitter (V_{GE}) of the IGBT. The low-side gate output from the UCC27714 device swings between ground and VCC (15 V) and the high-side gate output from the UCC27714 device swings between ground and 14.4 V (VCC – diode drop).

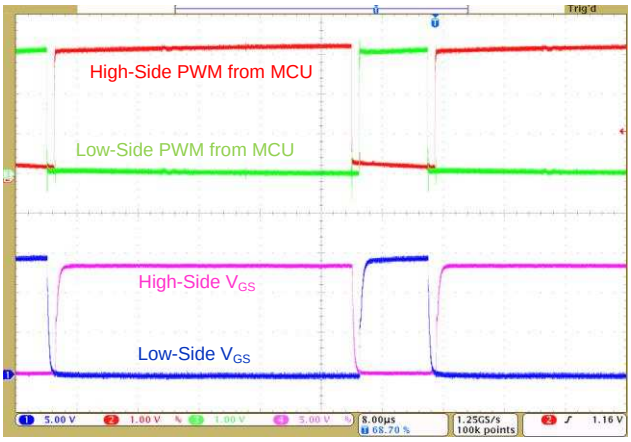


Figure 31. Low-Side and High-Side Gate Drive Voltage From UCC27714

The scope shots in Figure 32 show the PWM signals and high-side and low-side gate to source voltage from UCC27714, which shows that the dead time inserted by the MCU at both the edges of the PWM. The dead time is programmed to 1 µs.

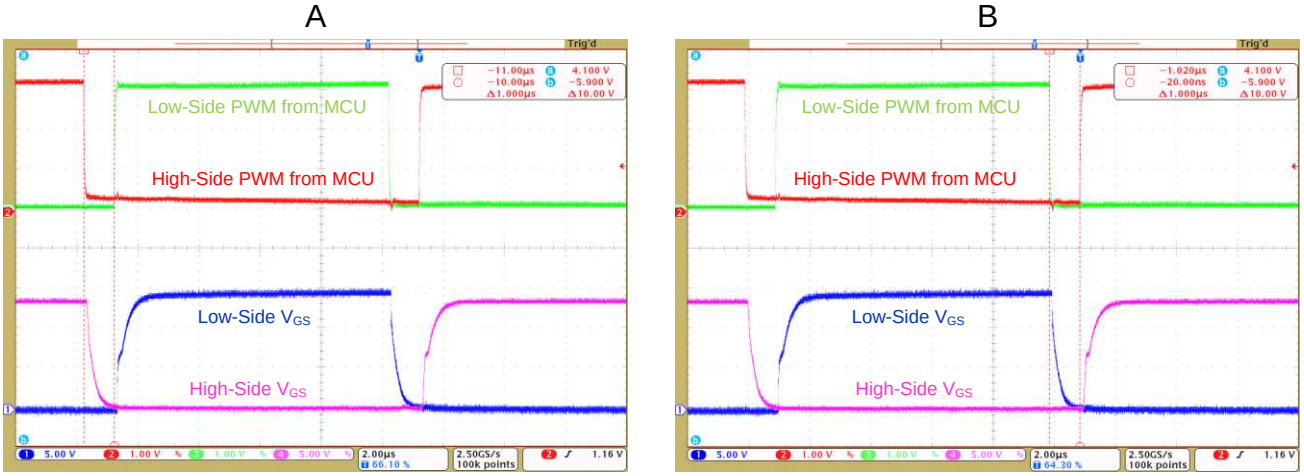


Figure 32. (A) Dead Time at Falling Edge of Low-Side PWM (B) Dead Time at Rising Edge of Low-Side PWM

Figure 33, Figure 34, and Figure 35 show the source and sink current provided by UCC27714. The results are captured with the following test conditions:

- $R_{G(on)}$ = 6.04 Ω
- $R_{G(off)}$ = 4 Ω, equivalent turnoff resistance = 6.04||12 = 4
- Gate charge (Q_G) = 270 nC

During this testing no external capacitance is connected between the gate and source of the IGBT.

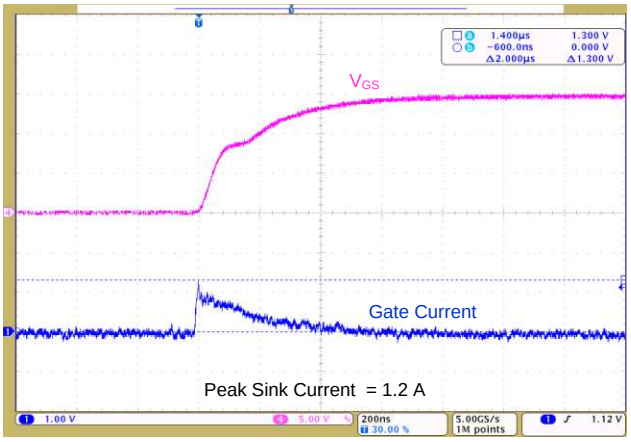


Figure 33. Source Current From Gate Driver

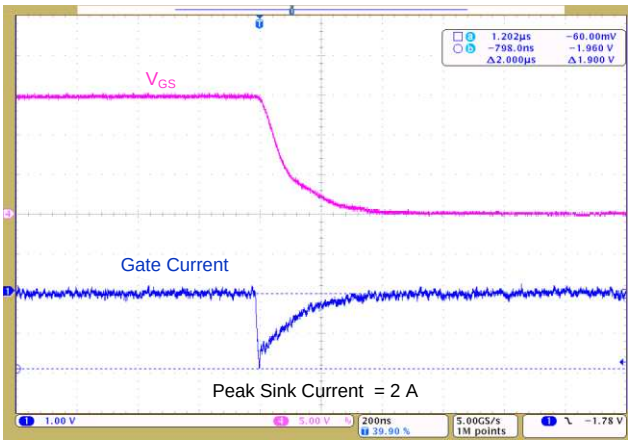


Figure 34. Sink Current From Gate Driver

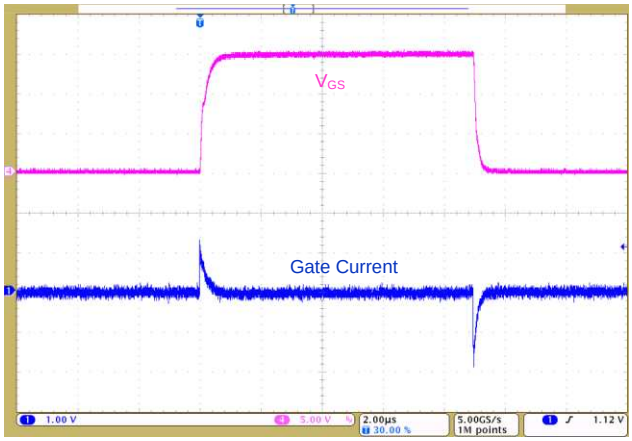


Figure 35. Source and Sink Current From Gate Driver

A bootstrap capacitor of 1 µF is used in the reference design. Figure 36 shows the ripple on the bootstrap capacitor. The peak-to-peak ripple voltage is 0.55 V. The test result is taken with a duty cycle of 80% and the designed bootstrap capacitor maintains voltage ripple within 5% and eliminates undervoltage lockout even in the worst conditions.

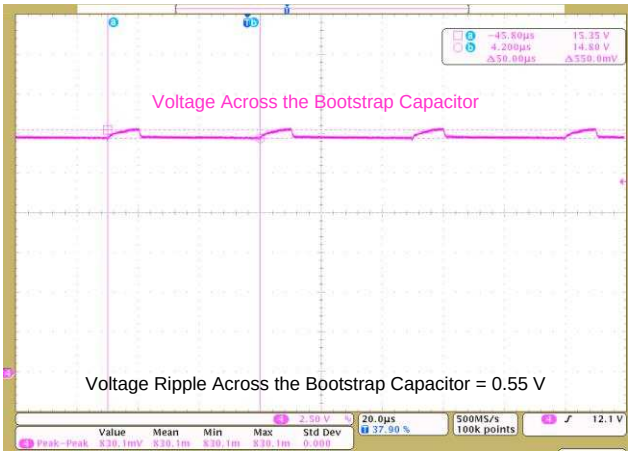


Figure 36. Voltage Ripple Across Bootstrap Capacitor

The scope shots in Figure 37 show the propagation delays measured for the low-side and high-side gate drivers at rising and falling edges. The measured propagation delay is less than 90 ns. The UCC27714 datasheet specifies the propagation delay of 90 ns (typical). The best-in-class propagation delay of the gate driver UCC27714 helps to achieve the lowest active-voltage-vector duration in single-shunt FOC.

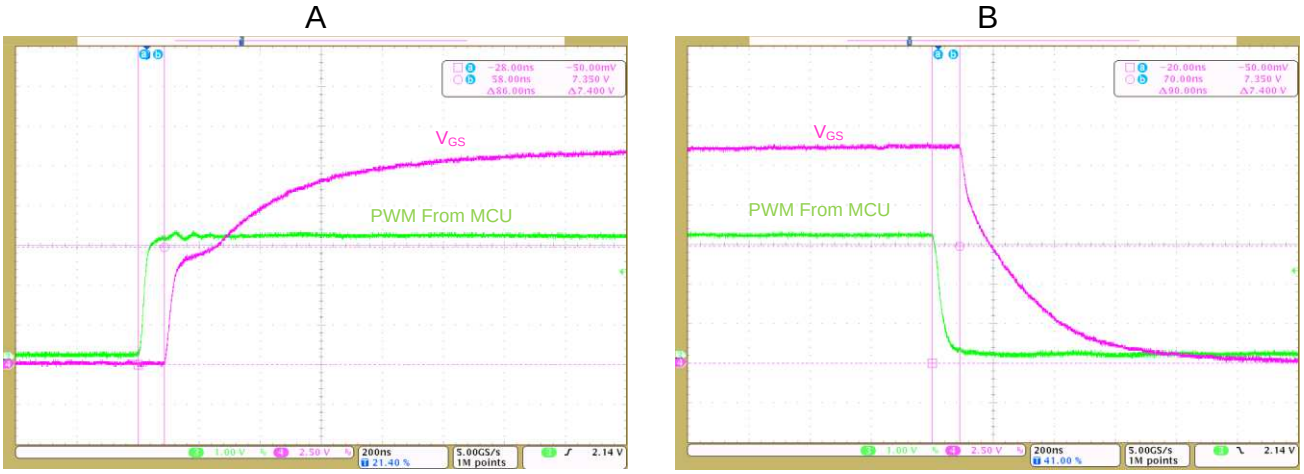


Figure 37. (A) Gate Driver Propagation Delay During PWM Turnon (B) Gate Driver Propagation Delay During PWM Turnoff

2.2.2.3 Single-Shunt Current Sensing

The transient response of the single-shunt current sense amplifier is evaluated with a step change in voltage across the shunt resistor. The step change in sense voltage is created by switching the corresponding IGBTs with the motor connected, causing the winding current to flow through the sense resistor.

Figure 38 shows the simulated step response of OPA835 with the circuit as shown in Figure 17. The settling time of the amplifier configuration to 95% of the steady state value is 800 ns.

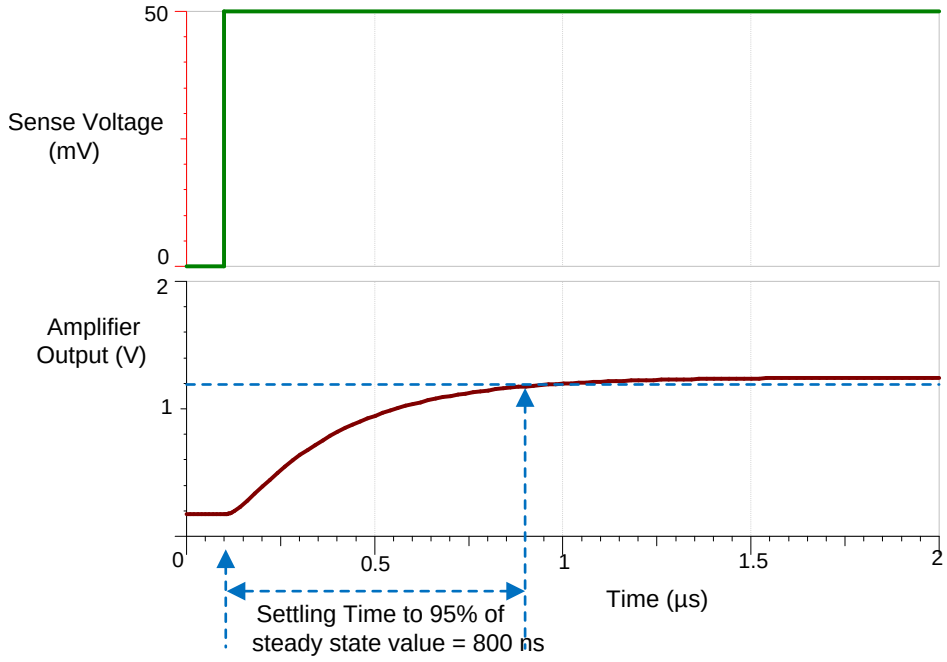


Figure 38. Simulated Step Response of DC Bus Current-Sensing Circuit

The step response of the amplifier is evaluated on TIDA-00778 and the test conditions are:

- Two 20-mΩ resistors are connected in parallel to get an effective shunt resistance of 10 mΩ
- Amplifier gain is set to 24.95
- Winding current = 5 A. The winding current of 5 A is selected because this value is close to the peak swing at 2 kW of inverter power.

Figure 39 shows the step response with a low-value input differential filter formed by R25, R26, and C17. The test is done with R25 = R26 = 100 Ω and C17 = 330 pF. The oscillations are produced mainly because of the parasitic inductance of the shunt resistor, circuit parasitic capacitance in the current path, and by the coupled noise from the IGBT switching. The input filter cutoff frequency is too high to filter the oscillations from the sense resistor. The voltage oscillations across the sense resistor propagate through the op amp. The high bandwidth of the op amp helps to track the voltage across the sense resistor at the output of the op amp. The ramp-up time of the output is 496 ns. The use of a sense resistor with minimum parasitic inductance helps to reduce oscillations, which enables it to achieve the minimum settling time.

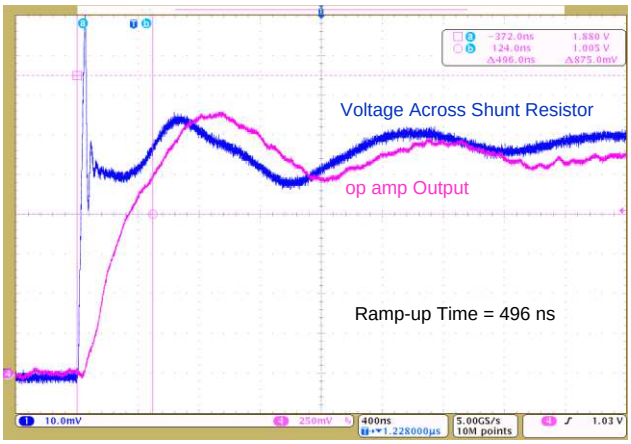


Figure 39. Transient Response of Current Sense Amplifier With Low-Value Input Filter

In the reference design, the input filter cutoff frequency is changed to suppress the voltage oscillations across the shunt resistor. The input filter critically damps the oscillations and therefore reduces the settling time. The reference design uses C17 = 3.3-nF filter along with R25 = R26 = 100 Ω. Figure 40 shows the transient response of the amplifier with a high input filter and the settling time is 976 ns to reach the final steady-state value within 5% dynamic error. The High GBW and the slew rate of OPA835 helps to achieve the fast ramp-up and settling time at a high gain of 24.95 V/V. The ramp-up and settling time can be further optimized by using a lower input filter with a very-low inductance shunt resistor.

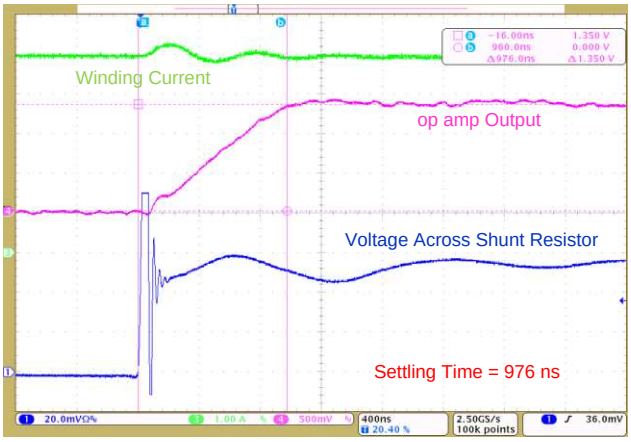


Figure 40. Transient Response of Current Sense Amplifier With High-Value Input Filter

The single-shunt amplifier configuration enables a minimum pulse width duration of 1 µs. The scope shots in Figure 41 show the total delay observed including the gate driver propagation delay and the current sense amplifier settling time, which enable a minimum active-vector duration less than 1 µs.

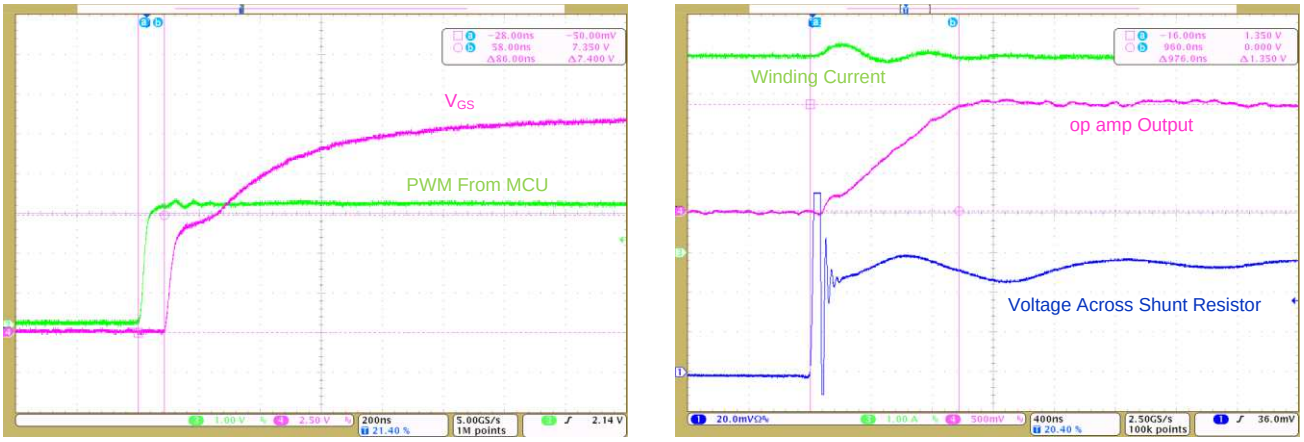


Figure 41. Single-Shunt Amplifier Configuration Enables Minimum Active-Vector Duration of 1 µs

The maximum measured propagation delay at the rising edge of gate signal, (T_{PD}) = 90 ns. The rise time plus the settling time of the amplifier, $T_r + T_s$ = 1066 ns; therefore, $T_r + T_s + T_{PD}$ = 1066 ns ≈ 1 µS.

2.2.2.4 *Single-Shunt Current Sensing Over PWM Cycle*

Figure 42 shows the performance of the single-shunt current sense over a space vector PWM (SVPWM) cycle at a 5-A winding current and at a medium active-voltage-vector duration. The fast settling of the amplifier provides more than enough time for the ADC to sample the current signal.

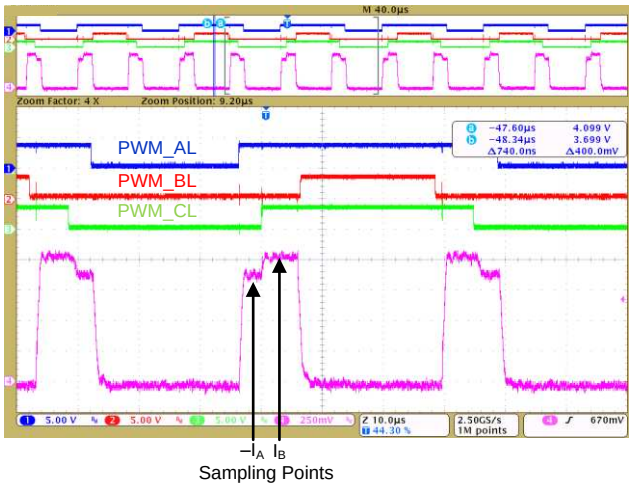


Figure 42. Single-Shunt Current Sampling at Medium Active-Voltage Vector Duration

Figure 43 shows the performance of the single-shunt current sense amplifier over an SVPWM cycle at a 5-A winding current and at a very-low active-voltage-vector duration of approximately 1 µs. The faste settling time provided by the OPA835 helps to achieve the minimum active-vector duration (as low as 1 µs), which provides enough time for the ADC to sample the signal.

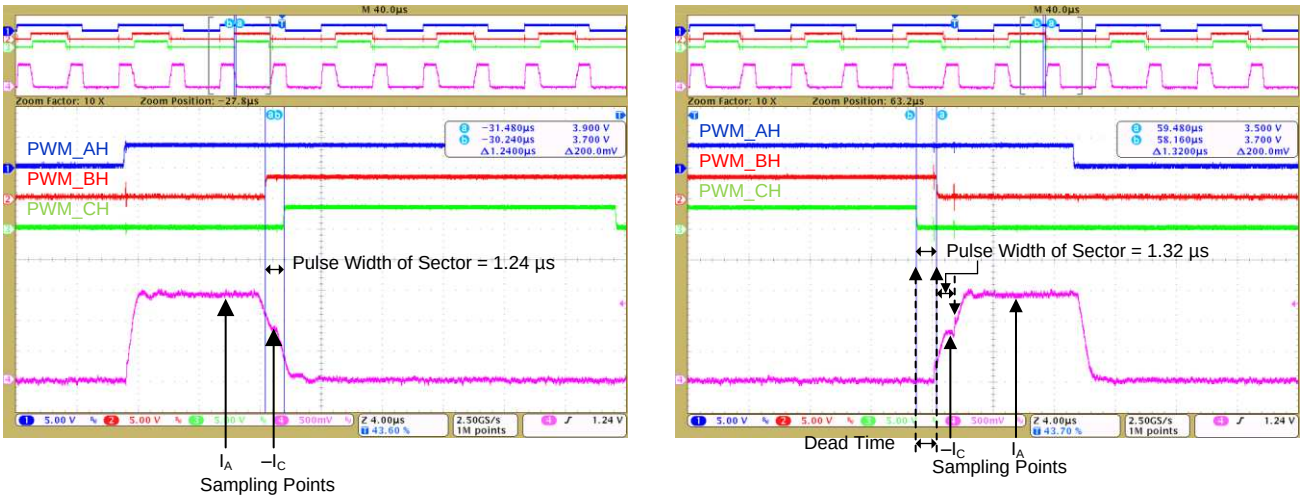


Figure 43. Single-Shunt Current Sampling With Active Voltage Vector Duration of 1.24 µs at Both Halves of SVPWM Cycle

2.2.2.5 *Single-Shunt Current Sensing Transfer Function*

Figure 44 shows the steady-state transfer function of the DC bus current through the 10-mΩ shunt resistor versus the output voltage of the OPA835 amplifier. The output voltage equals 7.25 mV when the DC bus current is zero. The transfer function is linear, which makes the software processing simple.

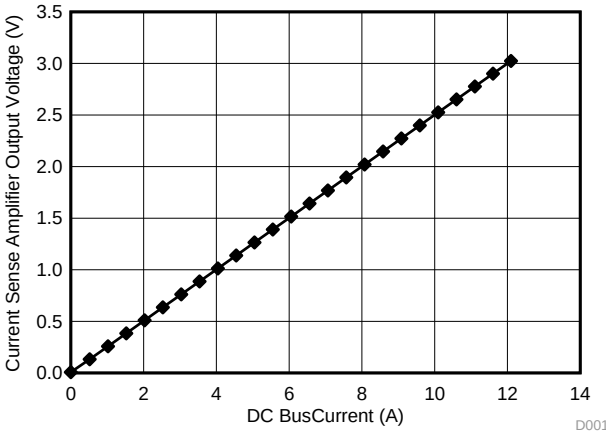


Figure 44. DC Bus Current-Sensing Transfer Function

2.2.2.6 DC Bus Current Sensing Accuracy

The test is done to measure the DC accuracy of the current sense amplifier with a 10-mΩ sense resistor and OPA835 configured as a single-ended differential amplifier configuration at a gain of 24.95 V/V at 25ºC ambient temperature. The full-scale DC bus current range is 0 A to 13.2 A. The DC bus current is measured with a precision 6½ digit multimeter in series to the DC shunt and the output voltage of the current sense amplifier OPA835 is measured with a 6½ digit precision multimeter.

Figure 45 shows the absolute error in DC bus current measurement. The uncalibrated absolute error remains within ±0.1 A with respect to the input current range from 0 A to +12 A. The uncalibrated error is dominated by sense resistor tolerances. The absolute error with calibration on the sense resistor tolerance is less than ±0.03 A. Furthermore, with offset calibration, the absolute error reduces to less than ±0.015 A. Figure 46 shows the calibrated and uncalibrated relative error [%] in measured current from the op-amp output voltage. The calibrated relative error is less than 0.15%. The error can be further optimized by using the amplifier gain setting resistors with tight tolerance. The low error enables accurate current sensing and better performance from the motor drive.

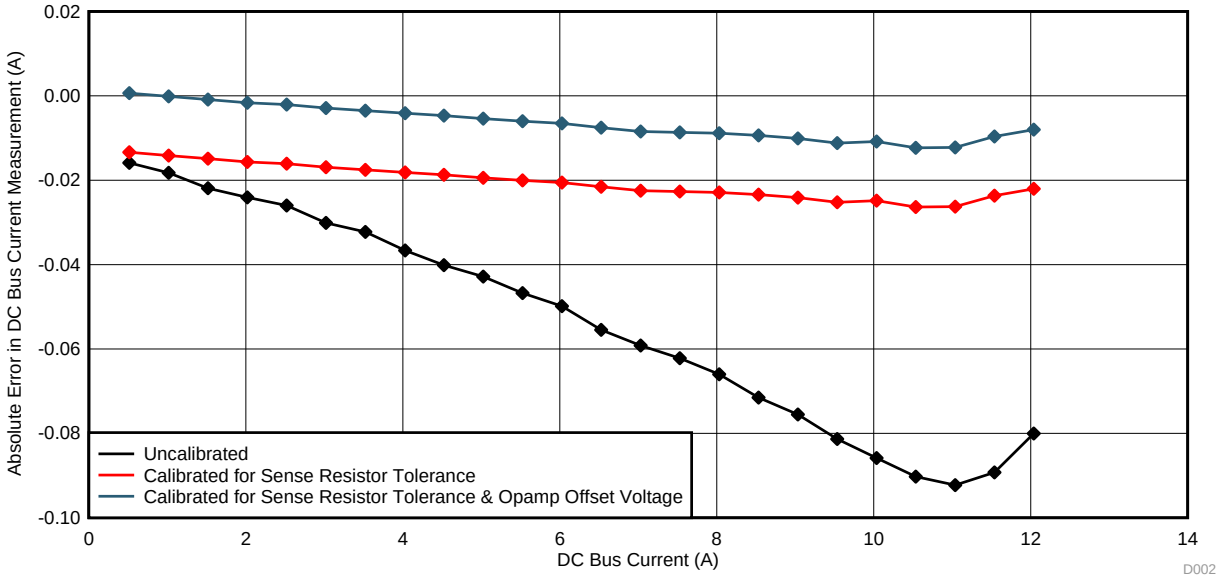


Figure 45. Absolute Error in DC Bus Current Measurement

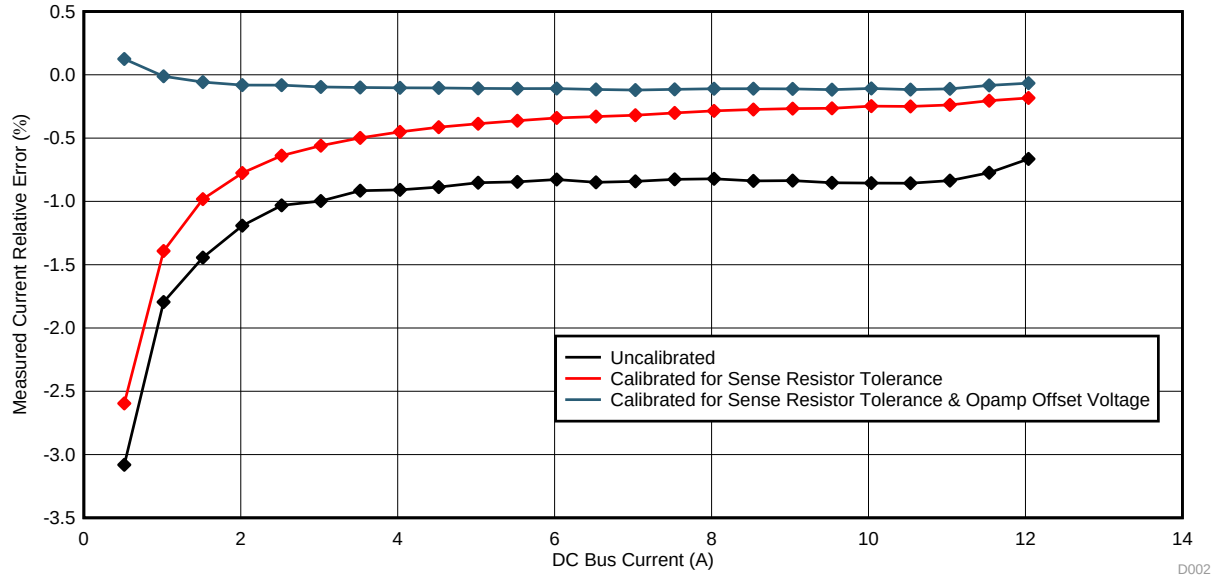


Figure 46. Relative Error [%] in Measured Current From Amplifier Output Voltage

2.2.2.7 Two- and Three-Shunt Current Sensing Using INA303

The INA303 current sense amplifier is used to sense the inverter leg current. The transient response of the inverter leg current sense amplifier is evaluated with a step change in voltage across the shunt resistor, which is created by switching the corresponding IGBTs with the motor connected, which causes the winding current to flow through the sense resistor.

The step response of the amplifier is evaluated on TIDA-00778 and the test conditions are as follows:

- 5-mΩ resistor is used as the inverter leg shunt resistor
- Amplifier gain is 20 V/V provided by the INA303A1
- Winding current = ±5 A

Figure 47 and Figure 48 show the step response of the current sense amplifier. Compared to single-shunt current sensing, lower bandwidth sensing is sufficient for two- and three-shunt current sensing. The oscillations are produced by the shunt resistor and are filtered by INA303 because of its slew rate limit.

The output of the INA303 has an output voltage level shift of 1.65 V by providing 1.65 V at the VREF pin INA303, which means the output voltage is 1.65 V at 0 A. The TIDA-00778 uses an op-amp voltage follower to derive 1.65 V. The measured VREF on the board is 1.628 V (the variation error is mainly from the resistive divider tolerance, refer to Figure 19). The inverter leg current can have both positive and negative polarity based on the direction of winding current. Figure 47 shows the transient response of the sensing circuit with positive voltage polarity across the sense resistor and Figure 48 shows the transient response of the sensing circuit with negative voltage polarity across the sense resistor. The evaluation is done at the phase-C inverter leg.

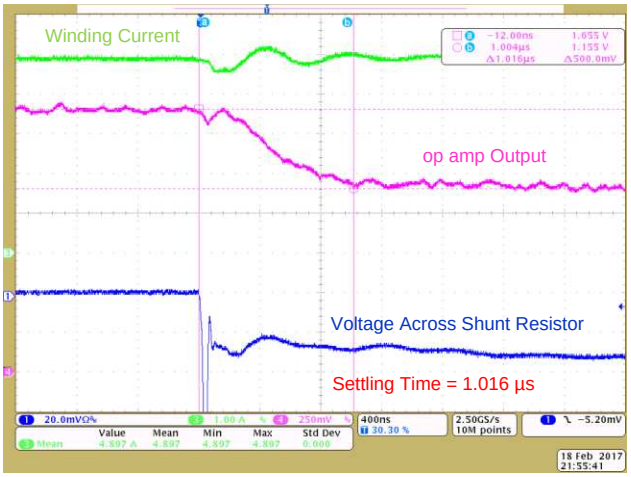


Figure 47. Transient Response of Sensing Circuit With Positive Voltage Polarity Across Sense Resistor

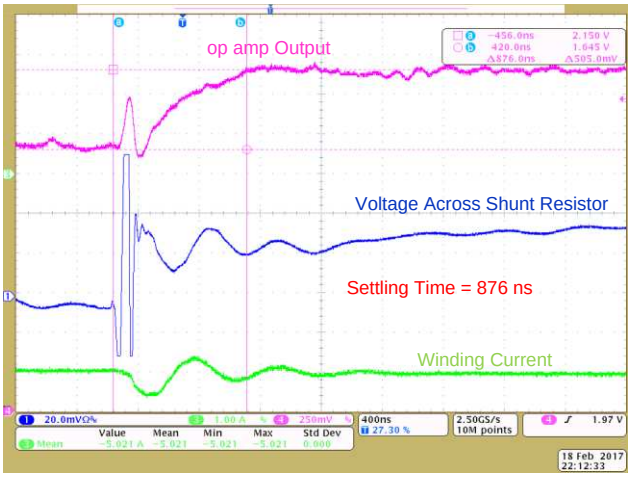


Figure 48. Transient Response of Sensing Circuit With Negative Voltage Polarity Across Sense Resistor

The settling time is approximately 1 µs to reach the final steady-state value within 5% dynamic error for a voltage swing from 1.65 V to 2.15 V, which indicates a differential voltage swing of 500 mV.

2.2.2.8 Single-Shunt Current-Sensing Transfer Function

Figure 49 shows the steady state transfer function of inverter leg current through the 5-mΩ shunt resistor versus the output voltage of the INA303 amplifier. The output voltage equals 1.628 V when the inverter leg current is zero.

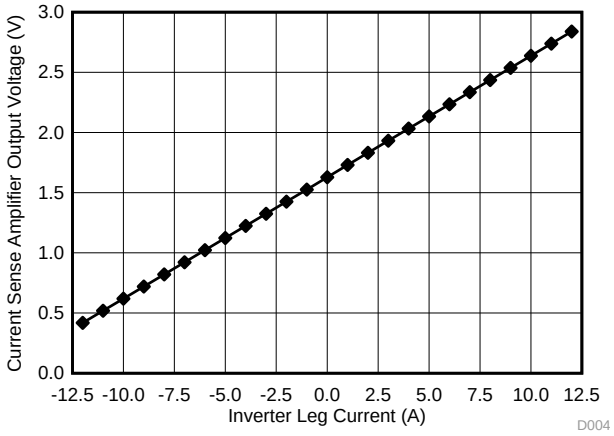


Figure 49. Phase-C Inverter Leg Current-Sensing Transfer Function

2.2.2.9 Inverter Leg Current-Sensing Accuracy With INA303

The test is done to measure the DC accuracy of the current sense amplifier using INA303 with 5-mΩ sense resistor at a gain of 20 V/V and at 25ºC ambient temperature. The full-scale DC bus current range is –16.5 A to +16.5 A. The inverter leg current is measured with a precision 6½ digit multimeter in series to the inverter leg shunt and the output voltage of the current sense amplifier INA303 is measured with another precision 6½ digit multimeter.

The INA303A1 has a gain tolerance of 0.02% and a gain drift of 3 ppm/°C. Figure 50 shows the absolute error in inverter leg current measurement. The uncalibrated absolute error remains within ±0.15 A with respect to the input current range from –16.5 A to +16.5 A. The uncalibrated error is dominated by sense resistor tolerances. The current sense amplifier output error is calibrated for sense resistor tolerances and the calibrated output error is less than ±0.01 A. Figure 51 shows the relative error [%] in measured current from the amplifier output voltage. The calibrated relative error is less than 0.04%. The very-low offset voltage of INA303 enables the designer to use the current sense amplifier even without offset calibration. The integrated gain setting resistors with low gain error help to achieve an overall low output error, which enables accurate current sensing, reduces software overhead on calibration, and provides better performance from the motor drive.

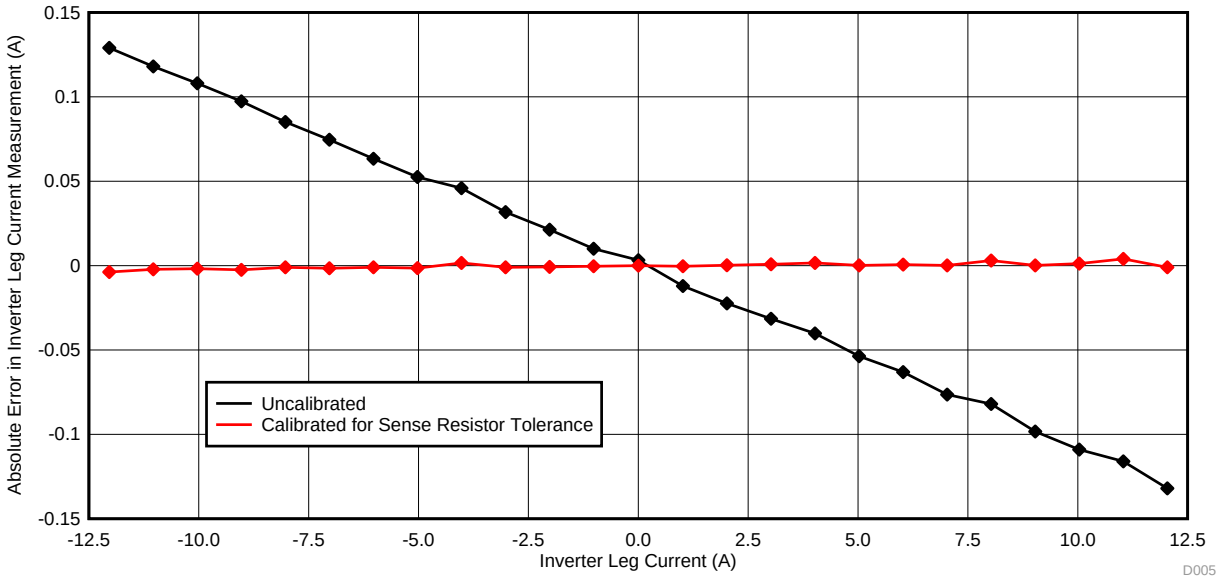


Figure 50. Absolute Error in Inverter Leg Current Measurement

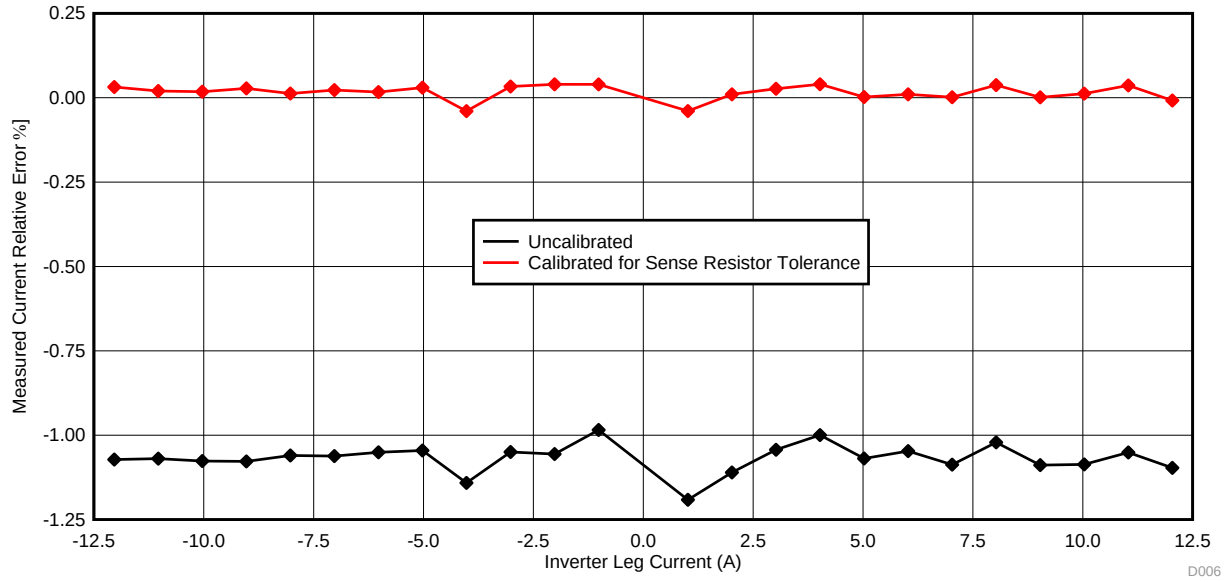


Figure 51. Relative Error [%] in Measured Inverter Leg Current From Amplifier Output Voltage

2.2.2.10 Overcurrent Protection

As explained in Section 1.4.2.2 and Section 1.4.8, the overcurrent protection is implemented by using the window comparator of the INA303 for inverter leg overcurrent detection and using TLV1701 for the DC bus overcurrent detection.

Overcurrent protection with DC bus current sensing and TLV1701:

The single-shunt amplifier output is connected to the comparator TLV1701 to detect overcurrent in DC bus. Figure 52 shows the overcurrent detection by the TLV1701 device. The overcurrent is set to 9 A by adjusting the threshold limit. The response time of the overcurrent detection is less than 1.5 µs (as Figure 53 shows), which is fast enough to protect an IGBT (IGBTs typically have more than a 5-µs short-circuit capability). The lowest propagation delay of the gate driver enables the fast turnoff of the IGBTs during an overcurrent event.

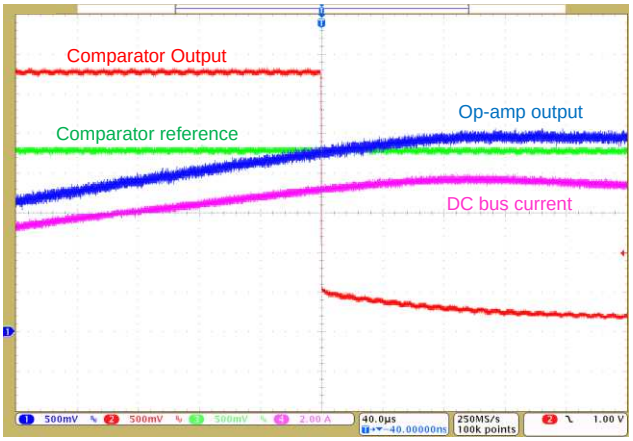


Figure 52. Overcurrent Detection by TLV1701 at a DC Bus Current of 9-A

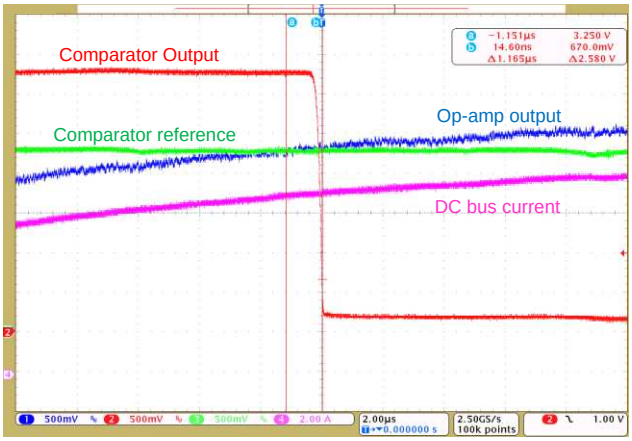


Figure 53. Response Time of Over current Protection by TLV1701 at 9-A

Overcurrent protection with inverter leg current sensing:

As explained in Section 1.4.2.2, the inverter leg overcurrent protection is implemented by using the window comparator of the INA303 device.

Overcurrent detection during positive polarity inverter leg current:

Figure 54 shows the overcurrent detection by the window comparator of the INA303 device for a positive inverter leg current (positive polarity inverter current refers to negative polarity winding current). Figure 55 shows the response time for overcurrent detection. The overcurrent is set to 9 A by configuring the INA303 comparator.

A 31.6-k resistor is used to set the overcurrent threshold for positive current.

- Set current limit voltage = (31.6 k × 80 µA) = 2.528 V
- Set current limit = (2.528 – V_{REF}) / (20 × 0.005) = 9 A; V_{REF} = 1.628 V
- Observed current Limit = 8.96 A

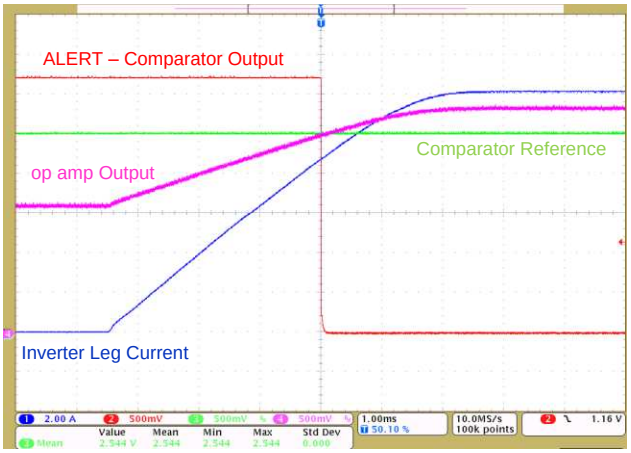


Figure 54. Overcurrent Detection by Window Comparator of INA303 for Positive Inverter Leg Current

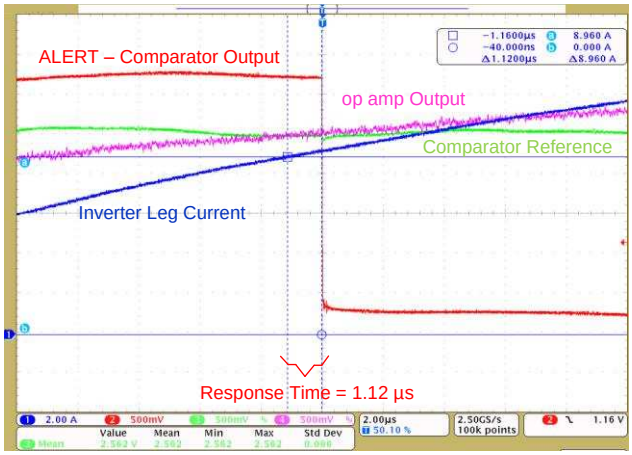


Figure 55. Response Time of Window Comparator of INA303 for Positive Inverter Leg Current

Overcurrent detection during negative polarity inverter leg current:

Figure 56 shows the overcurrent detection by the window comparator of INA303 for negative inverter leg current (negative polarity inverter current refers to positive polarity winding current). Figure 57 shows the response time for overcurrent detection. The overcurrent is set to –9 A by configuring the INA303 comparator.

A 9.09-k resistor is used to set the overcurrent threshold for negative current.

- Set current limit voltage = (9.09 k × 80 µA) = 0.7272 V
- Set current limit = (0.7272 – VREF) / (20 × 0.005) = –9.008 A; VREF = 1.628 V
- Observed current Limit = –8.68 A

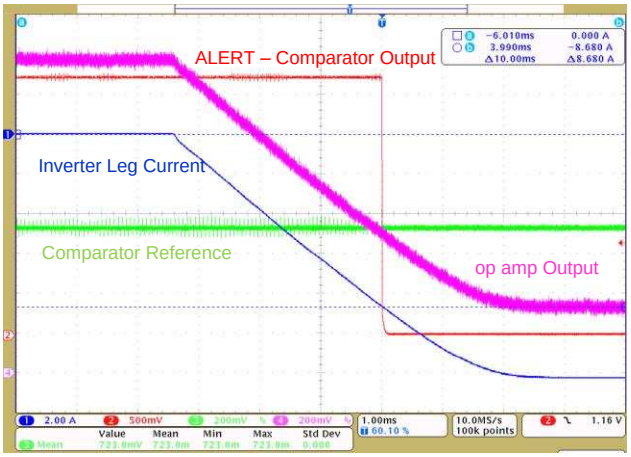


Figure 56. Overcurrent Detection by Window Comparator of INA303 for Negative Polarity Inverter Leg Current

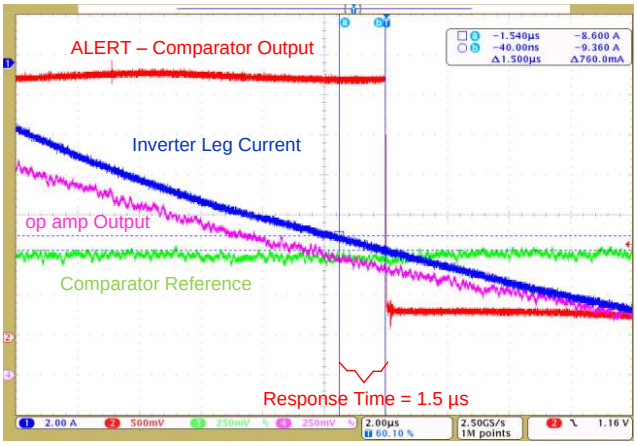


Figure 57. Response Time of Window Comparator of INA303 for Negative Polarity Inverter Leg Current

The response time of the overcurrent detection is less than 1.5 µs in both current polarities, which is fast enough to protect an IGBT (IGBTs typically have more than a 5-µs short-circuit capability). The lowest propagation delay of the gate driver enables the fast turnoff of the IGBTs during an overcurrent event.

2.2.2.11 Two- and Three-Shunt Current Sensing Over PWM Cycle

Figure 58 shows the current sense amplifier output with winding current. The peak winding current is approximately 4 A. The amplifier output voltage is inverted compared to the winding current because the inverter leg shunt voltage has a positive polarity when the bottom IGBT is conducting, which occurs during the negative winding current. If the designer wants to have the same polarity for the amplifier output and the winding current, the inverting and non-inverting input connection to the INA303 differential amplifier can be reversed. Figure 59 shows the performance of the inverter leg current sensing over a space vector PWM cycle. The fast response of the INA303 enables more than enough window for ADC sampling and helps to achieve the extreme duty cycles in a dual-shunt FOC.

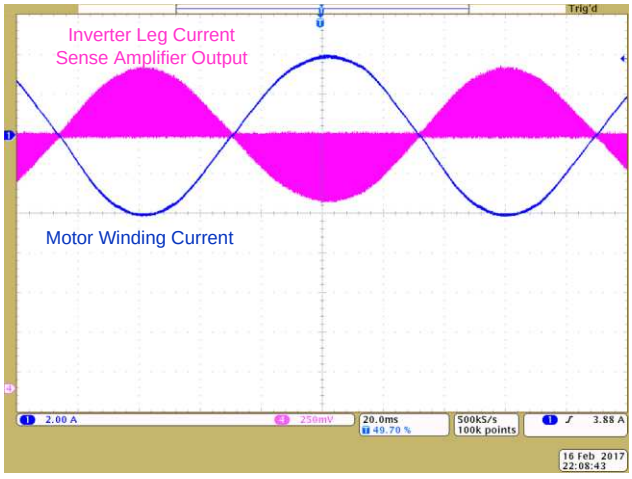


Figure 58. Inverter Leg Current Sense Amplifier Output With Winding Current

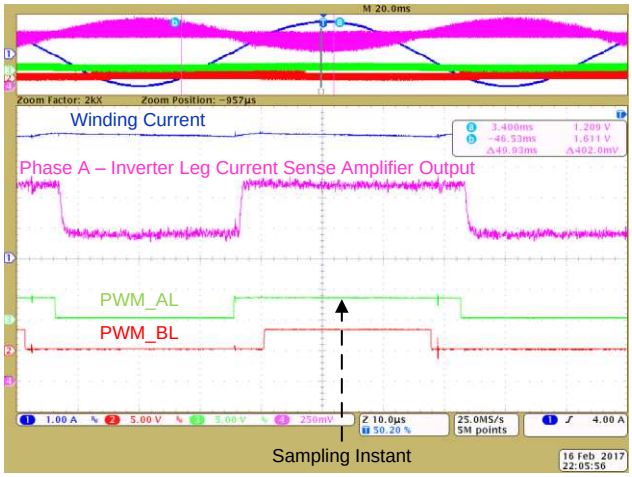


Figure 59. Inverter Leg Current Sense Amplifier Output Over a Space Vector PWM Cycle Modulation

3 Design Files

3.1 Schematics

To download the schematics, see the design files at TIDA-00778.

3.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00778.

3.3 PCB Layout Recommendations

Use the following layout recommendations when designing the current sense layout.

- Use Kelvin connection for the sense resistor placement and sense voltage routing.
- The sense voltage signal connection to the amplifier must be connected using a symmetric differential trace routing.
- The recommended placement of the low-pass RC filter at the output of the amplifier is near the MCU.
- The recommended placement of the current sense amplifier input filter is close to the op amp.

3.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-00778.

3.4 Altium Project

To download the Altium project files, see the design files at TIDA-00778.

3.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00778.

3.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00778.

4 Software Files

To download the software files, see the design files at MotorWare™ Software.

5 Related Documentation

1. Texas Instruments, *UCC27714 High-Speed, 600-V High-Side Low-Side Gate Driver with 4-A Peak Output*, UCC27714 Datasheet (SLUSBY6)
2. Texas Instruments, *InstaSPIN-FOC™ and InstaSPIN-MOTION™*, User's Guide (SPRUHJ1)
3. Texas Instruments, *Space-Vector PWM With TMS320C24x/F24x Using Hardware and Software Determined Switching Patterns*, Application Report (SPRA524)
4. Texas Instruments, *Reference Design for Reinforced Isolation Three-Phase Inverter With Current, Voltage, and Temp Protection*, TIDA-00366 Reference Design (TIDUBX1)
5. Texas Instruments, *48V 3-Phase Inverter with Shunt-based In-line Motor Phase Current Sensing Reference Design*, TIDA-00913 Reference Design (TIDUCE8)
6. Texas Instruments, *Three phase current measurements using a single line resistor on the TMS320F240*, TMS320F240 White Sheet (BPRA077)

5.1 Trademarks

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6 Terminology

FET— Field-effect transistor

IGBT— Insulated gate bipolar transistor

MCU— Microcontroller unit

MOSFET— Metal–oxide–semiconductor field-effect transistor

PWM— Pulse-width modulation

PMSM— Permanent magnet synchronous motor

RMS— Root mean square

RPM— Rotation per minute

SVM— Space vector modulation

7 About the Author

MANU BALAKRISHNAN is a systems engineer at Texas Instruments where he is responsible for developing subsystem design solutions for the Industrial Motor Drive segment. Manu brings to this role his experience in power electronics and analog and mixed signal designs. He has system level product design experience in permanent magnet motor drives. Manu earned his bachelor of technology in electrical and electronics engineering from the University of Kerala and his master of technology in power electronics from National Institute of Technology Calicut, India.

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