Design Guide: TIDA-020088

8-Channel, 1kVA, Class-H Audio Amplifier Reference Design

Description

This reference design demonstrates a 1kVA Class-H audio and tracking power supply audio subsystem. The TAS6684-Q1 audio amplifier tracks the envelope of the digital audio input and adjusts the LM5125A-Q1 boost output voltage to meet the power efficiency requirements without the need for an external microcontroller. This design leads to improved efficiency, thermal performance, and a smaller total footprint. In addition, this reference design allows for a Class-H implementation to be plug-and-play with minimal software changes to the rest of the automotive audio architecture.

Resources

TIDA-020088	Design Folder
LM5125A-Q1	Product Folder
TAS6684-Q1	Product Folder
MSPM0G3507-Q1	Product Folder
LM74700-Q1	Product Folder

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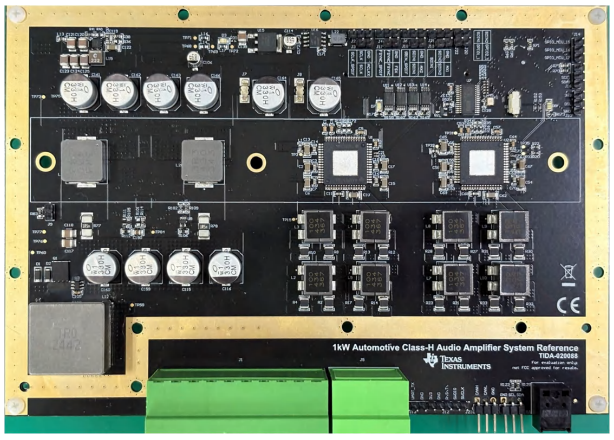
Features

- TAS6684-Q1 is a 45V automotive Class-D audio amplifier with integrated current sense and integrated Class-H control
- Maximum output power and high-fidelity audio
- LM5125A-Q1 is a wide-V_{IN} dual-phase synchronous boost controller with a ATRK/DTRK pin for simplified tracking power-supply design
- Self-contained Class-H control allows for simplified implementation in external amplifier applications and minimizes the need for additional digital power controller or software
- Includes an input protection circuit to protect against external transients, reverse battery conditions, and system overcurrent events

Applications

- Boosted audio amplifier with ANC



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1 System Description

In a premium automotive audio system, there is a demand for high speaker channel counts at higher power levels for a more immersive listening experience. This includes a wide array of tweeters, woofers, and subwoofers all with unique dynamic requires that frequently change depending on the audio source.

The automotive audio system is typically powered by Class-D audio amplifiers due to the efficiency advantages. With higher power level requirements leads to increased power supply voltage requirements for the amplifier, which is typically handled with a boost converter. The boost converter provides a constant output voltage (PVDD) to the audio amplifier. The audio amplifier output voltage and PVDD are shown in Figure 1-1.

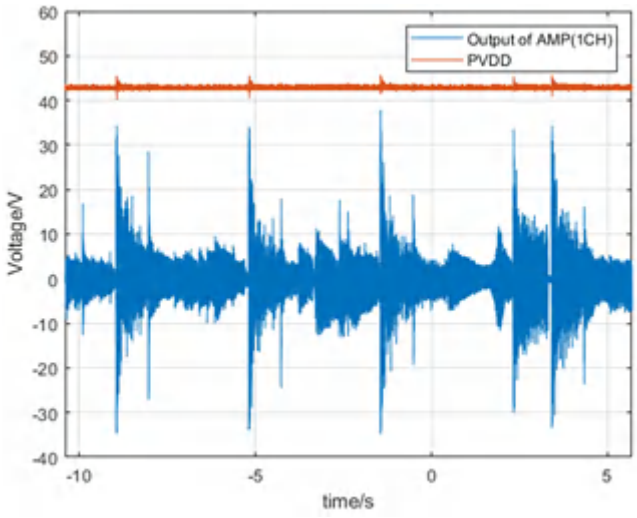

Figure 1-1. Audio Amplifier Output Voltage and PVDD

As shown in Figure 1-1, the music typically only needs this maximum voltage for short moments. However, high peak audio amplifier output voltage determines a high PVDD. High supply voltage leads to high switching loss and low efficiency at low power. An efficiency comparison of TAS6684-Q1 audio amplifier switching at 480kHz with different PVDD is shown in Figure 1-2. There is around 15 percentage points efficiency improvement at 40W from 45V PVDD to 14.4V PVDD.

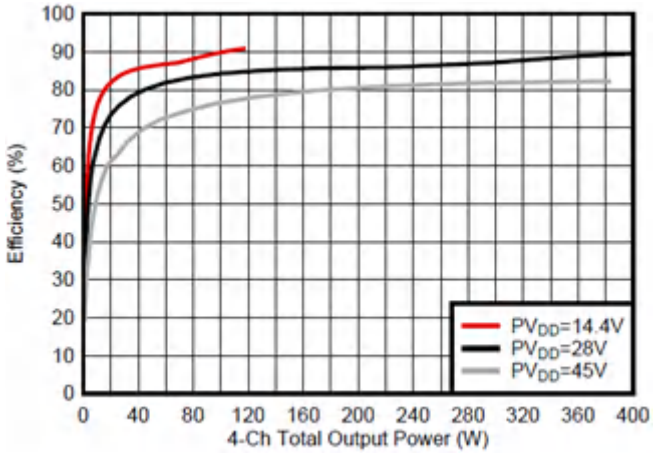

Figure 1-2. TAS6684 Efficiency vs. Output Power

The total system must be designed for this maximum power use-case and suffers in thermal performance and system efficiency. This leads to larger heat sinks, inductors, MOSFETs, and copper area on the system to handle the increased thermal load.

By introducing the concept of audio envelope tracking, we can dynamically control the boost converter voltage to provide just enough headroom for the audio waveform for any specific moment in time. The PVDD and

audio amplifier output voltage of the Class-H system are shown in Figure 1-3. The entire system operates to directly match the needs of the audio signal at all times instead of only maintaining the voltage required at the maximum power use-case. Power losses in the system are reduced and power efficiency and thermals improve significantly.

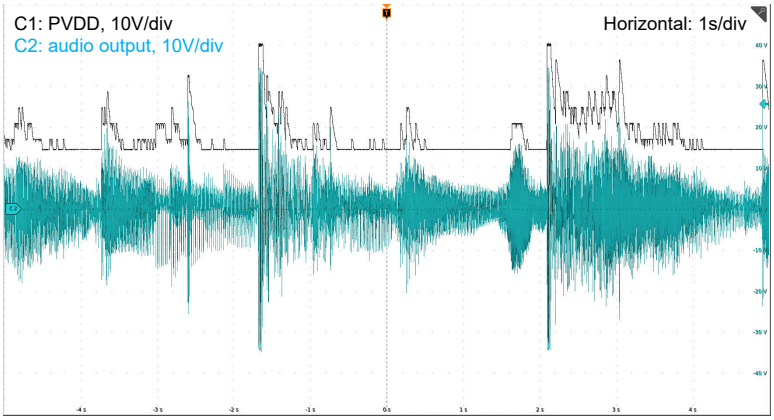

Figure 1-3. Class-H Operating Waveform

The Class-H tracking power supply system is shown in Figure 1-4. The audio signal sent to the audio amplifier is analyzed to determine the required PVDD voltage at a given moment in the audio stream. A PWM signal is sent to the boost converter to adjust PVDD voltage.

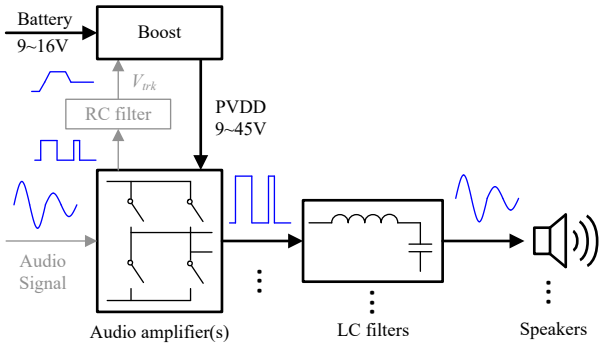

Figure 1-4. Simplified Class-H Audio Amplifier System Block Diagram

Figure 1-5 showcases the integrated Class-H features of the TAS6684-Q1. Utilizing the integrated DSP, the TAS6684-Q1 can track the envelope of the incoming audio stream and send a signal to the LM5125A-Q1 boost converter to adjust the PVDD voltage. This function is self-contained within these two devices. No additional monitoring of the audio signal or external control of the boost converter from a microcontroller is necessary.

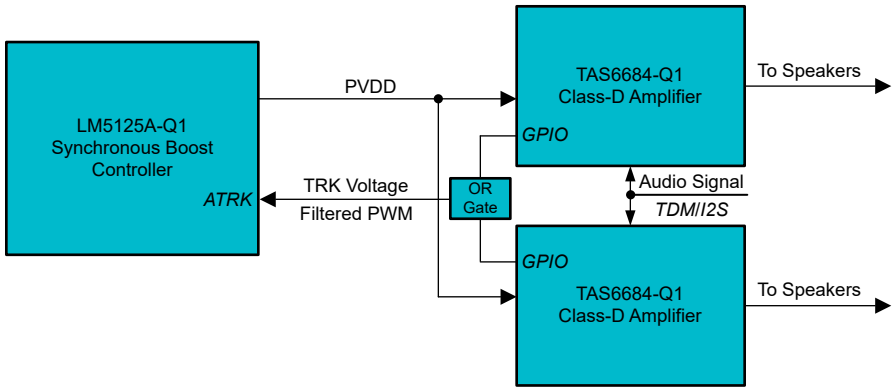

Figure 1-5. Simplified Class-H System With TAS6684-Q1 and LM5125A-Q1

This self-contained system provides design flexibility to an automotive audio system designer. External amplifiers can operate as more of a “plug-and-play” system rather than one that needs monitoring and control from a remote module (like a head unit or radio tuner) to calculate the audio envelope and control the power supply. Different automotive fleet variants with different audio system requirements do not need significant changes to the delivery of the audio data to the external amp or new software variants for different Class-H envelope tracking needs.

The implementation of Class-H power control in Figure 1-5 also provides several other key benefits at the system level, such as:

- Smaller boost inductor due to lower inductor loss
- Smaller heat sink for the TAS6684-Q1 Class-D amplifier due to lower loss
- Less copper thermal relief area on the PCB due to lower loss in the system
- Improved EMI performance due to lower switch-node voltage leading to lower electromagnetic energy

1.1 Key System Specifications

Table 1-1. Key System Specifications of the Boost Converter

PARAMETER	VALUE
Minimum input voltage, V_{in_min}	9V
Typical input voltage, V_{in_typ}	14.4V
Maximum input voltage, V_{in_max}	16V
Minimum output voltage, V_{out_min}	8V
Maximum output voltage, V_{out_max}	40V
Maximum output power at maximum output voltage and typical input voltage, P_{out_total}	1200W
Average current output power, P_{rated_total}	300W
Maximum delay at twice rated output power and typical input voltage, t_{delay}	100ms
Estimated efficiency, η	95%

Table 1-2. Key System Specifications of the Audio Amplifier

PARAMETER	VALUE
Total Channels	8
Speaker Load	4Ω
Total Peak VA of the output	1kVA
Continuous output power	300W rms

2 System Overview

2.1 Block Diagram

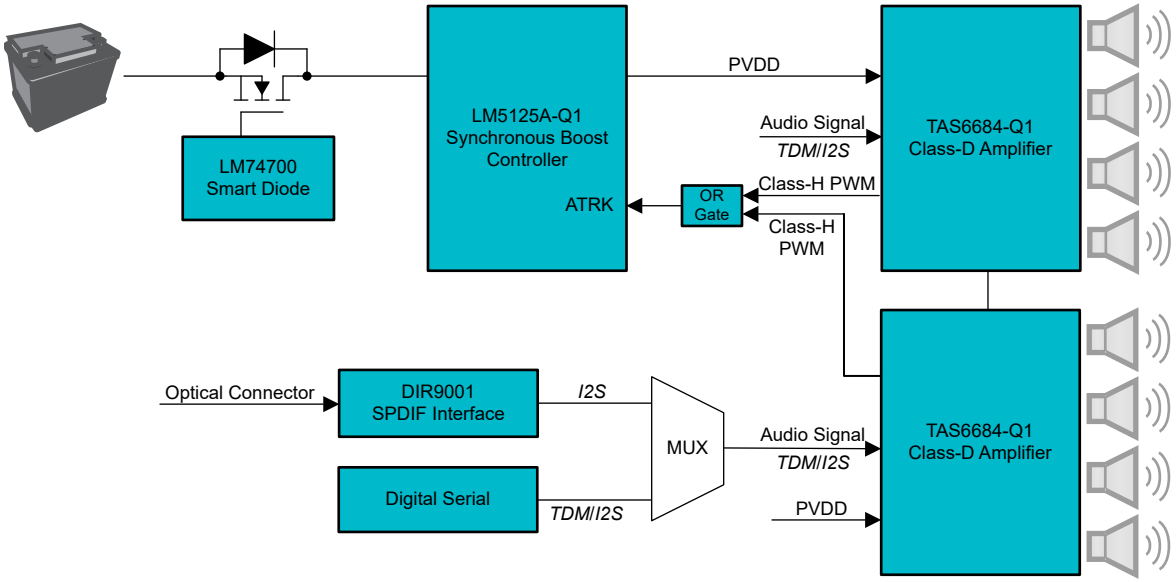

Figure 2-1. TIDA-020088 Block Diagram

2.2 Design Considerations

Figure 2-2 shows the power tree and the audio stream.

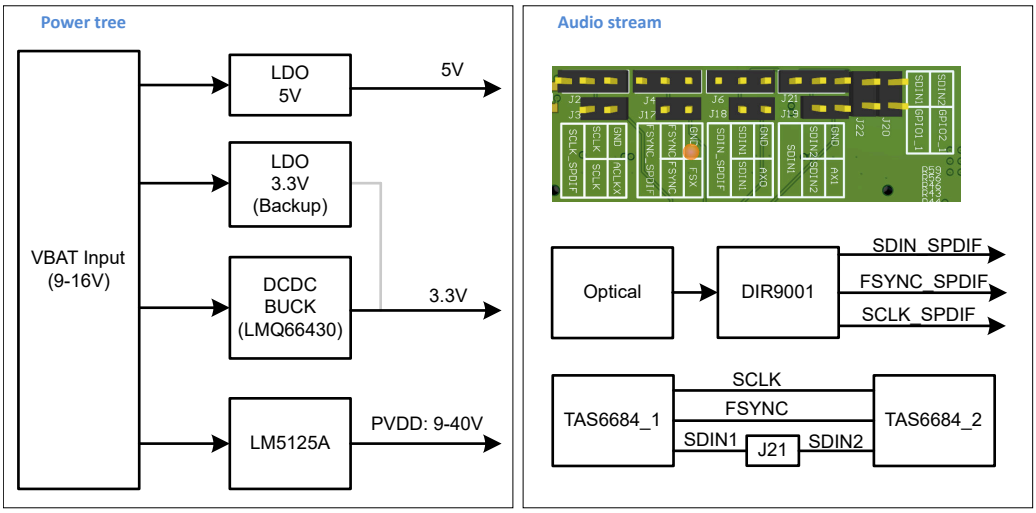

Figure 2-2. Power Tree and Audio Stream

2.3 Highlighted Products

2.3.1 TAS6684-Q1

The TAS6684-Q1 is a four-channel, digital-input, high voltage, Class-D audio amplifier that supports up to 45V supply voltage. Combined with up to 13A output current, this device delivers maximum output power and high-fidelity audio in high and low impedance loads. The device provides four channels at 118W (45V, 8Ω, 1% THD, BTL) and 218W (45V, 4Ω, 1% THD, BTL).

The TAS6684-Q1 integrates DC and AC load diagnostics to determine the status of the connected loads before enabling the output stage. During audio playback, the status can be monitored through the output current sense

and temperature of each channel which is available for each channel and reports the measurement to a host processor through TDM with minimal delay. The device monitors the output load condition while playing audio using real-time load diagnostics which operate independently from the host and audio input.

To optimize system efficiency, the integrated DSP of the TAS6684-Q1 enables Class-H envelope tracking control, eliminating the need for the development of complex tracking software and making local boost voltage control possible without the need for an external microcontroller.

The TAS6684-Q1 device features an additional low-latency signal path for each channel, providing up to 70% faster signal processing at 48kHz and support an audio signal path latency of < 100us at 96kHz sample rate, which enables time-sensitive Active Noise Cancellation (ANC), Road Noise Cancellation (RNC) applications.

2.3.2 LM5125A-Q1

The LM5125A-Q1 is a dual-phase, synchronous boost controller intended for high power audio application. The control method is based upon peak-current-mode control. Current-mode control provides inherent line feed forward, cycle-by-cycle current limiting, and ease of loop compensation.

The LM5125A-Q1 supports 6V to 60V output voltage. The output voltage can be dynamically programmed using ATRK/DTRK function. An internal charge pump allows 100% duty cycle for high-side switch (bypass operation). The switching frequency is programmable up to 2.2MHz.

Higher efficiency is achieved by two 5V MOSFET gate drivers with selectable deadtime. A user-selectable diode-emulation mode also enables discontinuous-mode operation for improved efficiency at light load conditions.

An average current limit loop (ILIM/IMON) is integrated. The loop allows high peak power for a short time and keeps the average power low. A phase shifted clock output enables easy multiphase interleaved configuration.

Additional features include low quiescent current, OVP, thermal shutdown, frequency synchronization, power good and adjustable line undervoltage lockout.

2.3.3 MSPM0G3507-Q1

The MSPM0G3507-Q1 is an AEC-Q100 compliant automotive-grade MCU powered by an 80MHz 32-bit Arm® Cortex®-M0+ core with MPU, boasting 128KB ECC flash and 32KB parity SRAM for reliable performance, and it meets ISO 26262 ASIL B functional safety standards with dual windowed watchdogs, comprehensive fault detection and TÜV certification. It integrates high-performance analog peripherals including two 4Msps 12-bit SAR ADCs, zero-drift chopper op-amps, a 12-bit 1Msps DAC, configurable VREF and high-speed comparators, plus programmable analog routing for flexible mixed-signal design. For digital and connectivity needs, it offers rich interfaces like CAN FD, LIN/IrDA/DALI-enabled UARTs, I2Cs and SPIs, along with 22 PWM channels with dead-time control, QEI/general-purpose timers, a trigonometric math accelerator, 128/256-bit AES encryption with TRNG and a 7-channel DMA controller for efficient control and secure communication. Operating over -40°C to 125°C with a 1.62V-3.6V supply voltage, it features ultra-low power modes and up to 60 5V-tolerant GPIOs in compact packages, ideal for space-constrained automotive safety-critical and mixed-signal applications.

3 System Design Theory

3.1 Boost Output Capacitance and Maximum Output Voltage

Figure 3-1 shows a Class-H audio amplifier operating waveform including the audio input, audio output and boost output voltage (PVDD). To avoid audio output clipping, the boost maximum output voltage must be higher than the maximum output voltage of the audio amplifier by a certain margin.

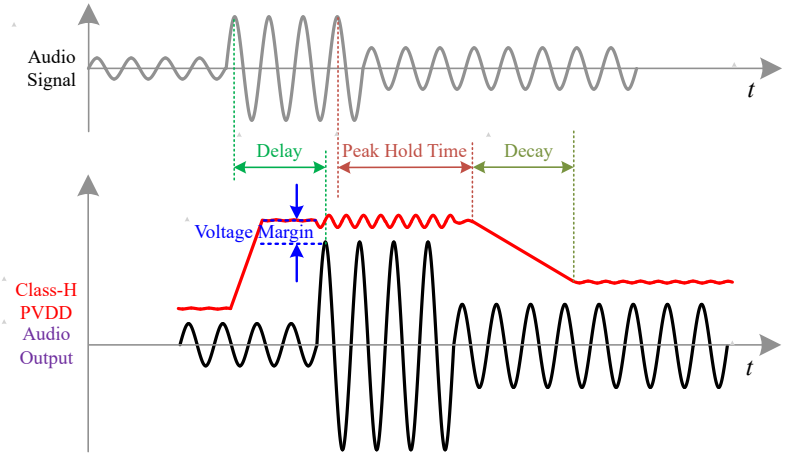

Figure 3-1. Class-H System Operating Waveform

Figure 3-2 shows the average audio amplifier output voltage $v_{ao}(t)$, output current $i_{ao}(t)$, output power $p_a(t)$ and input current $i_{ai}(t)$. A pure resistor R_{sp} is used as the worst-case model of the speaker. The waveform is an average waveform within the audio frequency range. The TAS6684-Q1 switching frequency is much higher than the audio frequency and is therefore ignored.

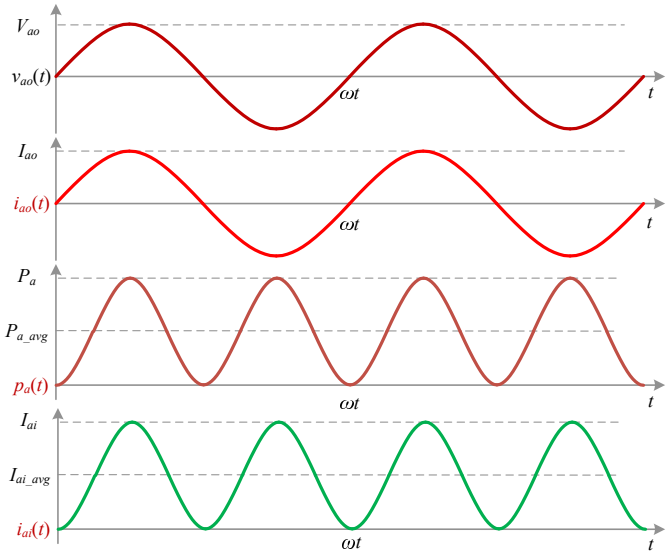

Figure 3-2. Average Audio Output and Input Waveform

The audio output voltage $v_{ao}(t)$ is express as,

$$v_{ao}(t) = V_{ao}\sin \omega t \quad (1)$$

where V_{ao} is the speaker maximum output voltage.

The audio output power $p_a(t)$ can be found as,

$$p_a(t) = \frac{V_{ao}^2}{R_{sp}} \cdot \frac{1 - \cos 2\omega t}{2} \quad (2)$$

Equation 2 shows that the audio amplifier average power P_{a_avg} is half of the peak power, and the frequency of the audio amplifier's output power is twice the frequency of the audio output voltage.

When R_{sp} and P_{a_avg} is defined, V_{ao} is obtained as,

$$V_{ao} = \sqrt{2 R_{sp} P_{a\_avg}} \quad (3)$$

The audio amplifier input current $i_{ai}(t)$ is expressed as,

$$i_{ai}(t) = \frac{V_{ao}^2}{R_{sp} V_{out}} \cdot \frac{1 - \cos 2\omega t}{2} \quad (4)$$

The audio amplifier peak input current can be found as,

$$I_{ai} = \frac{V_{ao}^2}{R_{sp} V_{out}} \quad (5)$$

Figure 3-3 shows a simplified model of boost and audio amplifier.

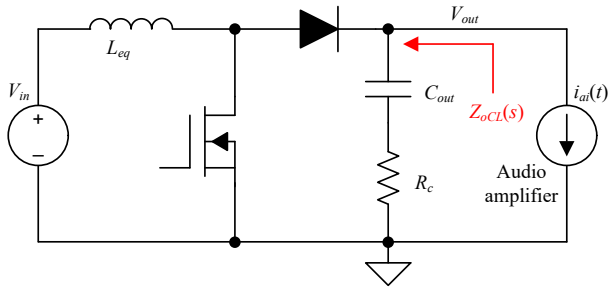

Figure 3-3. Simple Model of Boost and Audio Amplifier

The audio amplifier is simplified as a current source which is drawing 40Hz to 40kHz sine wave current from the boost output. C_{out} is the total boost output capacitance; R_c is the equivalent series resistance (ESR) of C_{out}. L_{eq} is the equivalent inductance of n_p phase boost,

$$L_{eq} = \frac{L_m}{n_p} \quad (6)$$

where L_m is the inductance of a single phase boost.

Considering output voltage ripple V_{out_pp}, voltage drop along the power path V_s and the output voltage tolerance V_t, the output voltage margin V_m can be expressed as,

$$V_m = \frac{V_{out\_pp}}{2} + V_s + V_t \quad (7)$$

where

$$V_{out\_pp} = I_{ai} \cdot |Z_{oCL}(s)| \quad (8)$$

$$V_s = I_{ao} R_s \quad (9)$$

Where $Z_{oCL}(s)$ is the closed-loop output impedance; R_s is the total resistance along the power path to the speaker. For a design with TAS6684, a good estimation of R_s is 0.25Ω. Audio amplifier internal power MOSFET $R_{ds\ (on)}$ is the main contributor to R_s.

The maximum value of $|Z_{oCL}(s)|$ should be used to for the worst output voltage ripple. A simple method is used to find the maximum value of $|Z_{oCL}(s)|$.

Figure 3-4 shows the approximate open-loop output impedance $|Z_{oOL}(s)|$. The impedance is determined by output capacitor impedance, which is,

$$Z_c(s) = \frac{1}{sC_{out}} + R_c \tag{10}$$

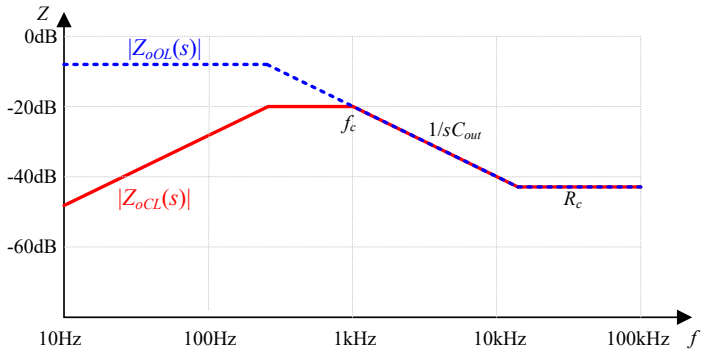

Figure 3-4. Open-Loop Output Impedance $|Z_{oOL}(s)|$ and Closed-Loop Output Impedance $|Z_{oCL}(s)|$

Figure 3-4 also shows the closed-loop output impedance $|Z_{oCL}(s)|$.

The relation between $Z_{oOL}(s)$ and $Z_{oCL}(s)$ can be obtained as:

$$Z_{oCL}(s) = \frac{Z_{oOL}(s)}{1 + T(s)} \tag{11}$$

At lower frequency ($f < f_c$) where $||T||>1$, $1+T\approx T$, the close loop output impedance is reduced by 1/T.

At higher frequency ($f > f_c$) where $||T||$ is small, $1+T\approx 1$, the output impedance is dominated by the output capacitor impedance.

From Figure 3-4, The maximum closed-loop output impedance can be obtained as,

$$Z_{oCL\_max} = \frac{1}{2\pi f_c C_{out}} \tag{12}$$

As f_c increases, the maximum closed-loop output impedance decreases. However, f_c is limited by the right-half-plane (RHP) zero in the boost converter transfer function.

The RHP zero frequency of a boost converter can be obtained as,

$$f_{RHPZ} = \frac{R_{out}(1-D)^2}{2\pi L_{eq}} \tag{13}$$

where D is the duty cycle of the boost converter; R_{out} is the equivalent load resistor.

In a boost with peak current limit, the maximum input current is relatively constant. Equation 13 can be written as,

$$f_{RHPZ} = \frac{V_{in}}{2\pi L_{eq} I_{in}} \tag{14}$$

where I_{in} the input current.

The minimum ω_{RHPZ} is found at V_{in_min} and I_{in_max},

$$f_{RHPZ} = \frac{V_{in\_min}}{2\pi L_{eq} I_{in\_max}} \tag{15}$$

The boost voltage loop crossover frequency f_c need to be less than 1/3 to 1/5 of the minimum RHP zero frequency. Here we select,

$$f_c = \frac{f_{RHPZ}}{5} \tag{16}$$

Substituting Equation 12, Equation 15 and Equation 16 into Equation 7, the output voltage margin V_m is found as,

$$V_m = \frac{I_{ai}}{2} \cdot \frac{5L_{eq}I_{in\_max}}{V_{in\_min}C_{out}} + I_{ao}R_s + V_t \tag{17}$$

The required boost output voltage at peak power is found as,

$$V_{out} = \sqrt{2R_{sp}P_{a\_avg}} + \frac{I_{ai}}{2} \cdot \frac{5L_{eq}I_{in\_max}}{V_{in\_min}C_{out}} + I_{ao}R_s + V_t \tag{18}$$

3.2 Peak Power of the Boost Converter

Define k as the ratio of the boost input peak power P_{in_pk} to the average power P_{in_avg},

$$k = \frac{P_{in\_pk}}{P_{in\_avg}} \tag{19}$$

The instantaneous audio amplifier power is shared between the boost power stage and the boost output capacitors. The boost output capacitors show lower impedance above f_c and share more power above f_c.

For $f < 0.1f_c$(including DC), almost all power comes from boost input.

The boost input peak power P_{in_pk} is twice average input power P_{in_avg}. That is, k = 2.

For $f > 10f_c$, the PVDD capacitors handle almost all the AC power. That is, k = 1.

For $0.1f_c < f < 10f_c$, k is between 1 and 2.

Figure 3-5 shows a bench result to support above analysis.

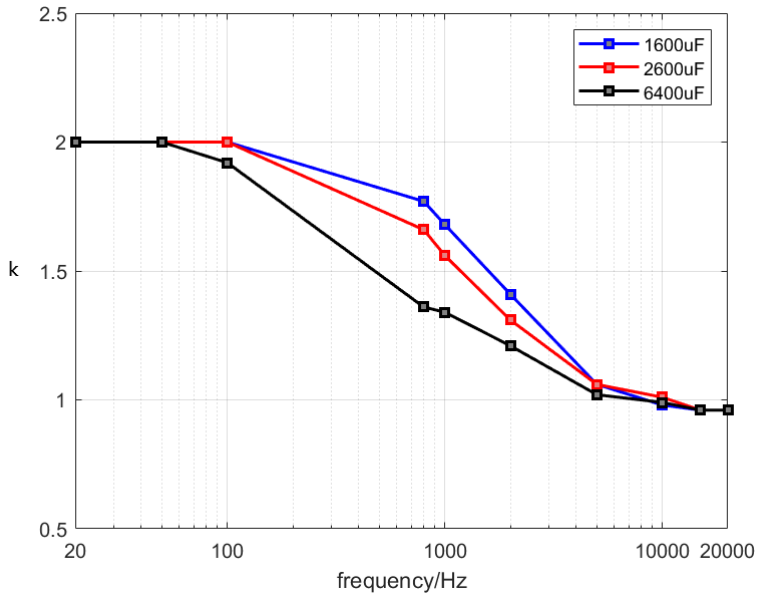

Figure 3-5. Bench Result of k versus Frequency

Table 3-1 shows the suggested k for different speaker types.

Table 3-1. Suggested k for different speaker types

Speaker Type	Frequency range	k
Woofer	20Hz-2kHz	2
Middle Range	250Hz-4kHz	1~2
Twitter	2kHz-20kHz	1

3.3 Ramp Time and Class-H delay

The boost output capacitance is typically higher than 1mF. The output voltage takes time to ramp up. The ramp time is limited by the boost output capacitance and the maximum input current of the boost converter.

The maximum input current I_{in_max} can be expressed by,

$$I_{in\_max} = I_{Lm\_pk} - I_{pp\_bias} \quad (20)$$

where I_{Lm_pk} is the peak current limit, $_{pp\_bias}$ is the inductor current ripple at peak current limit. For powder core inductor, the inductance decreases with increased DC bias current. This leads to higher ripple current at higher current.

When ramping from minimum output voltage (V_{in}) to the maximum output voltage, the ramp up time t_r is found from energy view,

$$t_r = \frac{C_{out}\left(V_{out}^2 - V_{in}^2\right)}{2\eta V_{in} I_{in\_max}} \quad (21)$$

where η is the efficiency of the boost converter. η=0.95 is a good starting point.

Select a Class-H delay that is higher than the ramp time.

3.4 Design of the Class-H Two Stage RC Filter

The TAS6684-Q1 provides a 384kHz Class-H PWM. The TAS6684-Q1's tracking GPIO supports two output modes: push-pull and open-drain.

Figure 3-6 shows a two stage RC filter to convert the PWM signal to an smooth analog voltage in push-pull mode. The filter is selected considering the ramp time on ATRK/DTRK.

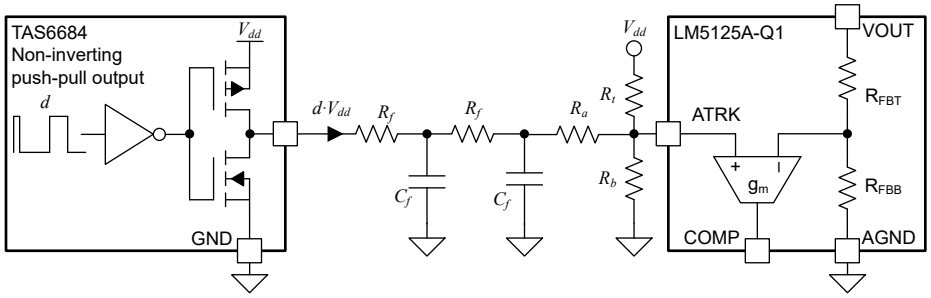

Figure 3-6. Two Stage RC Filter to ATRK/DTRK

100% PWM duty cycle sets the output voltage to V_{out_max} and 0% PWM duty cycle sets the output voltage to V_{out_min}. R_t and R_b are used to adjust ATRK/DTRK offset voltage.

The V_{trk_max} and V_{trk_min} is found as,

$$V_{ATRK\_max} = V_{dd}\frac{R_b}{(2R_f + R_a)\|R_t + R_b} \quad (22)$$

$$V_{ATRK\_min} = V_{dd}\frac{(2R_f + R_a)\|R_b}{(2R_f + R_a)\|R_b + R_t} \quad (23)$$

where V_{dd} is the amplitude of the PWM signal; d is the PWM duty cycle.

The AC transfer function from input to V_{ATRK} can be found as,

$$G_{trk}(s) = \frac{\frac{R_L}{2R_f + R_L}}{1 + 2\zeta\frac{s}{\omega_n} + \left(\frac{s}{\omega_n}\right)^2} \quad (24)$$

where

$$R_L = R_a + R_b \| R_t \quad (25)$$

$$\omega_n = \frac{1}{R_f \times C_f \sqrt{\frac{R_L}{2R_f + R_L}}} \quad (26)$$

$$\zeta = \frac{1}{2}\left(\frac{R_f}{R_L} + 3\right)\sqrt{\frac{R_L}{2R_f + R_L}} \quad (27)$$

The roots of the denominator are found as,

$$s_1 = -\zeta\omega_n + \omega_n\sqrt{\zeta^2 - 1} \quad (28)$$

$$s_2 = -\zeta\omega_n - \omega_n\sqrt{\zeta^2 - 1} \quad (29)$$

As ζ>1, this is an over damped second order system. s_1 is the dominate pole. 2% settling time t_s is estimated as,

$$t_s = \frac{1}{s_1} \cdot \ln\left(-\frac{0.02 \cdot 2s_1\sqrt{\zeta^2 - 1}}{\omega_n}\right) \quad (30)$$

3.5 Class-H Tracking with Multiple TAS6684-Q1s

For boost controllers without a tracking pin, connect the RC filter to the FB pin. In this case, however, a 100% PWM duty cycle sets the minimum output voltage and 0% PWM duty cycle sets the maximum output voltage. To make sure the tracking function works properly, select "inverting output" for the TAS6684-Q1 tracking GPIO.

Multiple TAS6684-Q1 devices can be synchronized via SCLK. The "OR" signal from multiple TAS6684-Q1 devices is the desired tracking PWM. Figure 3-7 shows the block diagram using an OR gate.

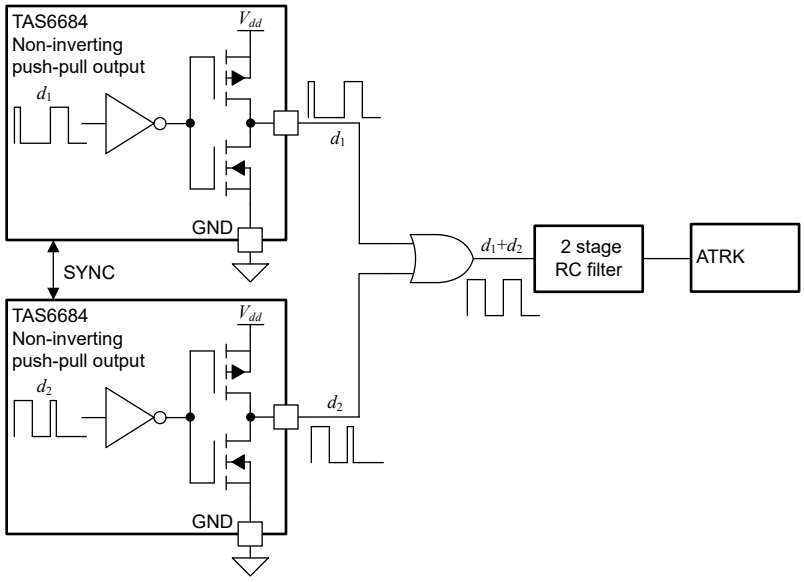

Figure 3-7. Class-H Tracking Using an OR gate with Two TAS6684-Q1s

The open-drain mode provides an "AND" signal by connecting the outputs of TAS6684-Q1 devices together. Figure 3-8 shows an "NOR" signal by connecting the outputs of two TAS6684-Q1 devices together. Note the TAS6684-Q1 outputs are set to inverting, open-drain mode. The "NOR" signal fits FB pin connection.

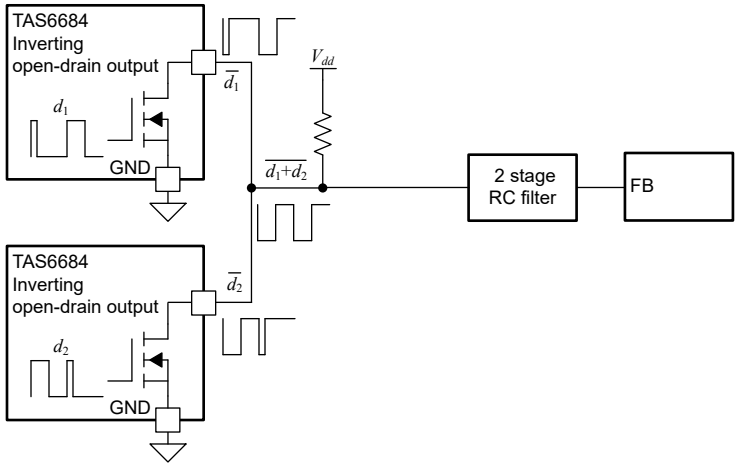

Figure 3-8. Class-H Tracking Connected to FB with Two TAS6684-Q1s

The "OR" signal can also be generated based on Figure 3-8. A "NOT" gate is inserted and the "OR" signal fits ATRK connection.

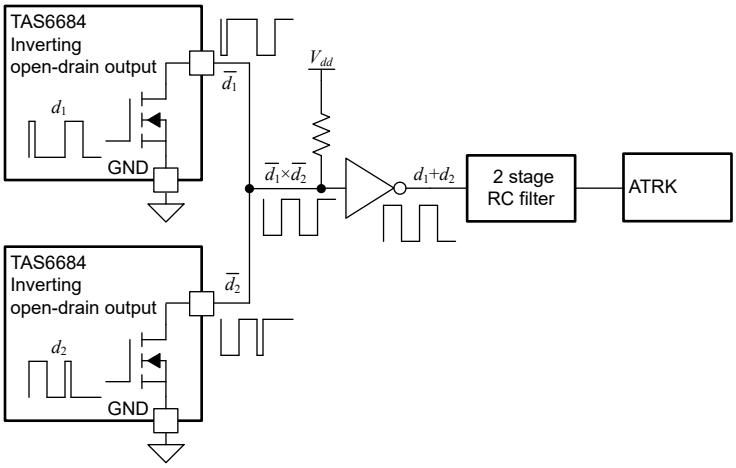

Figure 3-9. Class-H Tracking Connected to ATRK with Two TAS6684-Q1s

Figure 3-10 shows the PWM Tracking Signals (d_1 and d_2) and the "OR" signal (d_1+d_2).

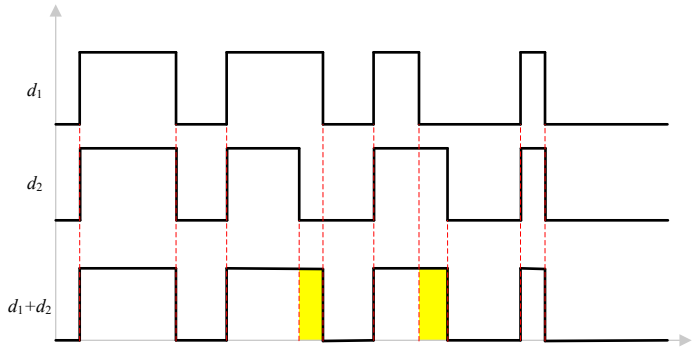

Figure 3-10. PWM Tracking Signals (d_1 and d_2) and the *OR* signal (d_1+d_2)

However, synchronization delay can occur between TAS6684-Q1s as shown in Figure 3-11. The worst-case delay is 325ns. The delay can increase the desired duty cycle by up to 325ns.

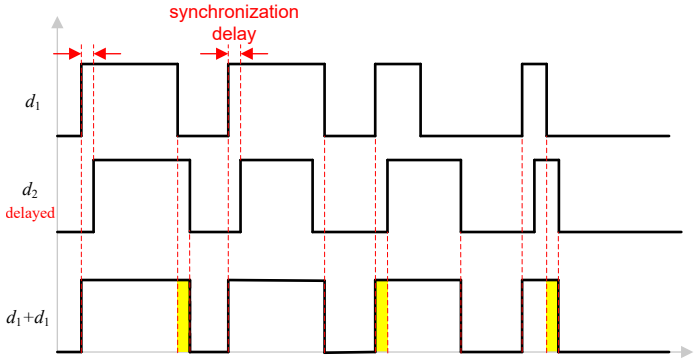

Figure 3-11. Synchronization Delay between TAS6684-Q1s

The TAS6684-Q1 Class-H tracking PWM has nine duty cycles: 0%, 12.5%, 25%, 37.5%, 50%, 62.5%, 75%, 87.5% and 100%. Table 3-2 shows the worst-case delay impact assuming multiple TAS6684-Q1s with the same duty cycle output and worst-case delay, and the maximum PVDD voltage is 40V and minimum PVDD voltage is 9V. At worst-case , the PVDD voltage can be approximately 4V higher than the PVDD voltage without delay.

Table 3-2. Worst-Case Delay Impact

Without Delay		**With Worst-Case Delay**		
Duty Cycle	PVDD / V	Pulse width / ns	Duty Cycle	PVDD / V

Table 3-2. Worst-Case Delay Impact (continued)

Without Delay		With Worst-Case Delay		
0.0%	9.00	0	0%	9.0
12.5%	12.88	650.52	25%	16.74
25%	16.75	976.04	37.5%	20.62
37.5%	20.63	1301.5	50%	24.49
50%	24.5	1627.0	62.5%	28.37
62.5%	28.38	1952.6	75%	32.24
75%	32.25	2278.1	87.5%	36.12
87.5%	36.16	2603.65	100%	39.99
100%	40	/	100%	40

3.6 TAS6684-Q1 Class-H Parameters

Figure 3-12 shows the TAS6684-Q1 Class-H DSP processing flow. The TAS6684-Q1 features a digital envelope tracking algorithm incorporating a delay buffer, which provides a look-ahead function to prevent audio clipping distortion. The internal DSP processes the input audio data and then outputs the tracking signal trough GPIO to adjust the boost converter output voltage. The look-ahead delay buffer supports audio signal tracking of up to 5ms, which is sufficient for most applications. Using the integrated Class-H algorithm instead of an external DSP reduces hardware costs and development time.

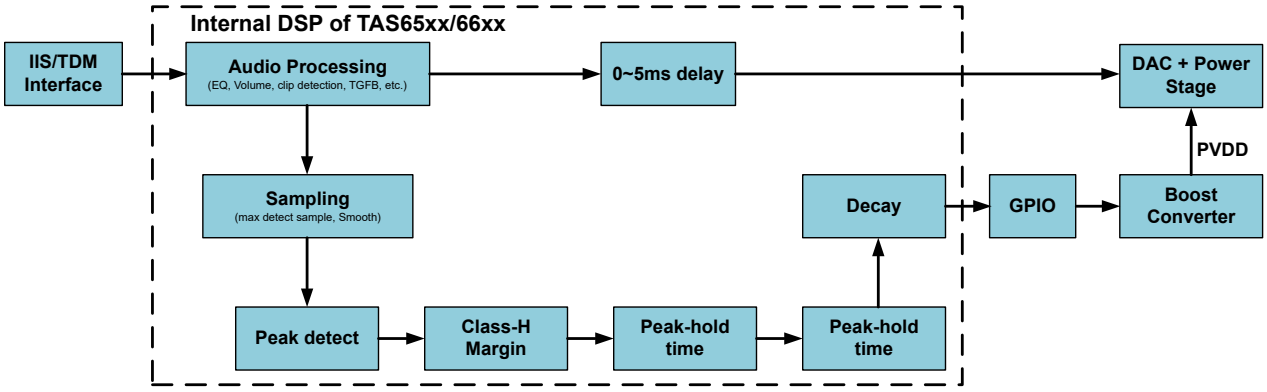

Figure 3-12. TAS6684-Q1 Class-H flow chart

Figure 3-13 illustrates the Class-H operating waveforms and marks some key parameters.

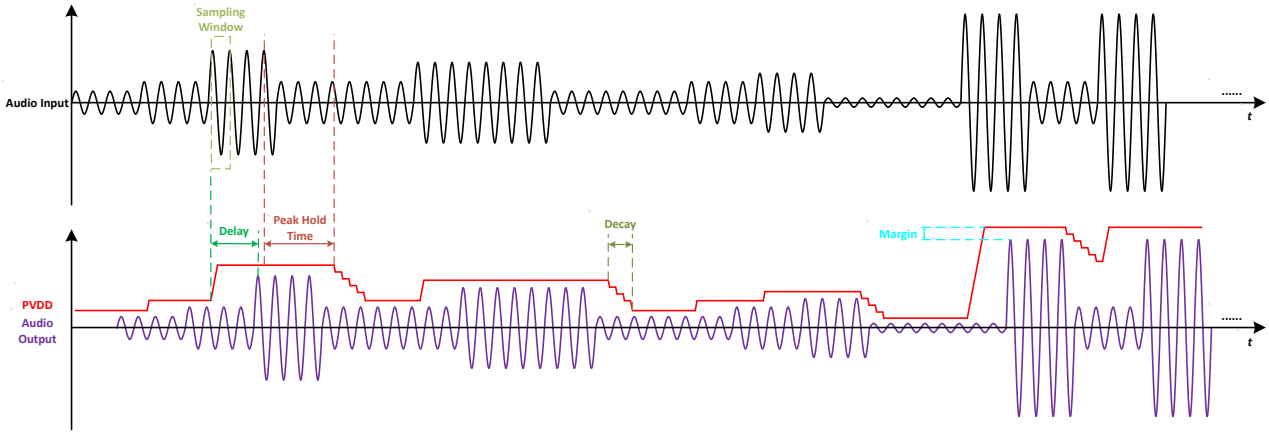

Figure 3-13. Class-H Operating Waveforms

The PPC3 GUI allows the customer to adjust some parameters according to different application scenarios. Figure 3-14 shows the recommended Class-H settings.

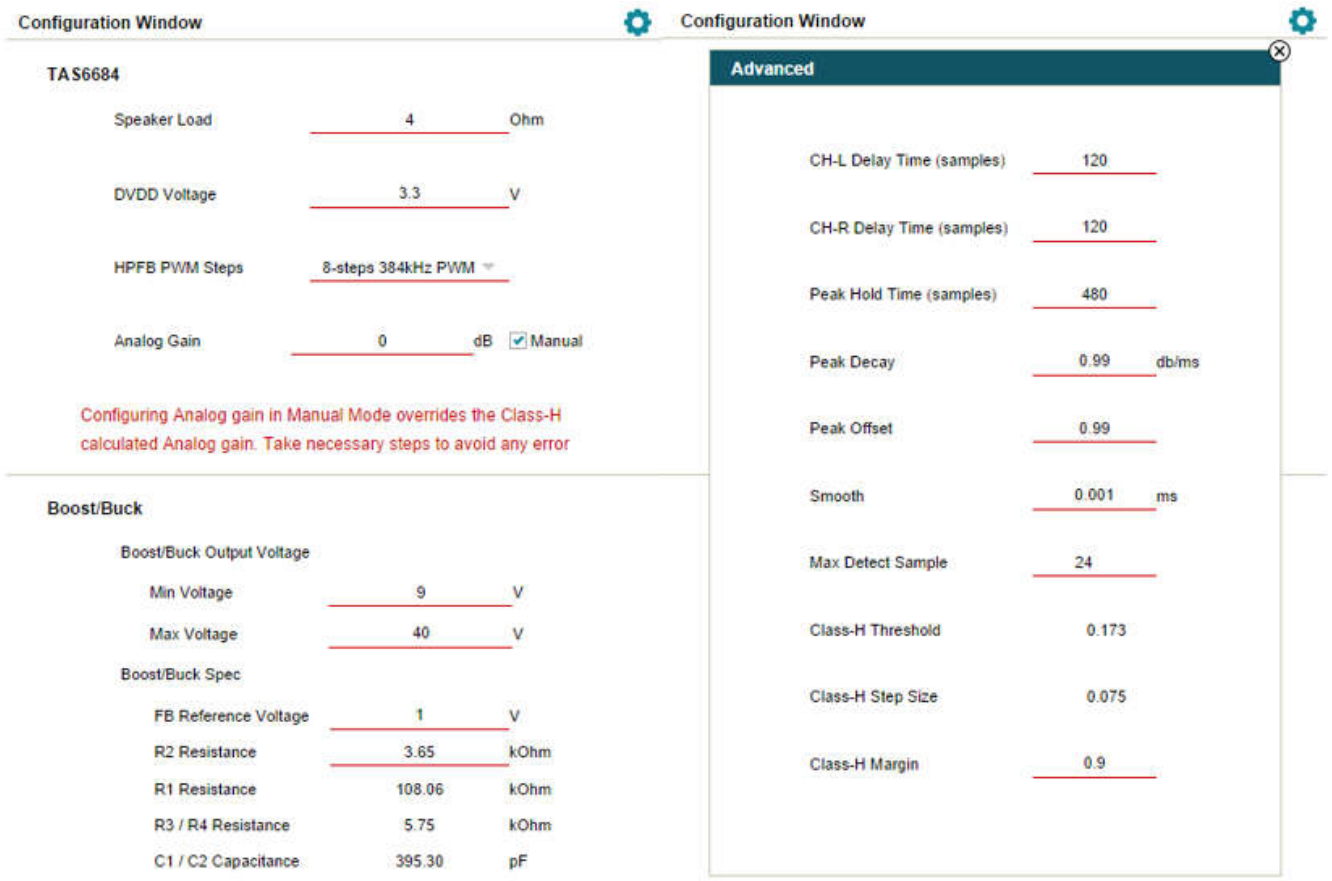

Figure 3-14. Recommended Class-H Settings

The parameters are explained below.

- Analog Gain

Adjust the Analog Gain according to the amplitude range of the output PVDD to avoid output clipping.

- Min Voltage and Max Voltage

Set minimum and maximum PVDD voltage. The internal DSP divides the output into nine levels linearly according to the set minimum and maximum PVDD voltage. The voltage of each level is calculated as follows,

$$V_{out} = PVDD_{min} + d \cdot (PVDD_{max} - PVDD_{min}) \quad (31)$$

where d is the duty cycle of Class-H tracking output, d = 0, 12.5%, 25%, … , 87.5%, 100%.

- Delay Time

Delay Time is selected considering the boost output voltage ramp time as discussed in Section 3.3.

$$\text{Delay time} = \frac{\text{Delay time setting*3}}{\text{sample rate}} \text{ ms} \quad (32)$$

- Peak Hold Time

Peak Hold Time refers to current Class-H max level hold time. When a peak signal is detected the hold counter begins to re-count and hold the PWM level. Hold time calculation formula shown as,

$$\text{Audio out Real delay time} = \frac{\text{Hold time setting}}{\text{sample rate}} \text{ ms} \quad (33)$$

- Peak Decay

Peak Decay refers to the decay rate of each level. This parameter controls how quickly the Class-H output level changes from high to low (non-inverting output). A smaller peak decay time means a faster PVDD voltage drop. in general, set the peak decay higher when the PVDD capacitor is large.

- Peak Offset

Peak Offset is a hysteresis which is a rate of Class-H trigger threshold. Keeping the default values is recommended.

- Smooth

Smooth time constant is the alpha smooth. This parameter enables a smooth transition from the initial PWM level to the final PWM level. When using an RC filter at Class-H PWM output as discussed in Section 3.4, set the smooth time to a very small value.

- Max Detect Samples

Max Detect Samples are the samples used during audio signal level detection.

$$\text{Max detect sample time} = \frac{\text{Max Detect Sample}}{\text{sample rate}}\ \text{ms} \tag{34}$$

- Class-H Margin

Class-H Margin is used to adjust the threshold and levels to make sure that the output margin is sufficient to prevent clipping. However, too much margin decreases the efficiency.

3.7 Design Parameters

Table 3-3 shows the quantity, average power of the speakers in the audio system. The k is selected based on Table 3-1.

Table 3-3. Quantity and Average Power of the Speakers

Speaker Type	Average Power	Quantity	k
Woofer	150W	2	2
Middle Range	80W	2	1.5
Twitter	40W	4	1

The peak power of the audio amplifier P_t can be found as,

$$P_t = 150\text{W} \cdot 2 \cdot 2 + 80\text{W} \cdot 2 \cdot 1.5 + 40\text{W} \cdot 4 \cdot 1 = 1\text{kW} \tag{35}$$

Knowing 150W average power of the 4Ω woofer, the maximum voltage across the woofer (V_{ao}) can be obtained from Equation 3,

$$V_{ao} = \sqrt{2R_{sp}P_{a\_avg}} = 34.6\text{V} \tag{36}$$

The woofer peak current I_{ao}can be found as,

$$I_{ao} = \frac{V_{ao}}{R_{sp}} = 8.7\text{A} \tag{37}$$

V_s can be found as,

$$V_s = I_{ao}R_s = 2.2\text{V} \tag{38}$$

Assuming V_{out_pp} = 2V, the minimal output capacitance can be found as,

$$C_{out} = I_{ai} \cdot \frac{5L_{eq}I_{in\_max}}{V_{in\_min}V_{out\_pp}} = 1060\mu\text{F} \tag{39}$$

where I_{ai} is the worst-case audio amplifier total input current which is estimated by P_t / V_{ao}.

Aluminum electrolytic capacitor is preferred due to low cost and high capacitance density. Considering the capacitance derating at low temperature, 6 pcs 330µF electrolytic capacitors are chosen.

Ceramic capacitors are mandatory to handle the current ripple and reduce the switching frequency voltage ripple. 18 pcs 10µF and 8 pcs 0.1µF ceramic capacitors are used. The 0.1µF ceramic capacitors are placed close to the MOSFETs following "vertical loop" concept. Refer to *Improve High-Current DC/DC Regulator EMI Performance for Free With Optimized Power Stage Layout* for more details.

Considering 2% settling error and 2% tolerance of the output voltage, the voltage margin needs to be higher than 4.8V from Equation 17. 40V maximum output voltage is selected. Minimum output voltage of 9V is selected. When the required output voltage is less than the input voltage, the boost enters bypass mode to further improve light load efficiency.

4 Hardware, Software, Testing Requirements, and Test Results

4.1 Hardware Requirements

Required hardware and accessories

- TIDA-020088 reference board
- Power Supply Unit (PSU) supporting 16V/80A
- 1-4 resistive loads or speaker loads
- USB-I2X board (refer to PCM186X EVM Users Guide)
- USB A male to micro B male cable
- Optical SPDIF cable or PSIA line (audio signal input)
- Desktop or laptop PC with Microsoft® Windows® 7, 8, or 10 operating system

4.2 Software Requirements

Required software

- PPC3 (PUREPATHCONSOLE)
- TAS6684 PPC3 GUI

4.3 Test Setup

4.3.1 Hardware Setup

Follow steps below:

1. Connect the power supply to connector J1. Make sure the input cable has a low impedance due to the high input current.
2. Connect the speaker loads to connectors J1 and J5.
3. Set the jumpers based on the audio input. When optical input is selected, follow Jumpers Settings for Optical Input. When external digital audio source such as Programmable Serial Interface Adapter (PSIA) from Audio Precision is selected, follow Table 4-2.

Table 4-1. Jumpers Settings for Optical Input

Jumper	Name	Optical
J2	SCLK_SPDIF, SCLK, GND	Connect SCLK_SPDIF and SCLK
J3	SCLK, ACLKX	OUT
J4	FSYNC_SPDIF, FSYNC, GND	Connect FSYNC_SPDIF and FSYNC
J6	SDIN_SPDIF, SDIN1, GND	Connect SDIN_SPDIF and SDIN1
J17	FSYNC, FSX	OUT
J18	SDIN1, AX0	OUT
J19	SDIN2, AX1	OUT
J20	SDIN2, GPIO2_1	IN
J21	SDIN1, SDIN2, GND	Connect SDIN1 and SDIN2
J22	SDIN1, GPIO1_1	IN

Table 4-2. Jumpers Settings for PSIA Input

Jumper	Name	PSIA (two SDIN lines)	PSIA (one SDIN line)
J2	SCLK_SPDIF, SCLK, GND	IN - SCLK	IN - SCLK
J3	SCLK, ACLKX	OUT	OUT
J4	FSYNC_SPDIF, FSYNC, GND	IN - FSYNC	IN - FSYNC
J6	SDIN_SPDIF, SDIN1, GND	IN - SDIN1	IN - SDIN1
J17	FSYNC, FSX	OUT	OUT
J18	SDIN1, AX0	OUT	OUT
J19	SDIN2, AX1	OUT	OUT
J20	SDIN2, GPIO2_1	Optional	Optional
J21	SDIN1, SDIN2, GND	IN - SDIN2	Connect SDIN1 and SDIN2

Table 4-2. Jumpers Settings for PSIA Input (continued)

Jumper	Name	PSIA (two SDIN lines)	PSIA (one SDIN line)
J22	SDIN1, GPIO1_1	Optional	Optional

The initialization code has been burned into the board, the board can be powered on with the default settings.

To change the settings manually, follow the extra steps below:

1. Connect GPIO_MCU_17 (J14) to GND. (When the MCU detects that the GPIO is pulled to ground, the MCU only pulls up the PDN and standby pins without performing other initialization operations.)
2. Connect the I2C port (J11) to USB-I2X board and connect USB-I2X board to PC through USB cable.

4.3.2 Software Setup

Open the PPC3 GUI, Figure 4-1 shows the startup window.

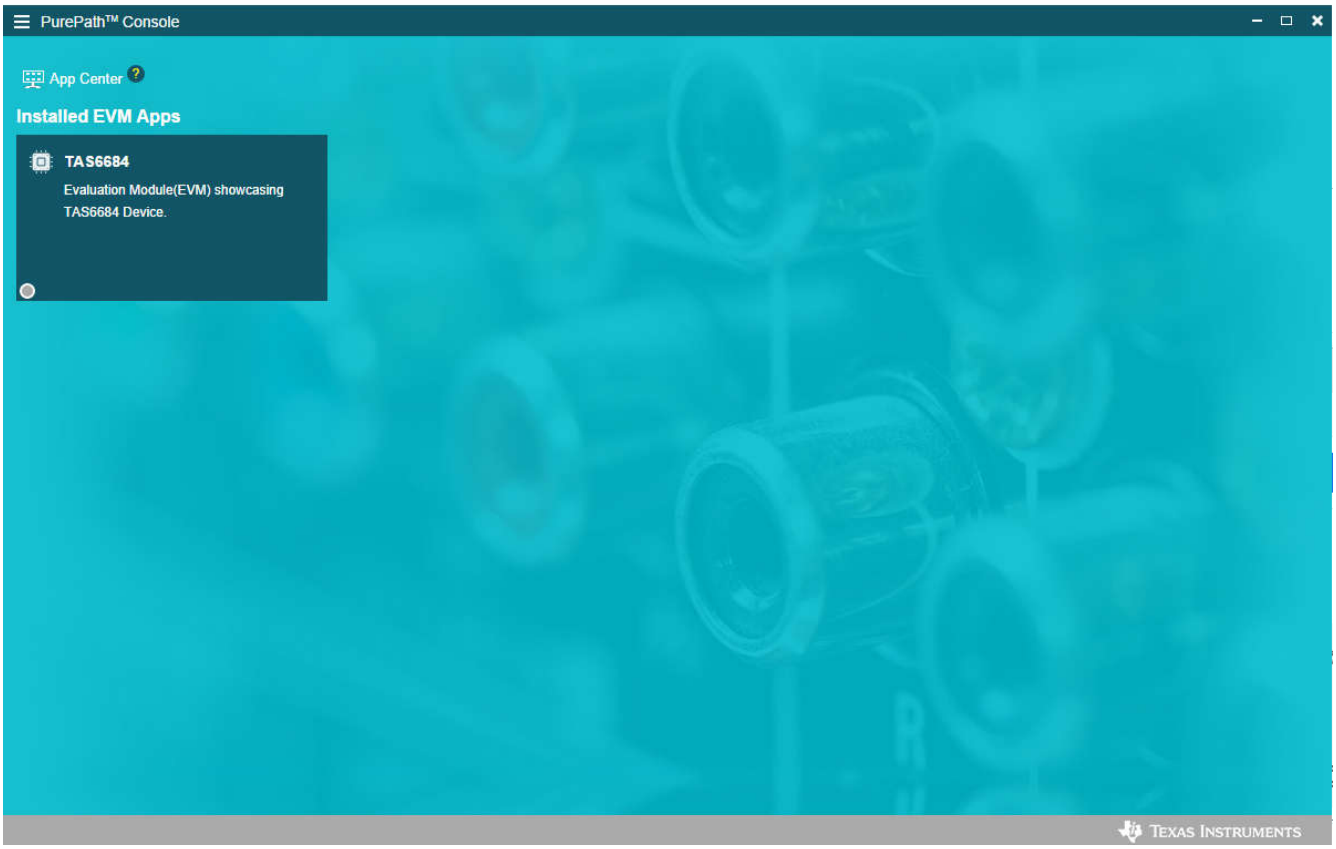

Figure 4-1. PPC3 Startup Window

If "TAS6684" does not appear in the startup window, follow below steps

1. Download TAS6684.tar.gz file.
2. Open the PPC3 software. (Need to sign out).
3. Choose “Open” button.
4. Choose “All Files” and then select the "TAS6684.tar.gz" to install.

Click on the dark green box labeled "TAS6684" in Figure 4-1. This opens the TAS6684 startup TAB. Then, set the audio input type, process flow, I2C address, GPIO settings, etc., and then click the "Apply Config" button.

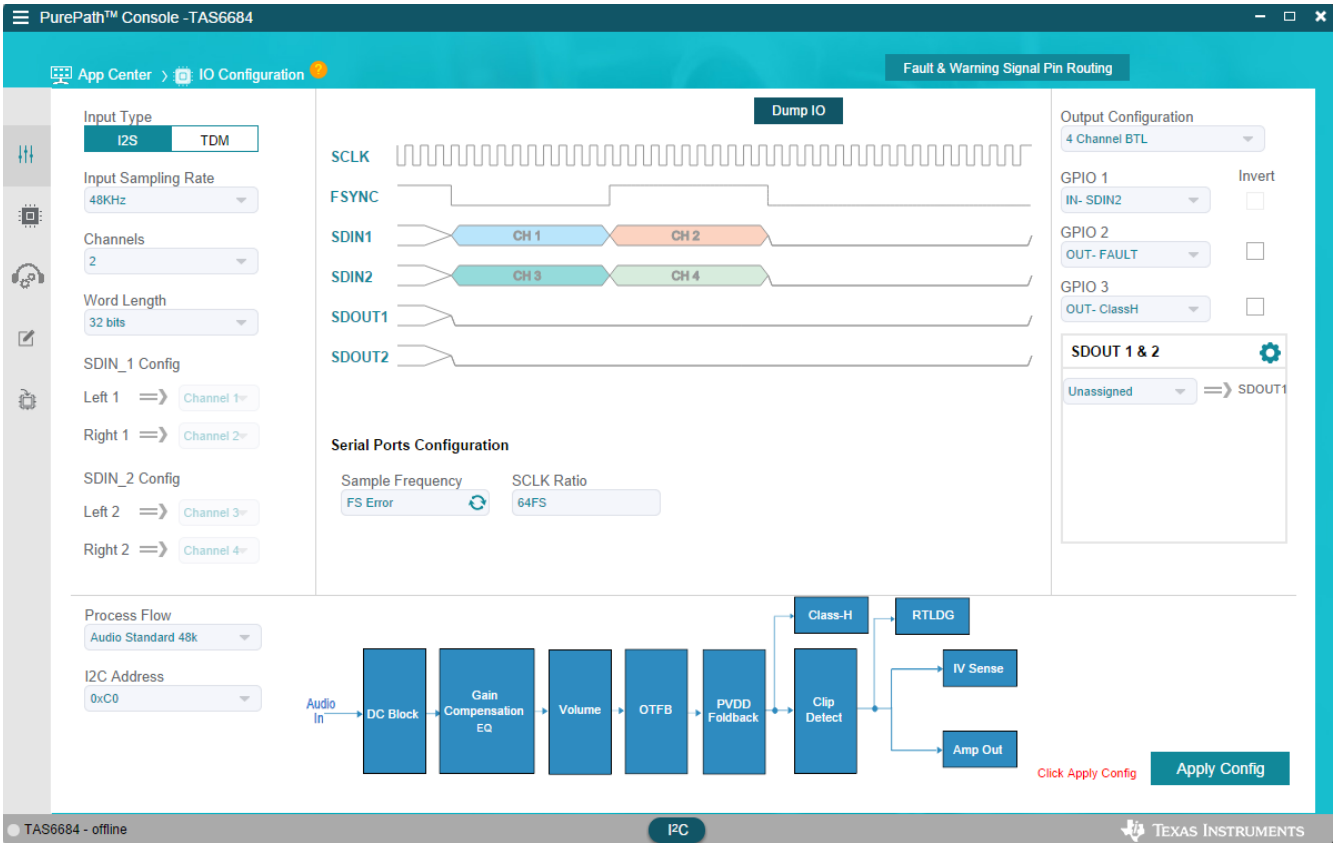

Figure 4-2. PPC3 startup Tab

The GUI can only configure one TAS6684 at a time. Change the address to configure the other TAS6684. The TAS6684 on the board has two default I^{2}C addresses, 0xC0 (U1) and 0xC2 (U2).

The "Device Monitor & Control" tab can be used to control multiple features of the TAS6684.

- Individual channel state and volume
- Global channel state
- Miscellaneous Controls
  - Over Current level. Change the level as needed.
  - PWM Frequency
  - Spread Spectrum control
  - Analog Gain
  - Phase selection for channel to channel PWM phase
- Fault and Warning Monitor
- AC Load Diagnostics
- DC Load Diagnostics

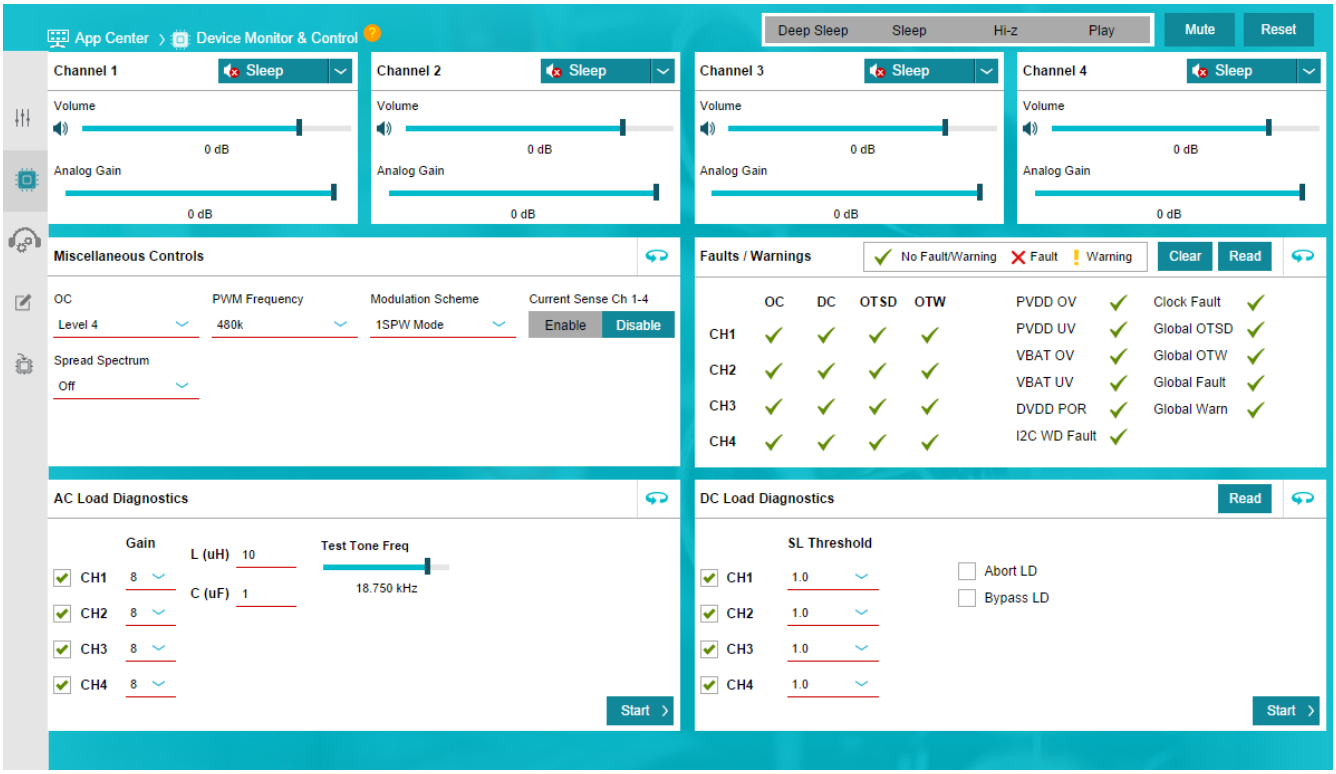

Figure 4-3. Device Monitor & Control Tab

The audio processing tab provides the functions which select in the process flow. Adjust the parameters as needed.

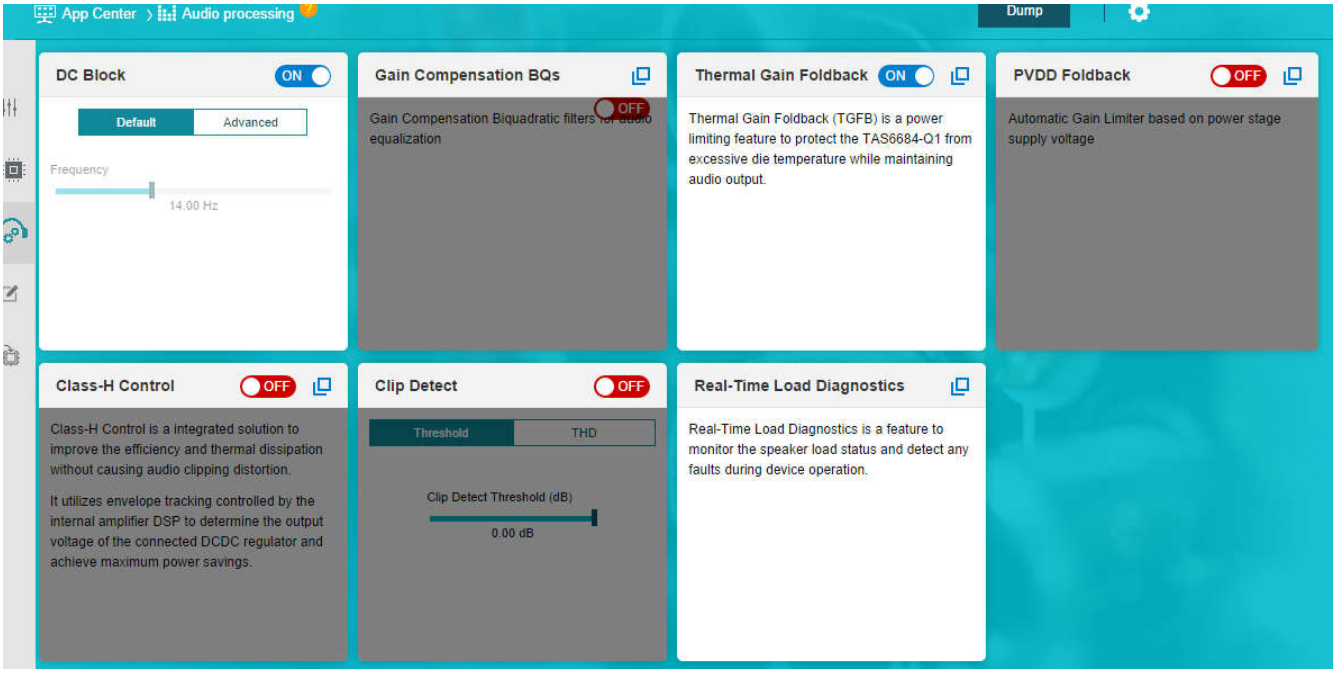

Figure 4-4. Audio Processing Tab

The end system integration tab provides the option to dump the final .h or .cfg configuration code.

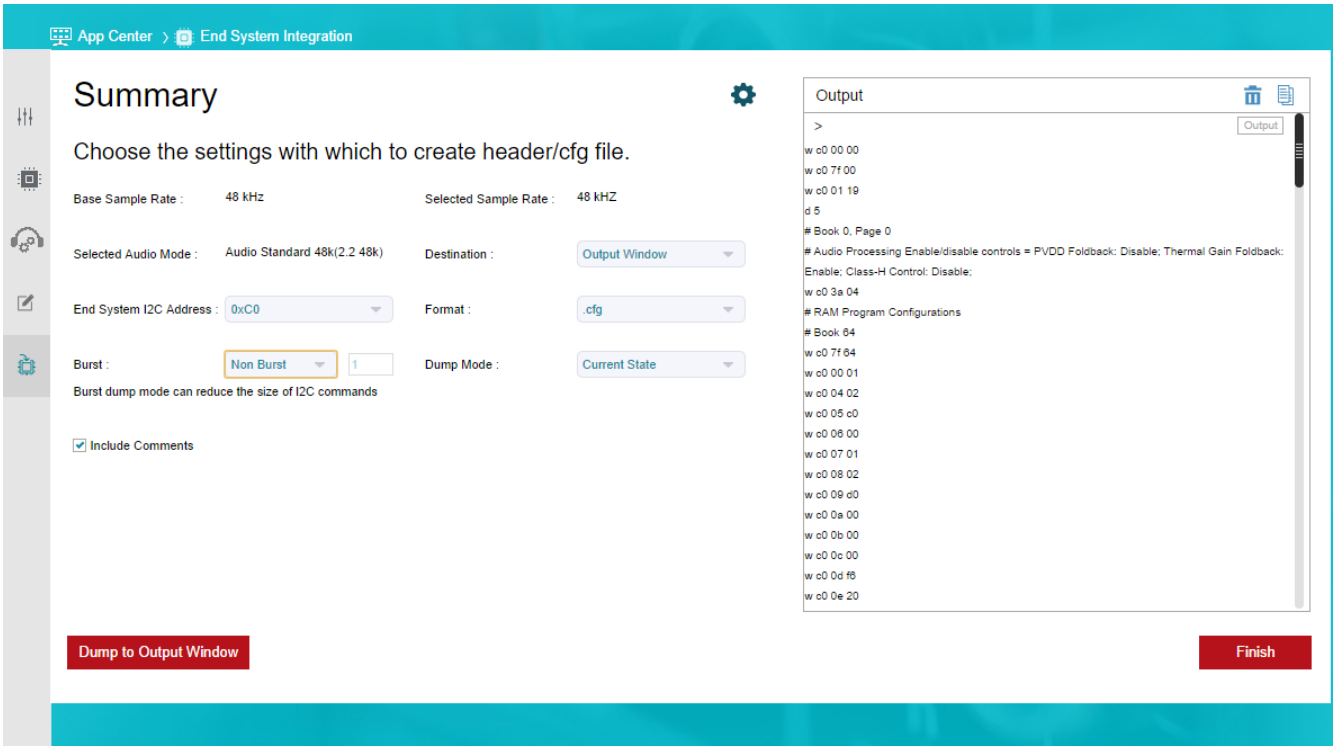

Figure 4-5. End System Integration Tab

The I²C Monitor Button is at the bottom of PPC3 window.

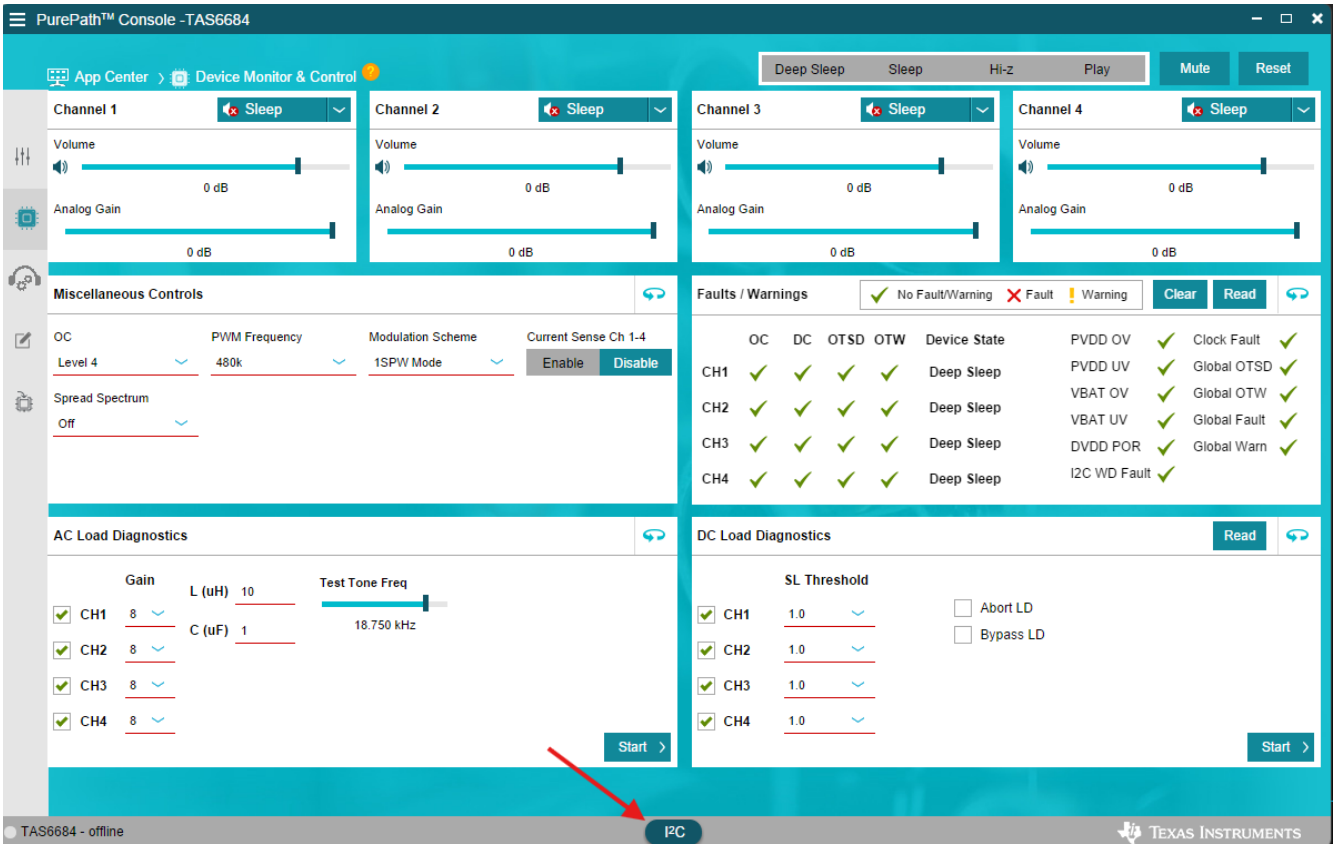

Figure 4-6. I²C Monitor Button

Select the "I/O" tab to read from and write to the TAS6684 registers directly. You can develop and test scripts here. Create a script by typing directly into the window, or by opening a script saved on your computer. Then, press "Execute" button to run the script and view the results in the "Output" pane.

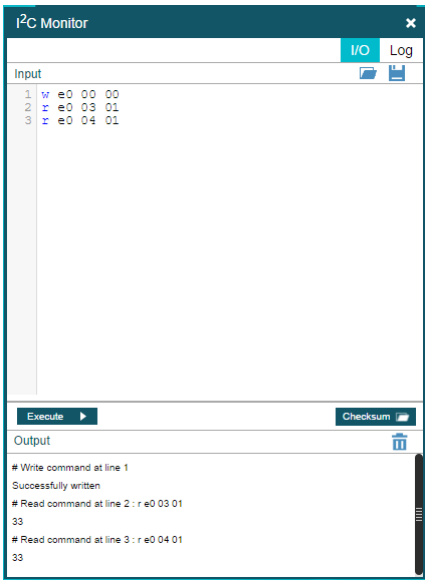

Figure 4-7. I/O Tag in the I²C Monitor Function

Select the "Log" tab, and start recording I²C, the Monitor window reports the I²C command for every step you perform in the PPC3 GUI. This is useful for viewing the I2C transaction each of the buttons in the other windows. The code used in the transactions can be used in the I/O tab.

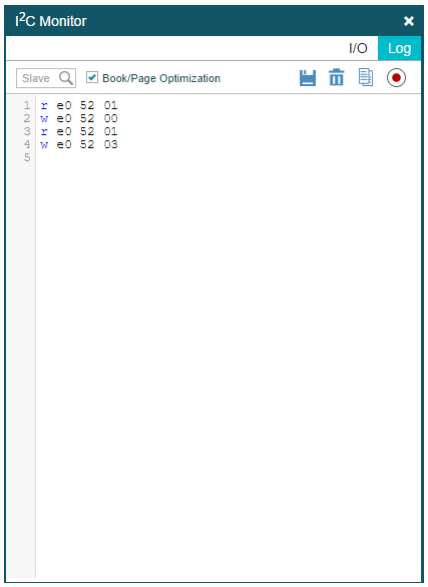

Figure 4-8. Log Tab in the I²C Monitor Function

4.4 Test Results

4.4.1 Test Results of Audio Amplifier

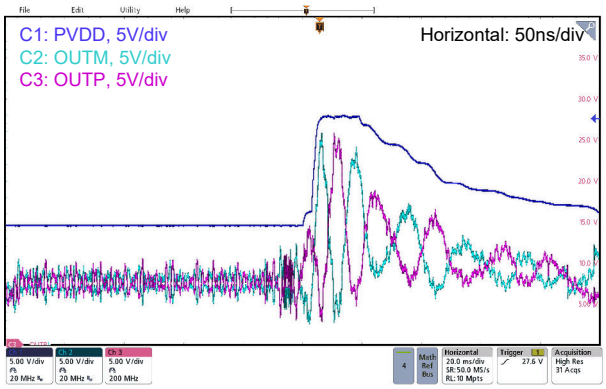

Figure 4-9. Class-H Amplifier Output and PVDD, Vin=9V

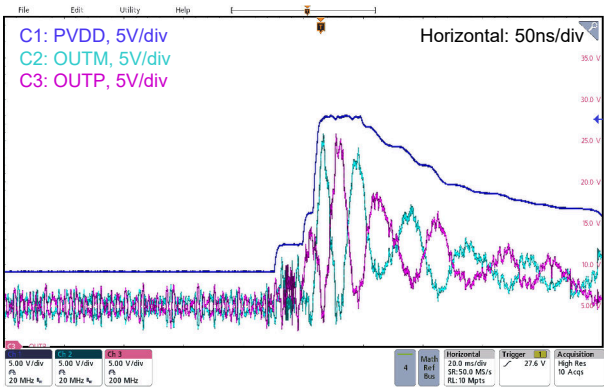

Figure 4-10. Class-H Amplifier Output and PVDD, Vin=14.4V

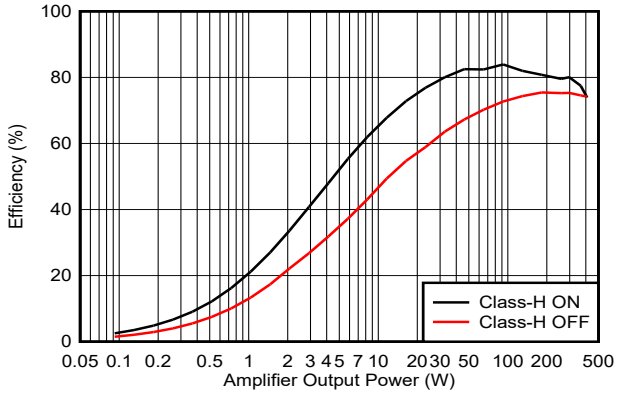

Figure 4-11. System Efficiency Comparison With Class-H On and Off

4.4.2 Test Results of Boost Converter

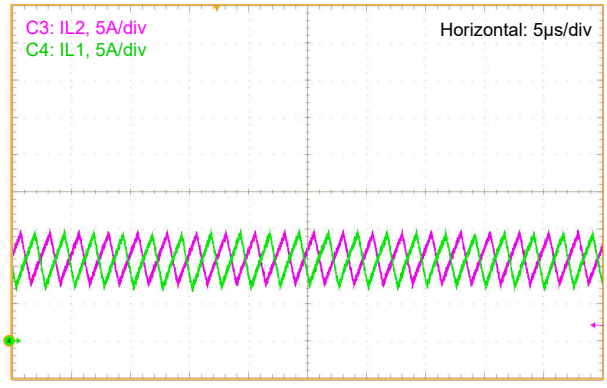

Figure 4-12. Static Current Sharing

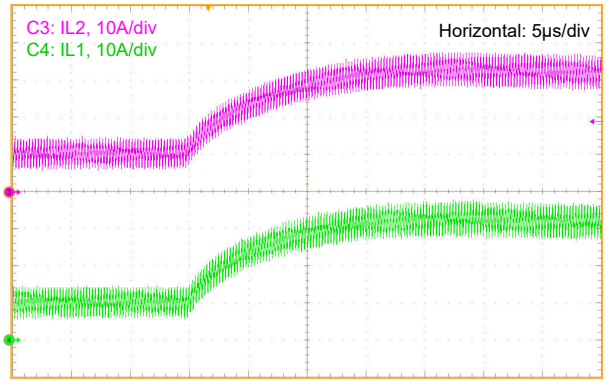

Figure 4-13. Dynamic Current Sharing

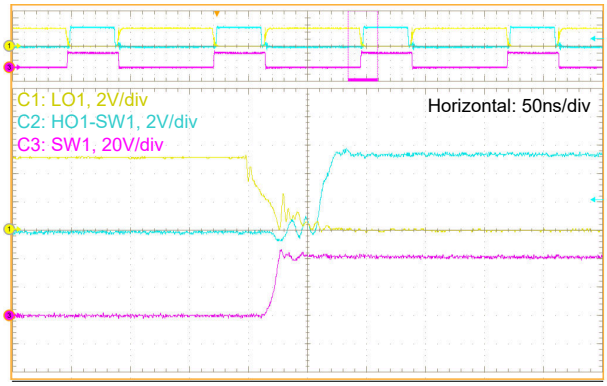

Figure 4-14. Deadtime LO to HO

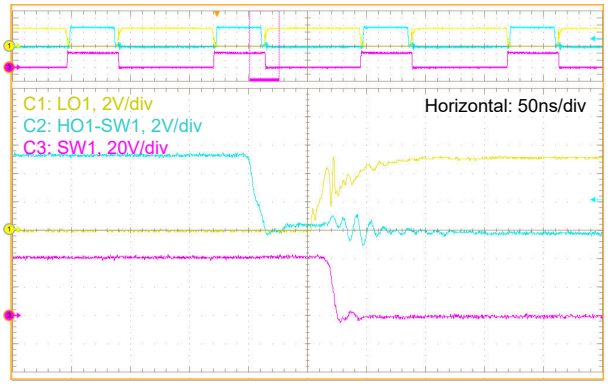

Figure 4-15. Deadtime HO to LO

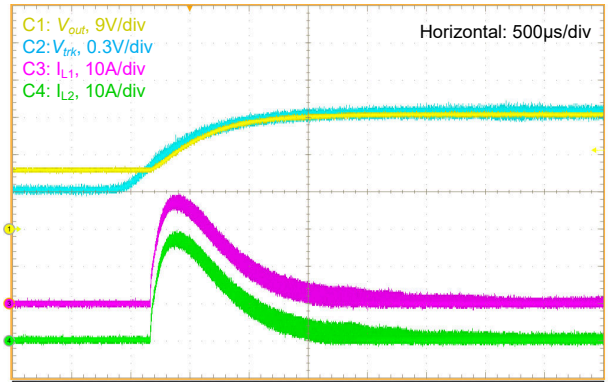

Figure 4-16. PVDD Voltage Tracking 9V to 28V

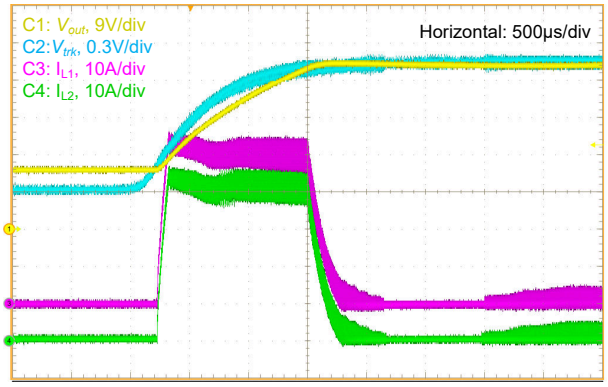

Figure 4-17. PVDD Voltage Tracking 9V to 40V

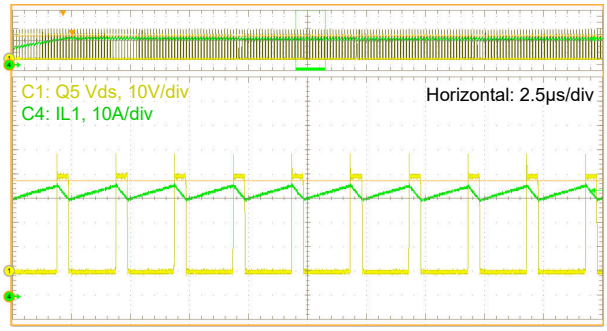

Figure 4-18. Q5 Vds Voltage Stress at Peak Current Limit

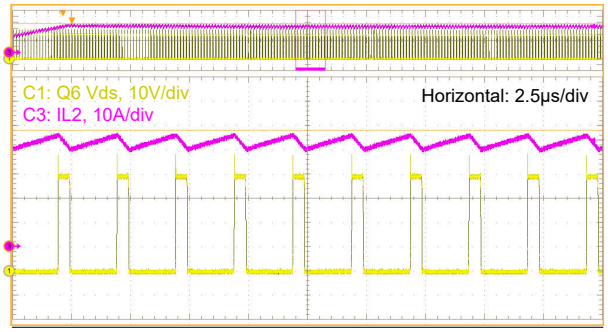

Figure 4-19. Q6 Vds Voltage Stress at Peak Current Limit

5 Design and Documentation Support

5.1 Design Files

5.1.1 Schematics

To download the schematics, see the design files at TIDA-020088.

5.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-020088.

5.1.3 PCB Layout Recommendations

5.1.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-020088.

5.2 Software

- PPC3 (PUREPATHCONSOLE)
- TAS6684 PPC3 GUI

5.3 Documentation Support

1. Texas Instruments, *LM5125A-Q1, Wide-VIN 2.2MHz dual-phase boost controller with VOUT tracking*
2. Texas Instruments, *TAS6684-Q1 - 45V, 13A Digital Input 4-Channel Automotive Class-D Audio Amplifier with Current Sense and Real-time Load Diagnostics*
3. F. Ji, W. Qiu and F. He, "Design Considerations of a Dual-Phase Interleaved Boost Converter in Class-H Audio Amplifier System," *PCIM Conference 2025; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, Nürnberg, Germany, 2025, pp. 2063-2070, doi: 10.30420/566541272.

5.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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