Design Guide: TIDA-010992

Centralized Six-Axis Motor Control Using a Single MCU for Humanoid Robot Hand Reference Design

Description

This reference design uses a single TI C2000™ F28P65 microcontroller for industrial Ethernet motor drives with six-axis control. The design uses a printed circuit board (PCB) with less than 42cm^2 to drive a 6 degree of freedom (DoF) humanoid robot hand. The design demonstrates a small form factor and integrated platform. This integrated platform leverages six DRV8376 three-phase motor drivers with integrated current sensing and FETs as the power stage. The platform includes real-time motor control and industrial Ethernet communication using the F28P65 device with two 32-bit C28x Digital Signal Processor (DSP) Central Processing Units (CPU) and one Control Law Accelerator (CLA) CPU, all running at 200MHz.

Resources

TIDA-010992	Design Folder
TMS320F28P650DK, TPS650352-Q1	Product Folder
DRV8376, DP83826A, LMK3C0105	Product Folder
C2000WARE-MOTORCONTROL-SDK	Tool Folder

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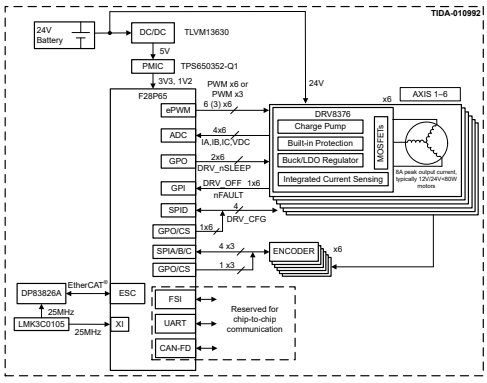
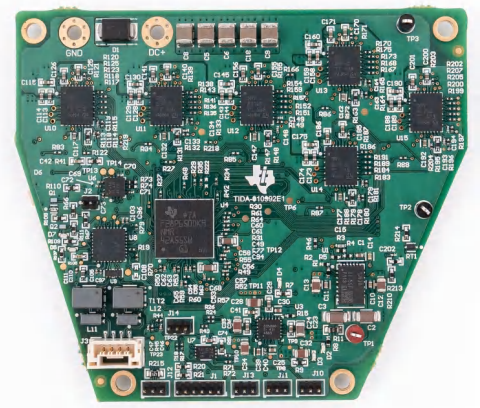
Features

- Compact design with highly integrated circuits (IC) facilitates a PCB size less than 42cm^2
- Single real-time microcontroller (MCU) with two CPUs to control six independent closed-loop field-oriented control (FOC) for current, velocity, and position
- High efficiency current monitoring and small form factor of DRV8376 with integrated low-side current-sense amplifier and integrated field-effect transistors (FET)
- Flexible communication interface option for chip-to-chip communication, for example, fast serial interface (FSI), universal asynchronous receiver-transmitter (UART), and controller area network with flexible data-rate (CAN-FD)

Applications

- Humanoid robot motor drive
- Robot communication module





1 System Description

This reference design demonstrates the capacity of TI C2000™ MCU-F28P65 devices to handle an industrial Ethernet-connected real-time motor drive with six-axis control.

The control part of this design includes one 200MHz C28x core on a F28P65 MCU with a small 9mm × 9mm BGA package to perform 2-axis closed loop field-oriented control (FOC) and run EtherCAT application also. Meanwhile, another C28x core of this F28P65 MCU is used to perform 4-axis closed loop FOC motor control. The single MCU F28P65 generates 36 complementary PWM signals with high-resolution epwm modules and measures the 3-phase current of 6 motors by 18 channels analog-to-digital converter (ADC) integrated in MCU. This reference design employs one digital encoder per motor with serial peripheral interface (SPI) to feedback the position data of the motor rotor.

The power stage includes six 70V, 4.5A peak 3-phase motor driver DRV8376 with integrated current sensing and integrated field-effect transistors (FETs), optimized for extremely low gate loop and low power loop impedance. The low on-state resistance RDS(ON) of 400mΩ (high-side plus low-side) to enable high-power drive capability. The phase current is sensed using an integrated current sensing feature eliminating the need for external shunt resistors. The DRV8376 also integrated protection features including supply under voltage lockout (UVLO), Charge pump under voltage (CPUV), Overcurrent protection (OCP), Overtemperature warning and shutdown (OTW/OTSD), Fault condition indication (nFAULT) and fault diagnostics over SPI. The control scheme is highly configurable through register settings ranging from motor current limiting behavior to fault response.

This reference design showcases the unique multi-axis motor control scheme to implement 6 independent FOC control loop with 16kHz control cycle time and with 64kHz PWM switching frequency to reduce the motor ripple current. The position loop can be controlled by the motion controller through EtherCAT connection.

1.1 Terminology

Table 1-1. Terminology

SOC	System on-chip
FOC	Field-oriented control
MCU	Micro-programmed control unit
MIPS	Million instructions per second
CLA	Control law accelerator
CLB	Configurable logic block
BLDC	Brushless DC
IGBT	Insulated gate bipolar transistor
GaN	Gallium Nitride
SiC	Silicon Carbide
DRAM	Dynamic random access memory
SRAM	Static random access memory
RPM	Revolutions per minute
EtherCAT	Ethernet for control automation technology
EPWM	Enhanced pulse-width modulation
CMP	Event comparator
CAP	Event capture
ISR	Interrupt service routine
EPWM	Enhanced pulse-width modulation
GPIO	General-purpose input output
FIFO	First in, First out
SPI	Serial peripheral interface

1.2 Key System and Interface Specifications

Table 1-2. Key System Specifications

PARAMETER	TYPICAL VALUE	COMMENT
DC input voltage	24V (12V to 36V)	36V absolute maximum
Maximum three-phase continues output current	$2A_{RMS}$	DRV8376 output current capability is 4.5A Peak
PWM switching frequency	64kHz	DRV8376 is capable of driving 100kHz PWM
PWM dead band	100ns	< 200ns
Current sense accuracy	+/- 5%	Based on DRV8376 datasheet
FOC loop control frequency	16kHz	For all 6 axes
PCB layer stack	8-layer, 1oz copper	
PCB size	6 × 7 cm	
Encoder	15-bit core resolution	SPI
Motor specification	12mm diameter, 30000rpm, 0.4Arms, 2.8mNm, with 1:16 gearbox	Back EMF factor: 0.55 V/krpm, line resistance 11.15Ω, line inductance 220µH, Inertia 0.194g/cm^2

Table 1-3. Interface Specification

PIN	SIGNAL	FUNCTION
J1-1	GND	JTAG
J1-2	JTAG_TMS	
J1-3	JTAG_TDI	
J1-4	JTAG_TCK	
J1-5	JTAG_TDO	
J1-6	3V3	
J2	Jumper ON (SCI/Wait mode) Jumper OFF (Flash mode)	BOOT MODE
J3-1	H0_TD_N	PHY0 MDI
J3-2	H0_TD_P	
J3-3	H0_RD_N	
J3-4	H0_RD_P	
J4-1, J4-2	U	Motor connector for axis1. (J5, J6, J7, J8, J9 are with same pin map)
J4-3, J4-4	V	
J4-5, J4-6	W	
J4-7	3V3	
J4-8	GND	
J4-9	SPI_MISO	
J4-10	SPI_MOSI	
J4-11	SPI_SCK	
J4-12	SPI_CS	
J10-1	FSI_TXA_CLK	FSI TX
J10-2	FSI_TXA_D0	
J10-3	GND	
J11-1	FSI_RXA_CLK	FSI RX
J11-2	FSI_RXA_D0	
J11-3	GND	
J12-1	CAN+	CAN-FD
J12-2	CAN-	
J12-3	GND	
J13-1	UART_TX	UART
J13-2	UART_RX	
J13-3	GND	
J14-1	DRV_OFF_PMIC	DRV_OFF source selection
J14-2	DRV_OFF	
J14-3	DRV_OFF_MCU	

2 System Overview

2.1 Block Diagram

Figure 2-1shows the system block diagram of the TIDA-010992 indicated in the dotted box.

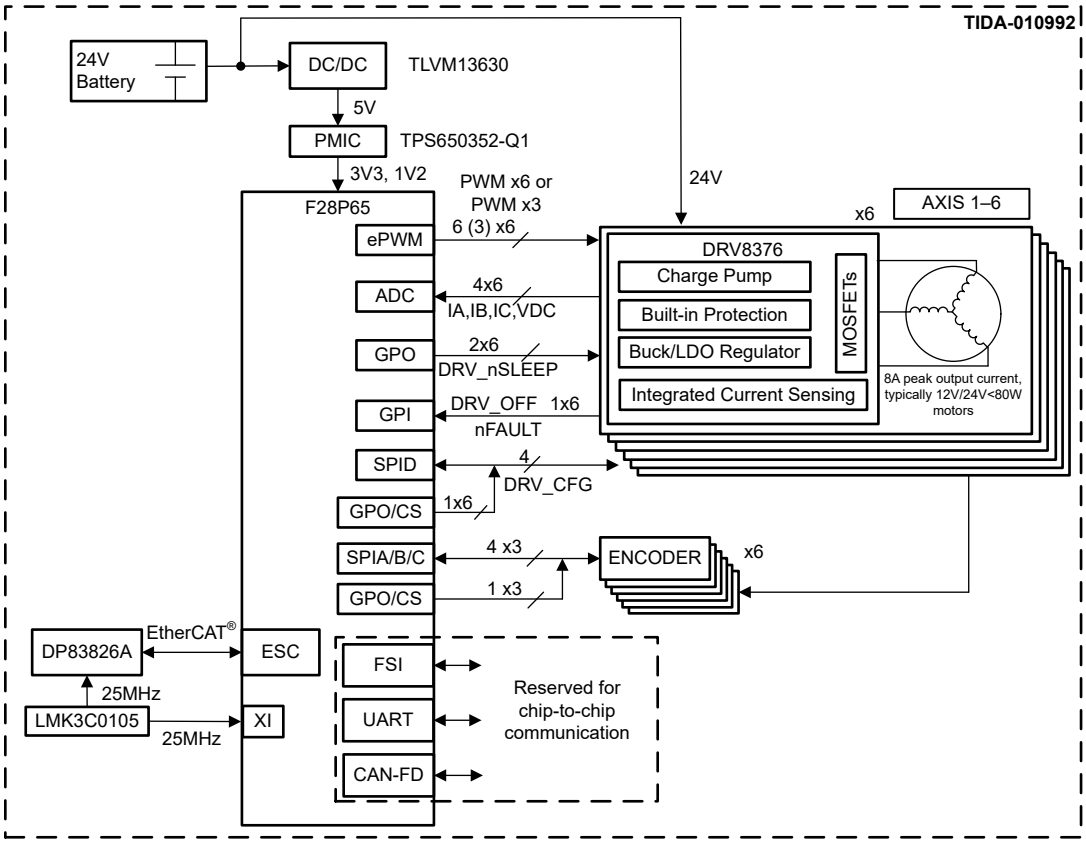


Figure 2-1. System Block Diagram of TIDA-010992

2.2 Design Considerations

The design goal is to implement an integrated multi-axis servo control for humanoid robot hand with 6 DoF. This design can operate from a single DC input voltage from 3V to 30V DC, nominal 24V and output three-phase sinusoidal wave to drive six AC motors. The design contains serval sub-systems including:

- Power trees – A wide input voltage range DC/DC module (TLVM13630) generates the 5V rail to supply the power management integrated circuit (PMIC) which can output and monitor rails 3.3V and 1.2V. 3.3V rail supplies the EEPROM, Ethernet PHYs, MCU IOs and other analog parts. 1.2V rail is for F28P65 core voltage.
- Power inverter – each axis employs a 70V, 4.5A three-phase integrated FET BLDC motor driver (DRV8376) with short circuit, under voltage and over temperature protection. The control scheme is highly configurable through register setting by SPI from motor current limiting behavior to fault response. The 3-phase current are sensed using an integrated current sensing feature eliminating the need for external sense resistors and then feedback the current data to three ADC modules inside the MCU to maintain the simultaneous sensing.
- Control and communication – The motor control and communication employs 200MHz dual-core C28x MCU (F28P65) with real-time control, safety and security. One 200MHz C28 core to perform closed loop field-oriented control (FOC) for 2 axis motor control plus EtherCAT application and another 200Mhz C28 core to run 4 FOC loop for 4 axis motor control. This reference design employs one digital encoder per motor with SPI communication to feedback the position data of the motor rotor.

2.3 Highlighted Products

2.3.1 TMS320F28P65x (F28P65x)

The TMS320F28P65x (F28P65x) is a member of the C2000 real-time microcontroller family of scalable, ultra-low latency devices designed for efficiency in power electronics, including but not limited to high power density, high switching frequencies, and supporting the use of IGBT, GaN, and SiC technologies. The functional block diagram is shown in Figure 2-2. Key features and benefits are summarized in Table 2-1.

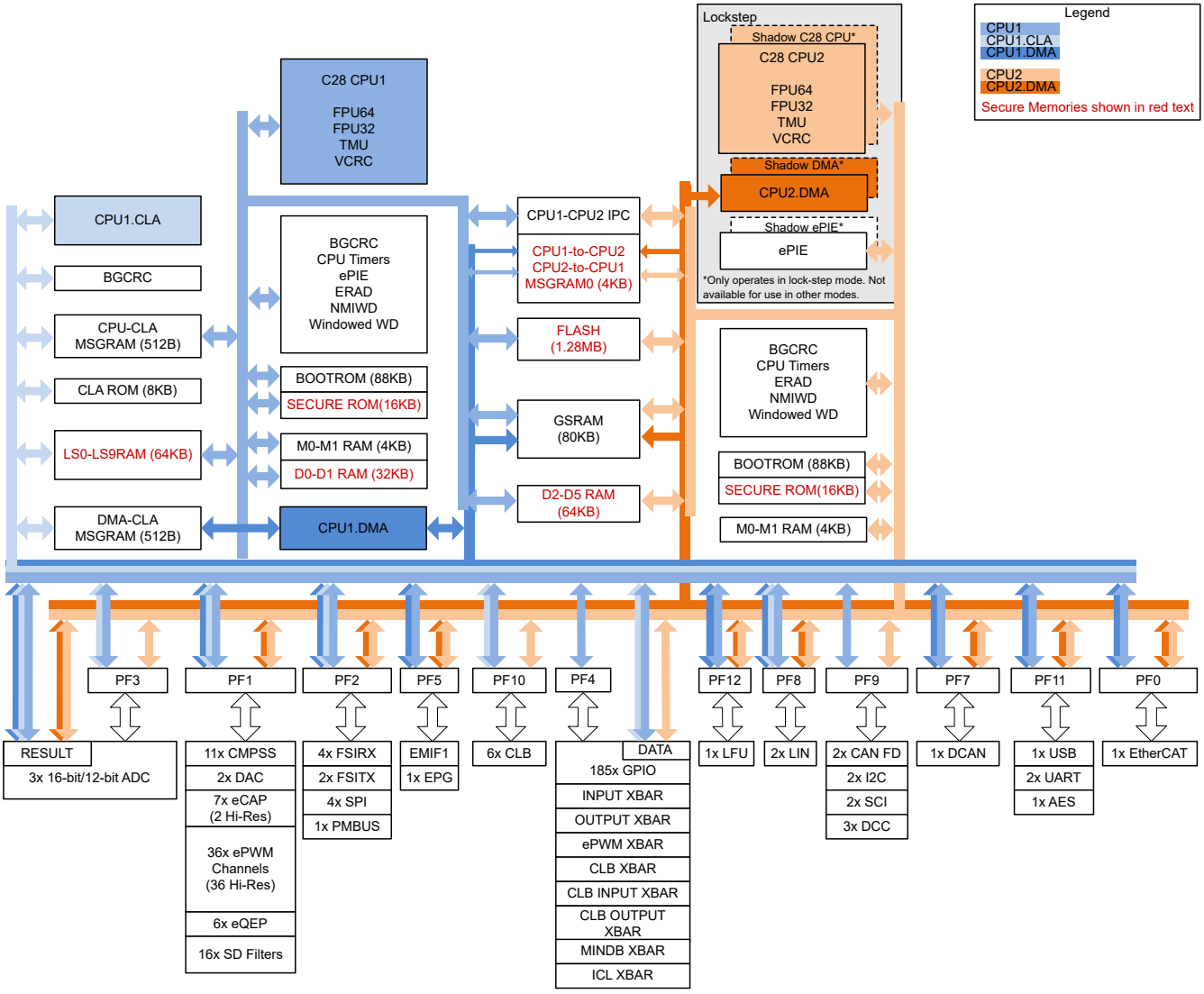


Figure 2-2. F28P65 Functional Block Diagram

Table 2-1. F28P65 Features and Benefits

Features	Benefits
Dual 200MIPS 32-bit C28x DSP core + 200MIPS CLA core with 1.28MB on-chip flash and 248KB RAM	Provide high CPU performance with small package and integration to meet complex real-time processing needs. Benefit to small form factor design.
Trigonometric Math Unit (TMU) on each core	Accelerate trigonometric function for motor control
3 × 16-bit ADC, 36 × Hi-Res PWM (18-ch), 7 × eCAP, 6x eQEP, 16-channel SDFM	Plenty peripherals for low latency motor control loop
EtherCAT SubordinateDevice Controller, 4 × high-speed SPI ports, 2 × CAN-FD, 6 × CLB tiles, FSI	Rich communication and connectivity options to support industrial Ethernet, position feedback interface and serial communication interface.

Table 2-1. F28P65 Features and Benefits (continued)

Features	Benefits
Lock-step on C28x CPU2, Memory Power-on self-test (MPOST), Hardware Built-in self-test (HWBIST), Advanced Encryption standard accelerator, JTAG/Zero-pin boot/dual-zone security.	SIL2 certified for functional safety with self-diagnostic library. Enables secure system design with cryptographic acceleration and secure boot.

2.3.2 DRV8376

The DRV8376 device is an integrated 400mΩ (combined high-side and low-side MOSFET's on-state resistance) driver for 3-phase motor-drive applications. The device reduces system component count, cost, and complexity by integrating three half-bridge MOSFETs, gate drivers, charge pump, current sense amplifiers, and linear regulator for the external load, as shown in Figure 2-3. A standard serial peripheral interface (SPI) provides a simple method for configuring the various device settings and reading fault diagnostic information through an external controller. Alternatively, a hardware interface (H/W) option allows for configuring the most commonly used settings through fixed external resistors. The architecture uses an internal state machine to protect against short-circuit events and protect against dv/dt parasitic turn on of the internal power MOSFET. The DRV8376 device integrates three, bidirectional current-sense amplifiers for monitoring the current through each of the low side MOSFET using a built-in current sense. The gain setting of the amplifier can be adjusted through the SPI or hardware interface.

In addition to the high level of device integration, the DRV8376 device provides a wide range of integrated protection features. These features include power-supply undervoltage lockout (UVLO), charge-pump undervoltage lockout (CPUV), overcurrent protection (OCP), AVDD and GVDD undervoltage lockout (AVDD_UV, GVDD_UV), and overtemperature shutdown (OTW and OTSD). Fault events are indicated by the nFAULT pin with detailed information available in the SPI registers on the SPI device version. The DRV8376 device in a VQFN surface-mount package. The VQFN package size is 6 mm × 5 mm. Key features are summarized in Table 2-2.

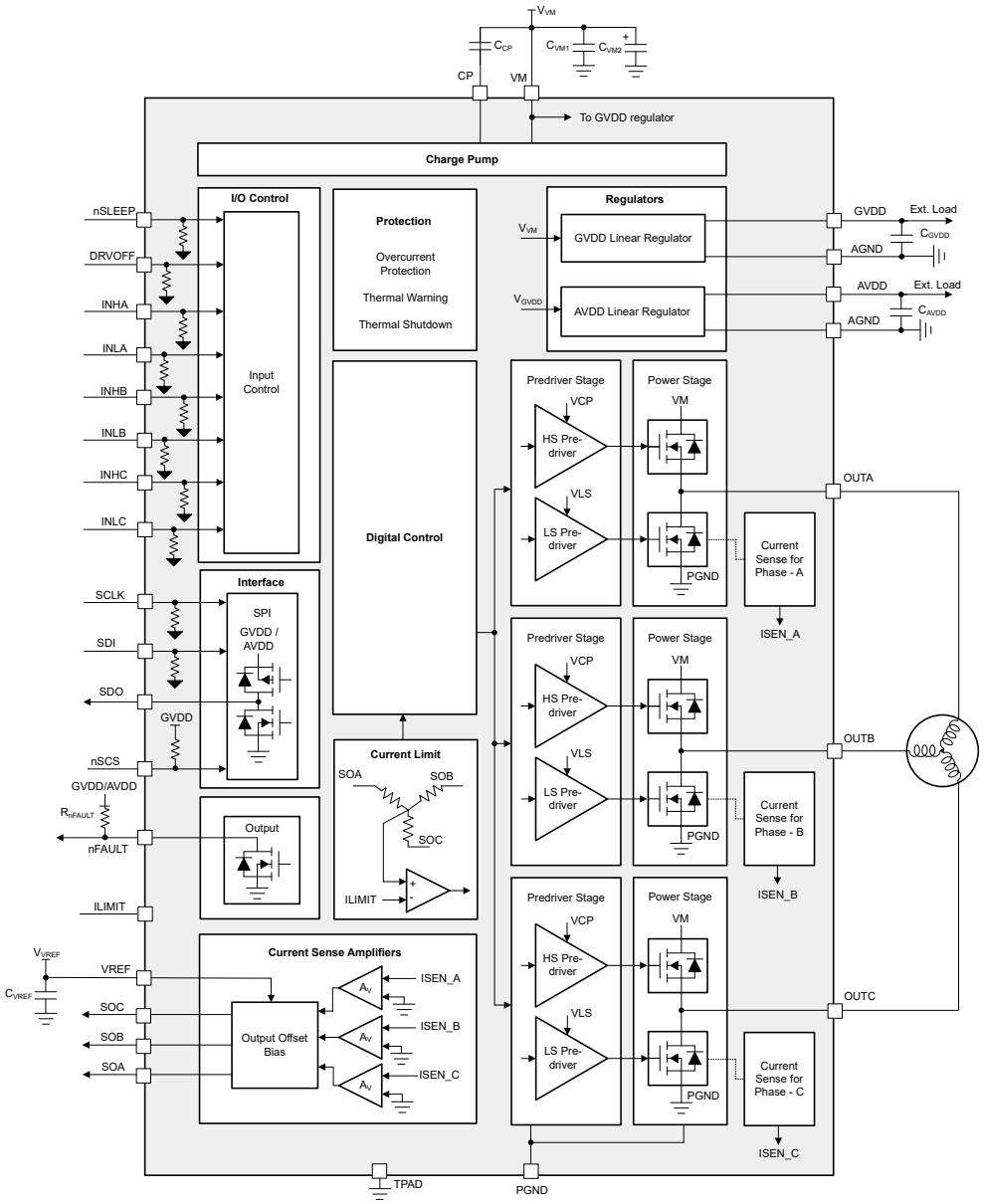


Figure 2-3. DRV8376S Functional Block Diagram

Table 2-2. DRV8376 Features and Benefits

Features	Benefits
Integrated 3-phase integrated 70V FET motor driver, 400mΩ devices for 4.5A Peak operation.	Enables up to 48VDC, three-phase inverter with 1ARMS phase current up to 100kHz high-switching frequency for low inductance and high-speed drives.
Active demagnetization and optimized pinout.	Minimized package parasitic elements enable fast switching for reduced switching losses. Easy PCB layout.
Low audible noise, ultra-low dead time < 200ns and propagation delay < 100ns.	Enables ultra-low dead band per half-bridge for major reduction of switching losses in three-phase inverter applications and elimination of dead-time distortions in the phase voltage. Excellent motor control performance.
6x or 3x PWM control interface, integrated current sensing, SPI interface to read/write DRV register	Dose not require external current sense resistor. Flexible device configuration via SPI interface. Reduce PCB size and BOM.
Drive OFF mode and low-power sleep mode	Enables OFF mode of device to output Hi-Z for all pins. Enables low-power sleep mode with 1.5uA at VVM=24V.
Integrated protection UVLO, CPUV, OCP, OTW, OTSD	BOM reduced for external protection circuitry.

2.3.3 DP83826A

The DP83826Ax offers low and deterministic latency, low power and supports 10BASE-Te, 100BASE-TX Ethernet protocols to meet stringent requirements in real-time industrial Ethernet systems. The device includes hardware bootstraps to achieve fast link-up time, fast link-drop detection modes and dedicated reference CLKOUT to clock synchronize other modules on the systems. The two configurable modes are BASIC standard Ethernet mode that uses a common Ethernet pinout, and ENHANCED Ethernet mode which supports standard Ethernet mode and multiple industrial Ethernet fieldbus applications with additional features and hardware bootstraps configuration.Figure 2-4shows the functional block diagram and Table 2-3 show the key features and benefits.

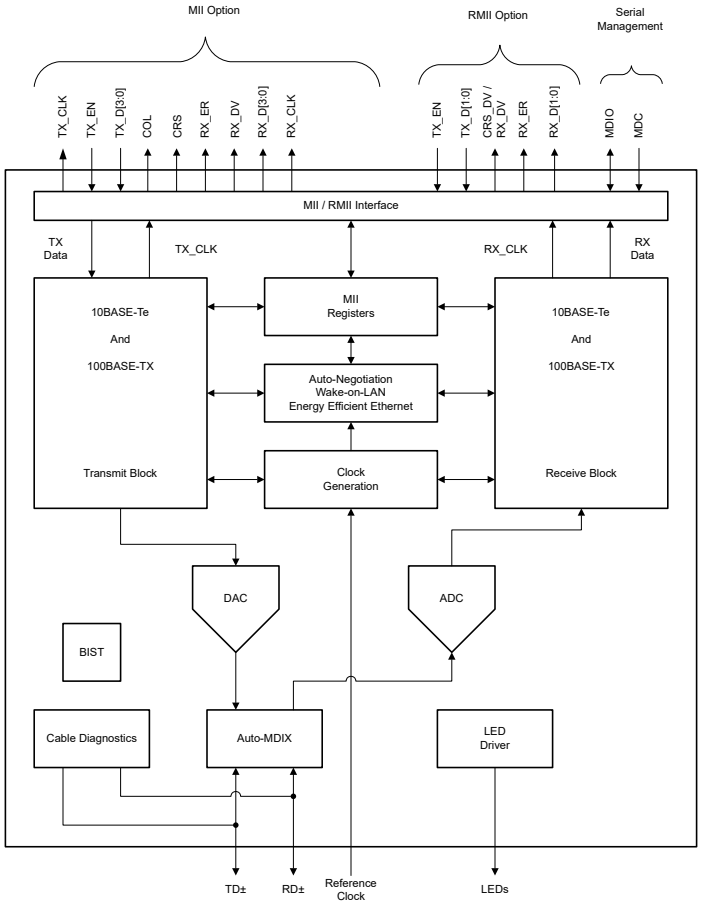


Figure 2-4. DP83826A Functional Block Diagram

Table 2-3. DP83826A Features and Benefits

Features	Benefits
Low and deterministic latency	To meet stringent requirements in real-time industrial Ethernet systems such as EtherCAT.
Integrated circuitry for enhanced EMC, IEEE 802.3 compliant	Enables robust and EMC compliant system design
Low power consumption, programmable energy-saving modes	Enables less power requirements of the system
Two selectable pin modes in single device	Provides flexible hardware bootstraps without any software for easy configuration.
Extended operation temperature range	To support higher ambient temperature such as humanoid application

3 System Design Theory

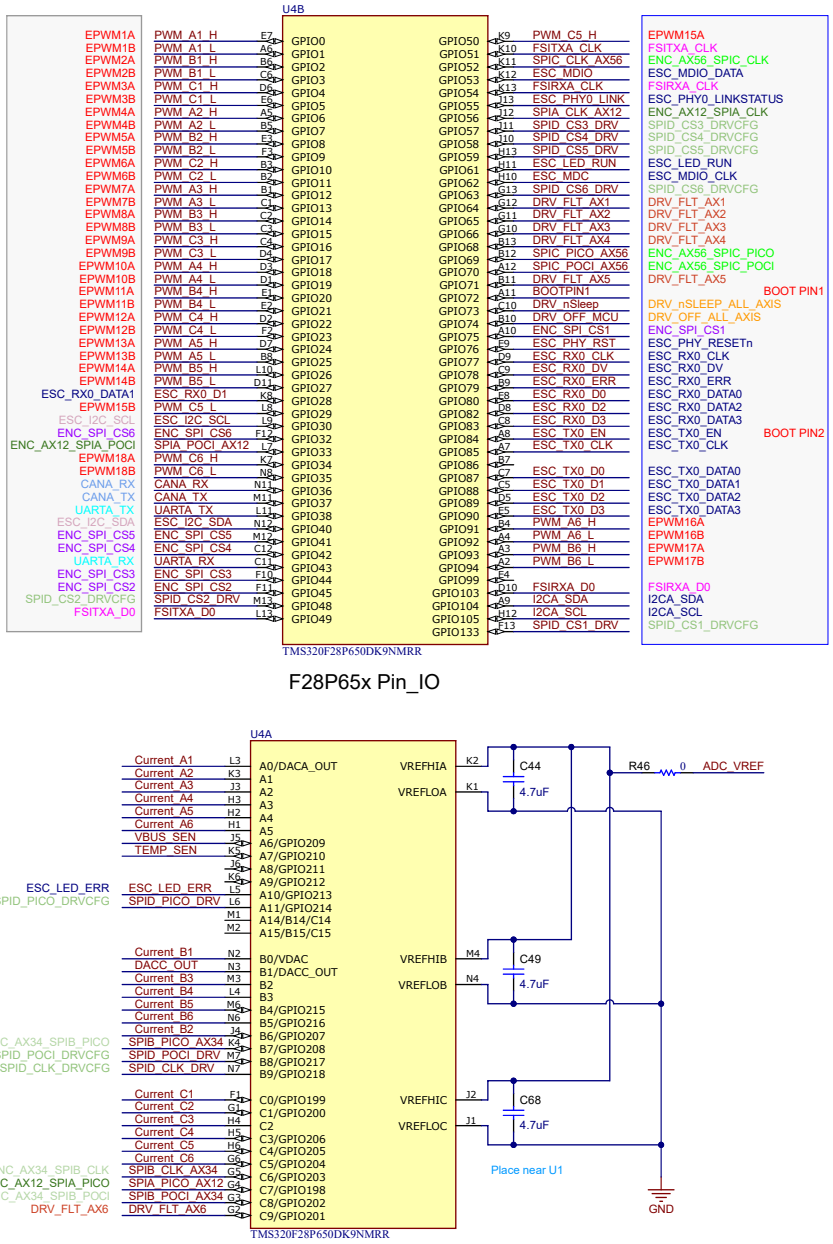
This section provides design guidelines for this reference design.

3.1 F28P65 Motor Control and Communication Interface

This design leverages F28P65 dual core with lockstep plus CLA and EtherCAT with NMR (9 × 9 mm) package as the motor control and communication controller. The motor control interface includes:

- Enhanced Pulse Width Modulator (ePWM) – The PWM peripheral is built up from smaller single channel submodules with separate resources that can operate together as required to form a system. This design employs ePWM 1 to 18 for the 6 axis's three phase motor driver. Each ePWM submodule has two channels A and B to generate two complementary PWM signals with configurable dead-band. For three-phase motor control, total 6 × PWMs are implemented per axis. All these PWM submodules share the same time base clock of 200MHz with up and down count mode and synchronize with each other. Each ePWM module has a synchronization input and an output which can be configured to link to serval sources and events such as EtherCAT sync0 pulse and FSI RXTRIG to close the loop between communication and PWM. In this reference design, EPWM1 of axis 1 is triggered by EtherCAT sync0 pulse and all the other EPWMx modules' sync IN are triggered by EPWM1's Sync OUT.
- Analog-to-digital converter (ADC) – The ADC peripheral is a successive approximation (SAR) style ADC with selectable resolution of 12 bits or 16 bits. Each ADC module consists of a single sample-and-hold (S/H) circuit allowing simultaneous sampling for 3-phase current of a motor. The ADC reference voltage is provided by an external high-precision voltage reference chip REF6230. The corresponding ADC channels start sampling time for each axis are triggered by its own ADC-start-of-conversion (SOCA) and this SOCA event is triggered by the compare event C of each axis EPWM module respectively. The interrupt which is used for the FOC calculation is generated automatically once data conversion is done by ADC SOC.
- EtherCAT SubordinateDevice Controller (ESC) – The ESC on this F28P65 MCU provides up to 2 Media Independent Interface (MII) ports to connect to EtherCAT PHYs. The process data interface is through 16-bit asynchronous interface. The ESC also provides a 64-bit distributed clocking which can be used internally or externally. Including utilizing SYNC0/1 and LATCH0/1 output signal to synchronize GPIOs, allow inputs from any GPIOs as well as other muxing options for internal device events and supporting timestamping. The ESC has 8 field bus memory management units (FMMUs) which can support all native types of RD/, WR/, RDWR, and built-in features of bit- and byte-addressing. An I^2C EEPROM interface is provided to store the information like MAC address. ESC access allocation is to the CPU1 subsystem during initialization.
- Dual core motor control design – This reference design leverages dual C28x DSP core to perform 6 axis motor control and industrial communication with CPU1 is handling axis 1 and axis 2 control plus EtherCAT application and CPU2 is handling axis 3 to 6 motor control. The memories and peripherals need to be assigned allocation for both CPUs as follows:
- Flash bank 0 to bank 3 (0x80000 - 0xFFFFF) owned by CPU1 and bank 4 (0x100000 – 0x11FFFF) owned by CPU2
- DRAM1-4 from 0x00C000 to 0x020000 for data purpose, GSRAM0-2 from 0x008000 to 0x022000 for code purpose are assigned to CPU1. DRAM5 from 0x020000 with 8KB length, GSRAM3-4 from 0x016000 with 16KB length are assigned to CPU2.
- EPWM1-6 are controlled by CPU1 and EPWM7-18 are controlled by CPU2
- ADCA and C are controlled by CPU1, ADCB is controlled by CPU2
- SPIA and D are controlled by CPU1 for axis 1-2 encoder interface and DRV configuration, SPIB and C are controlled by CPU2 for axis 3-6 encoder interface
- EtherCAT controlled by CPU1
- CLB1 is controlled by CPU1 for triggering SPIA data transmission, CLB2 and CLB5 are controlled by CPU2 for triggering SPIB and C data transmission.

Figure 3-1 shows the motor control and communication interface of TIDA-010992, and Figure 3-2 shows the axis 1 motor control peripherals example.



F28P65x Pin_IO

Figure 3-1. F28P65 Motor Control and Communication Interface of TIDA-010992

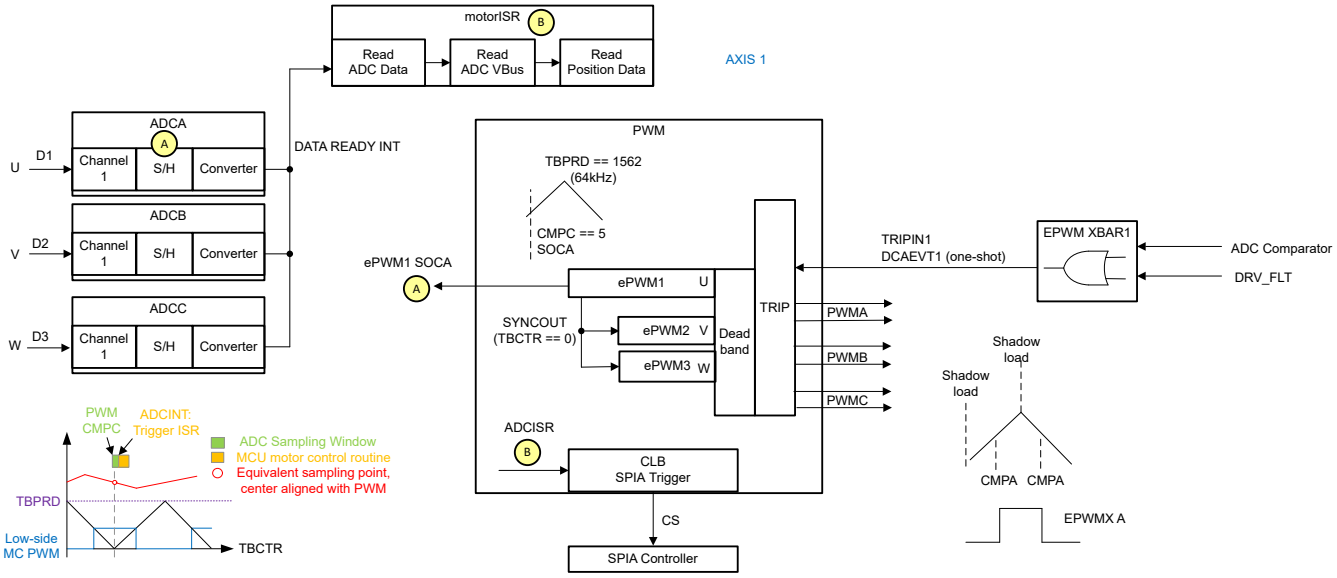


Figure 3-2. AXIS 1 Motor Control Peripherals Example of TIDA-010992

3.2 Multi-Axis Motor Control Scheme

To avoid the sampling timing overlaps for the current and position of each axis since the three ADC modules and three SPI controllers are peripheral resources shared between all axes. Hence, a specific control scheme is employed in this reference design. Figure 3-3 shows the timing scheme for all axes FOC loop of motor control. The SOCA event timing which triggers the ADC sampling of each axis is staggered to ensure only one axis current is sampled during one time. And also, the position data is requested in the ADC interrupt service routine during the same time. With this control scheme, all six axes FOC loops are calculated without any overlaps and within a certain cycle time of 16kHz. While the PWM switching frequency is set to 64kHz to reduce the ripple current of the motor.

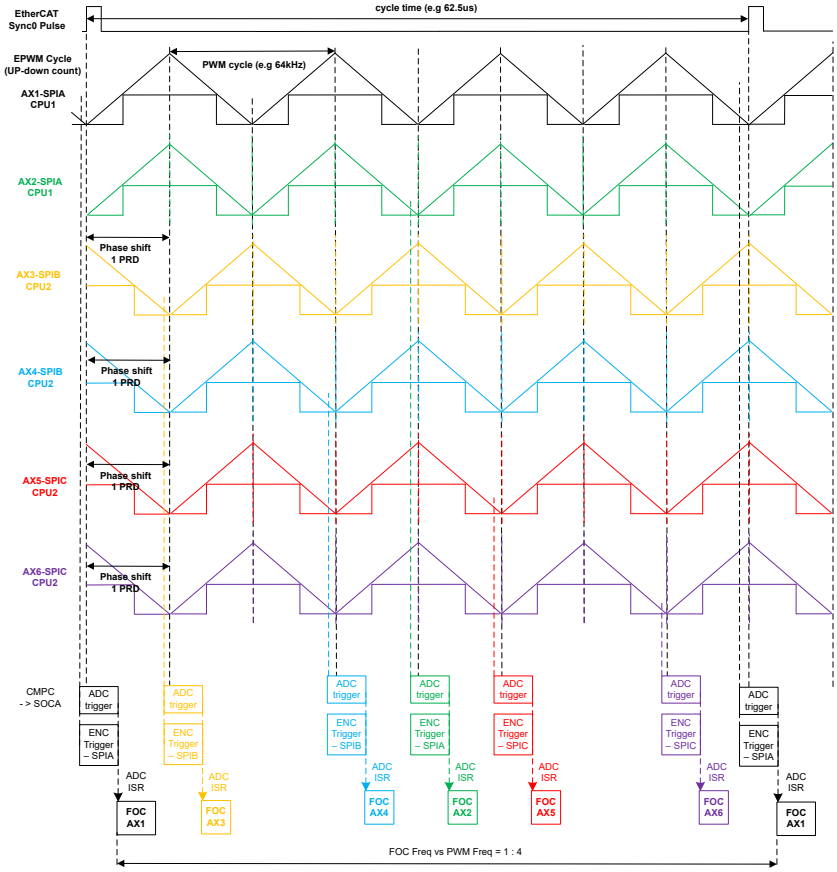


Figure 3-3. 6 Axis Motor Control FOC Loop Timing Scheme

3.3 DC Link Decoupling

The nominal 24V DC input voltage is buffered with eleven 10µF ceramic capacitors to get a total of 110µF DC-bus capacitance. A transient voltage suppressor (TVS) diode is implemented also to protect the over-voltage of the input. The PCB employs one entire and solid ground polygon to have better thermal performance.Figure 3-4 shows the schematic of DC-link decoupling.

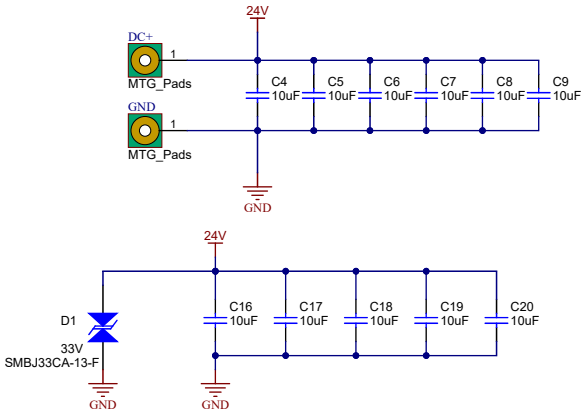


Figure 3-4. DC-link Decoupling Schematic

3.4 Three-Phase Inverter With DRV8376

This design leverages six 70V, 4.5A three-phase integrated FET BLDC motor driver (DRV8376) with short circuit, under voltage and over temperature protection. The 3-phase current per axis are sensed using an integrated current sensing feature eliminating the need for external sense resistors and then feedbacking the current data to three ADC modules inside the MCU to ensure simultaneous sensing. The DRV control scheme is highly configurable through register setting by SPI from motor current limiting behavior to fault response. The PCB space is further reduced due to high integration and the fact that only a few additional passive components are required. Figure 3-5 shows the schematic of one axis inverter power stage.

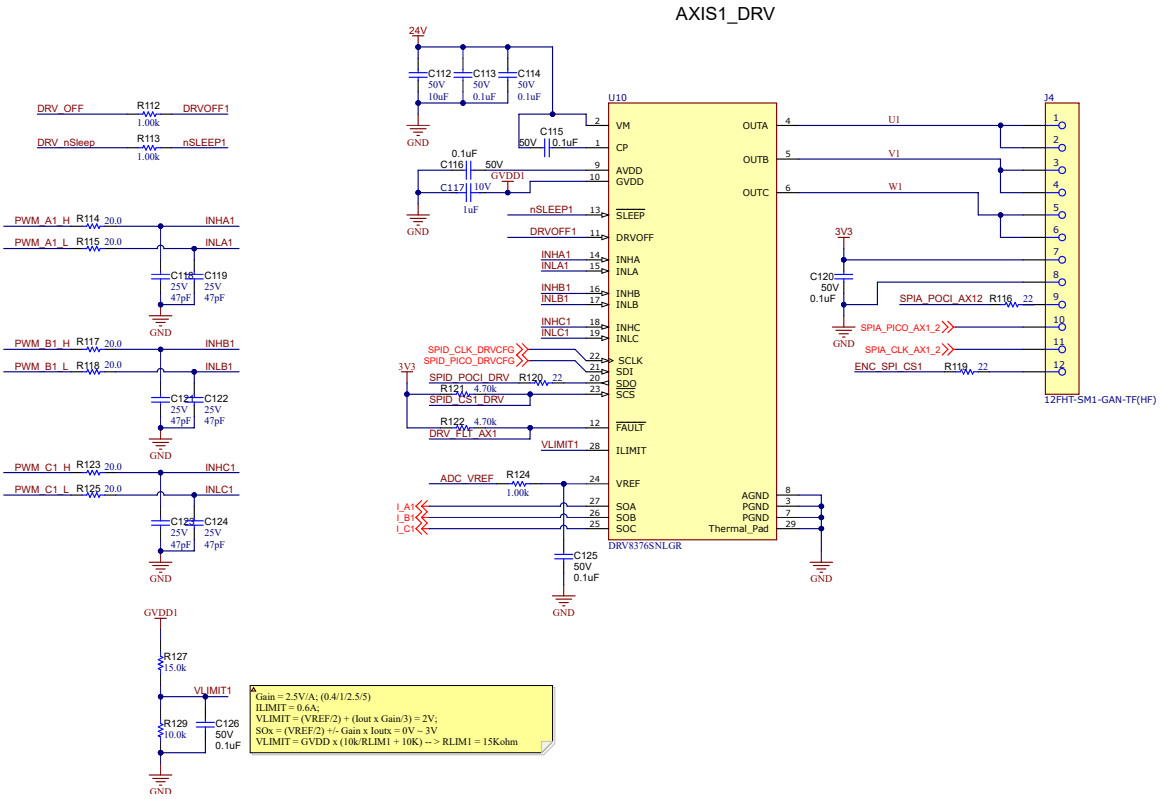


Figure 3-5. Three Phase Inverter Power Stage Schematic for Axis 1

The 24V DC-link voltage is connected to the DRV8376 VM pin and referenced to the ground (PGND/AGND) pin. Local ceramic bypass capacitors C112, C113, C114 are placed in parallel close between the VM and PGND pins to minimize loop inductance.

The DRV8376 integrated gate driver is supplied with internal charge pump. A 0.1µF ceramic bypass capacitor (C115) is placed close to the CP pin and VM pin, as suggested in the data sheet.

A 1uF ceramic bypass capacitor (C117) is placed close to the GVDD pin which is the 5V internal regulator output.

The complementary PWM signals for the high-side and low-side of switch from MCU are low-pass filtered with R114, C118, R115, C119, R117, C121, R118, C122, R123, C123, R125 and C124 to reject high-frequency impulse noise and avoid false switching with a cutoff frequency of around 160MHz and a propagation of around 1ns. The OUT pins are connected to the motor 3-phase A, B and C with the motor connector J4.

The SCLK, SDI, SDO and nSCS pins are connected to the SPID controller of MCU for parameters configuration and fault status read back via SPI interface. The nSCS and SDO pins are pulled up with 4.7kohm resistors R121 and R126.

The DRVOFF pin is connected to the MCU GPIO74 via 1kohm resistor R112. When this pin is pulled high then the six MOSFETs are turned OFF, making all outputs Hi-Z.

The nSLEEP pin is connected to the MCU GPIO73 via 1kohm resistor R113. When this pin is logic-low, the DRV device goes into a low-power sleep mode. A 20 to 40us low pulse can be used to reset fault conditions without entering sleep mode.

The VREF pin is connected to the output of a high-precision voltage reference REF6230 via a 1kohm resistor R124 for the phase current feedback. Pin SOA, SOB and SOC are connected to three ADC modules with low-pass filter R48, R49, R50, C50, C56 and C62. The cutoff frequency is around 2.3MHz with a propagation of around 68ns.

The ILIMIT pin is set to 2V with resistors divider R127 and R129. So, the output current is limited to 0.6A according to Equation 1 and the SOA/B/C output voltage range is set from 0V to 3V according to Equation 2.

$$V_{LIMIT} = \frac{V_{REF}}{2} + \frac{I_{LIMIT} \times GAIN}{3}, \quad with \quad V_{REF} = 3V \quad and \quad Gain = 2.5V/A \tag{1}$$

$$SOX = \frac{V_{REF}}{2} \pm \left(GAIN \times I_{LIMIT}\right), \quad with \quad V_{REF} = 3V, \quad Gain = 2.5V/A, \quad I_{LIMIT} = 0.6A \tag{2}$$

The DRV8376 implements four kinds of protection:

- Overcurrent protection – overcurrent event is sensed by monitoring the current flowing through FETs. If the current through a FET exceeds the overcurrent threshold for longer than the deglitch time, an OCP event is recognized, and action is done according to the OCP_MODE bit.
- Under-voltage detection – implements an UVLO on both VM Supply, AVDD, GVDD and VCP supplies. When either of above supply voltage is below the threshold voltage of UVLO, all of the integrated FETs, driver charge-pump and digital logic controller are disabled.
- Thermal warning and shutdown – monitor the die temperature in the device and indicates a warning or fault when the threshold is exceeded. All the FETs are disabled, the charge pump is shut down, and the nFAULT pin is driven low when thermal shutdown (OTS) triggered.

Above three kinds of faults are indicated on nFAULT pin which is the open-drain output. Once asserted, the active low fault signal remains asserted as long any of the three faults exist.

3.5 System Power Management

Figure 3-6 shows the power supply tree. A wide input voltage DC/DC buck module TLVM13630 is designed to generate the 5V rail for the power management integrated circuit (PMIC). The PMIC TPS65035x device is a highly integrated power management IC which combines three step-down converters and one low-dropout (LDO) regulator. These three step-down converters can output three independent voltage rails 3.3V, 1.8V and 1.2V respectively. The 3.3V supplies all the IO voltage of MCU and another analog parts such as logic gate, transceivers. The 1.8V voltage rail is reserved without any load on this reference design. The 1.2V voltage rail supplies the core voltage of F28P65. All converters operate in a forced fixed-frequency PWM mode.

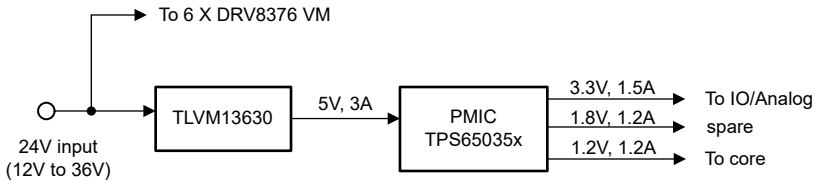


Figure 3-6. System Power Tree of TIDA-010992

3.6 Ethernet Physical Layer

This design leverages one DP83826A Ethernet PHYs to enable EtherCAT sub-device applications. Figure 3-7 shows one of the PHY circuitry with transformers and connector.

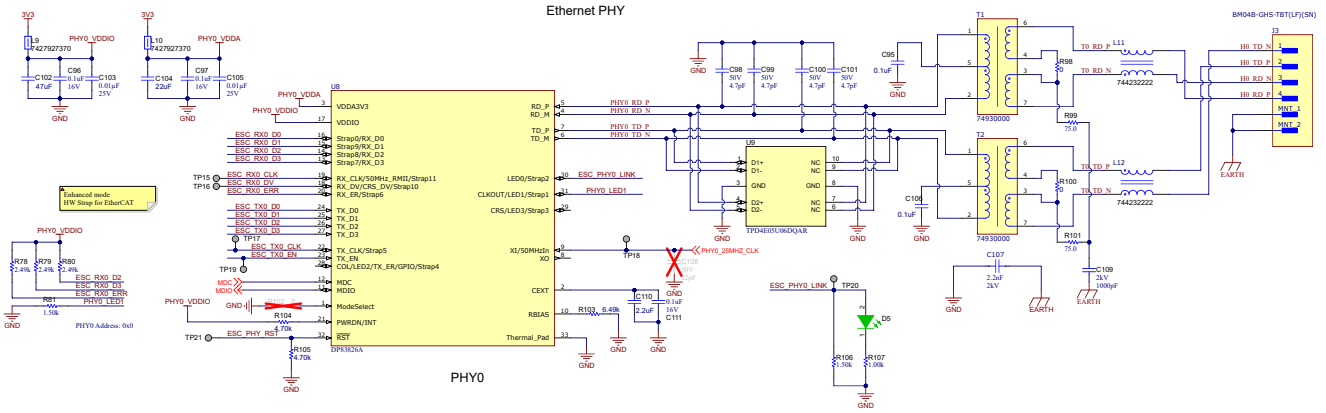


Figure 3-7. Ethernet PHY Schematic

Enhanced mode is selected by floating pin 1 of U8 to enable hardware strap configuration for EtherCAT usage. The R78 to R81 are strap resistors. See the How and Why to Use the DP83826 for EtherCAT® Applications application note for the details. Both the analog power (VDDA3V3) and digital IO power (VDDIO) are decoupled by ferrite bead L9 and L10. Media Independent Interface (MII) is used for minimum latency on the Ethernet signal path to connect between PHY and medium access control (MAC) layer. ESD diode U9 is put on the Media Dependent Interface (MDI) differential lines to suppress the noise. Discrete transformers (T1, T2), common mode choke (L11, L12) and connector (J3) are implemented instead of integrated RJ45 port to reduce the PCB space. R99, R101 and C109 are connected as Bob-smith termination to reduce the noise also. C107 is connected between board ground and earth to suppress interference.

4 Hardware, Software, Testing Requirements, and Test Results

4.1 Hardware Requirements

4.1.1 TIDA-010992 PCB Overview

Figure 4-1 and Figure 4-2 show labeled photos of the top and bottom of the PCB.

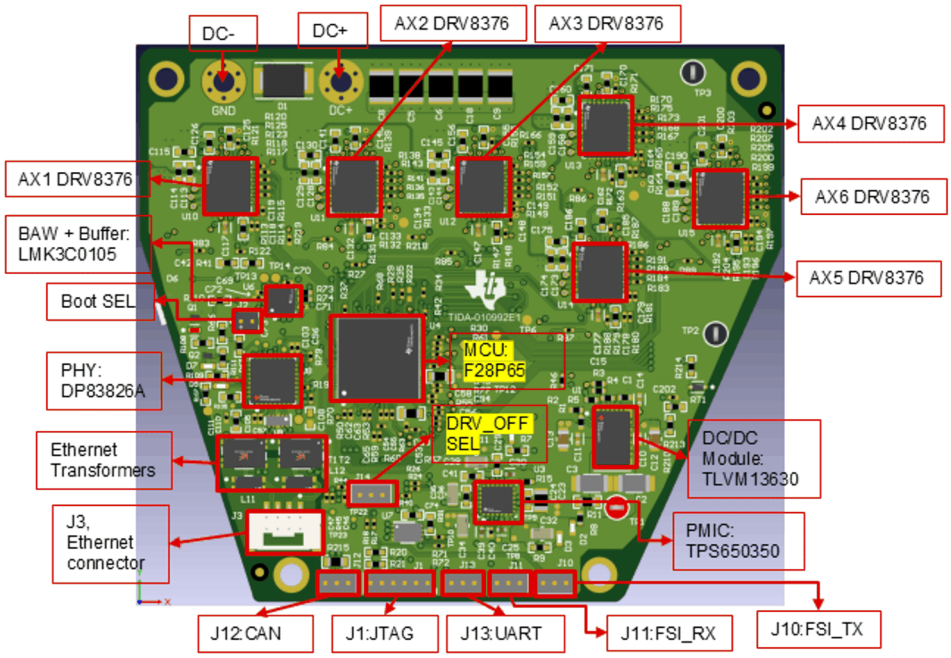


Figure 4-1. TIDA-010992 PCB Top View

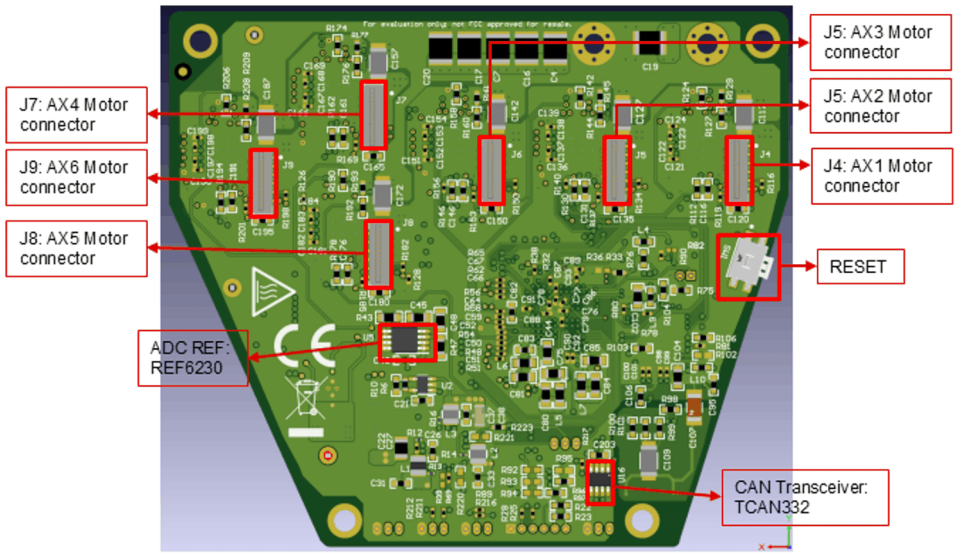


Figure 4-2. TIDA-010992 PCB Bottom View

4.1.2 TIDA-010992 Hardware Settings

To enable the TIDA-010992 board, DC voltage 24V (or lower voltage which depends on the motor rated) is required to be applied between DC+ and GND through holes located on the top left of the PCB. The motor power cable including the encoder signals are connected to J4 to J9 motor connectors for axis 1 to axis 6 respectively. J1 is the JTAG connector for software code debugging. XDS110 JTAG Debug Probe can be

connected to J1. J2 is the boot mode selection jumper. With J2 shorted, MCU boots from serial communication interface (SCI) or wait mode is enabled. With J3 opened, the flash mode is enabled as the MCU boot mode. J13 is the UART connector and it can also be connected to the XDS110 AUX pins to print the information on terminals or transmit data through UART communications. J3 is the Ethernet connector which can be connected to the EtherCAT MainDevice or other EtherCAT SubDeivce node. J12 is the CAN-FD interface which is reserved for communicating with other boards. J10 and J11 are connectors for FSI Transmit and Receive respectively which are also reserved for communicating with other boards. Figure 4-3 shows the overview hardware setup of TIDA-010992. Figure 4-4 shows the motor cable connection direction since the motor cables and the motor connectors have one-sided connection. Figure 4-5 shows the motor cables assembly for a humanoid hand. The fingers should connect to the pre-defined motor connectors accordingly.

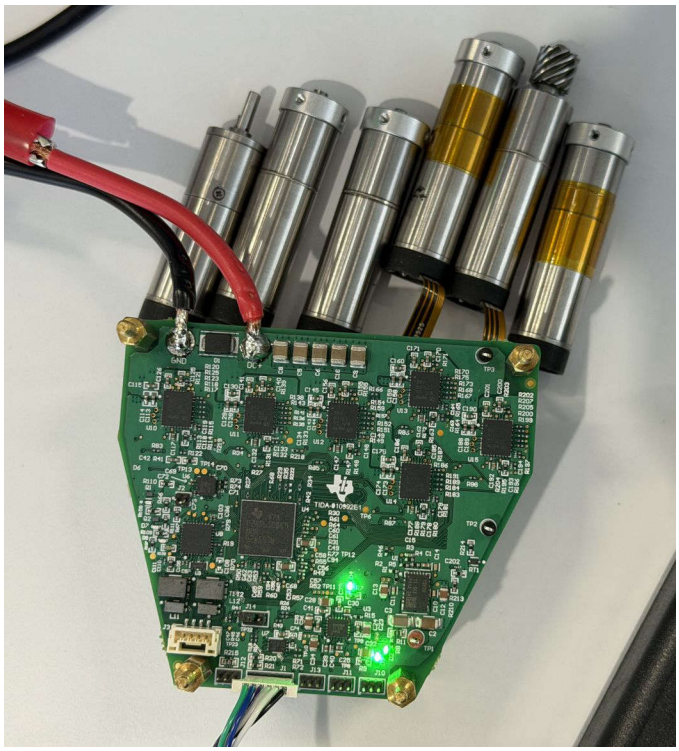


Figure 4-3. TIDA-010992 Overview Hardware Setup

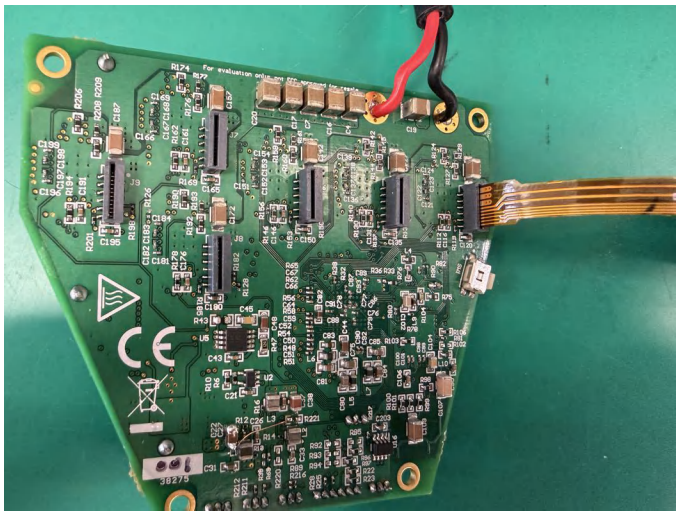


Figure 4-4. TIDA-010992 Motor Cable Connection

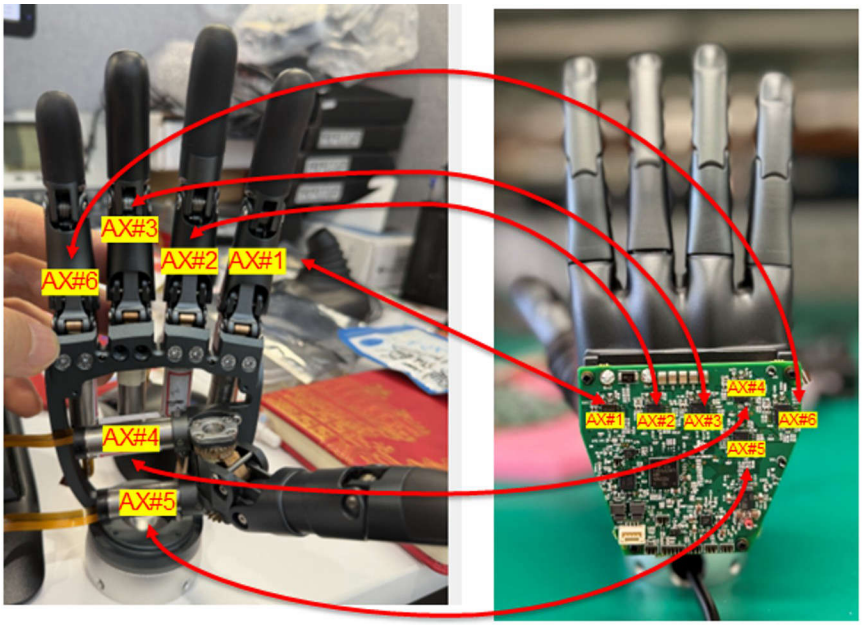


Figure 4-5. TIDA-010992 Motor Cable Assembly for Hand

4.2 Software Requirements

To validate this reference design, a TI internal test software has been developed for the F28P65. For F28P65 software support, see the C2000WARE-MOTORCONTROL-SDK Software development kit (SDK) | TI.com and C2000WARE Software development kit (SDK) | TI.com tool page and the C2000 microcontrollers forum - C2000™ microcontrollers - TI E2E support forums for C2000™ microcontrollers.

4.3 Testing and Results

4.3.1 Power Management and System Power Up and Power Down

This is used to validate the onboard power supplies, voltage, and sequence including 24V, 5V, 3.3V and 1.2V rails. Figure 4-6 and Figure 4-7 showcase the power up and down waveforms, respectively.

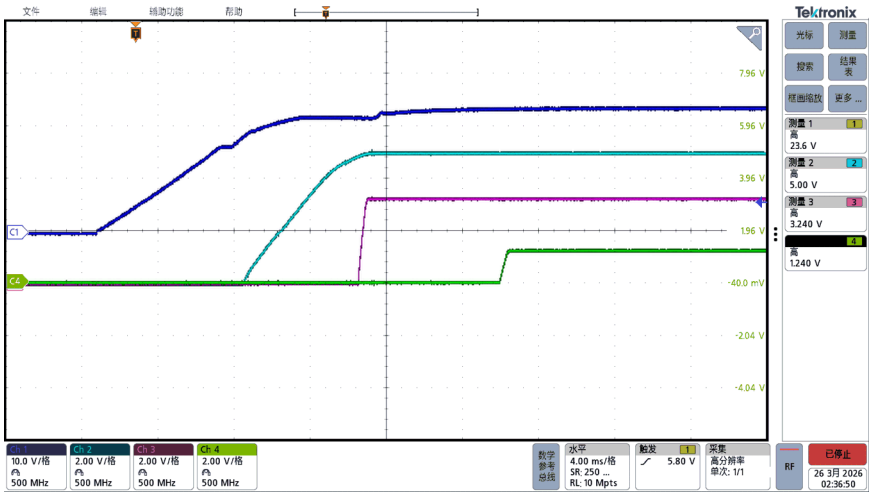


Figure 4-6. TIDA-010992 System Power Up

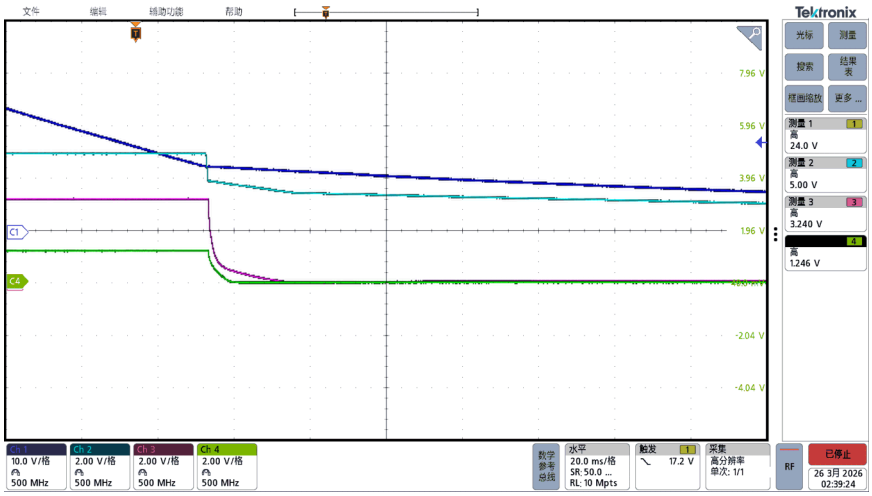
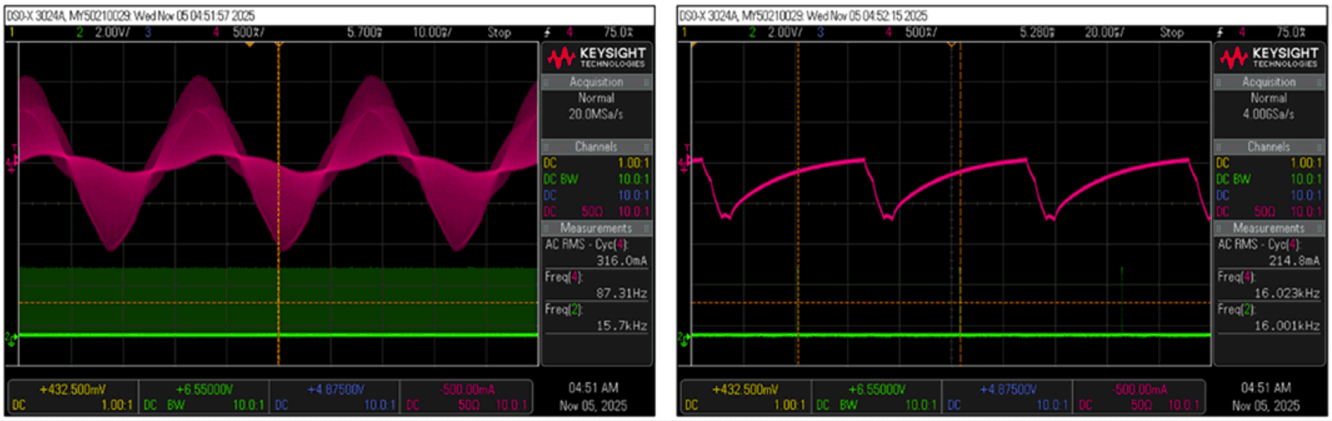


Figure 4-7. TIDA-010992 System Power Down

4.3.2 Current Feedback

The three-phase current per axis are sensed using an integrated current sensing feature eliminating the need for external sense resistors and then feedbacking the current data to three ADC modules inside the MCU to ensure simultaneous sensing. Figure 4-8 shows the current sense sampling with 16kHz PWM frequency with no-load motor. The peak ripple current is around 1A and the RMS ripple current per PWM cycle is around 214mA. Figure 4-9 shows the current sense sampling with 50kHz PWM frequency. The peak ripple current is around 250mA and the RMS ripple current per PWM cycle is around 98mA. From the comparison test results, we can see the motor ripple current reduced significantly with the PWM switching frequency increasing. To have better motor control performance and avoid over-heating the motor, 64kHz PWM switching frequency is implemented for this reference design. The motor type of humanoid hand is all coreless motor with very small inductance. So, the control PWM switching frequency should be set at more than 50kHz.



Pink = PhA current (Probe)
Green = EPWM_U ADC SOCA (OUTPUTXBAR
Peak ripple = 1A, RMS ripple per PWM cycle = 214mA

Figure 4-8. TIDA-010992 Current Sense Sampling With 16kHz PWM

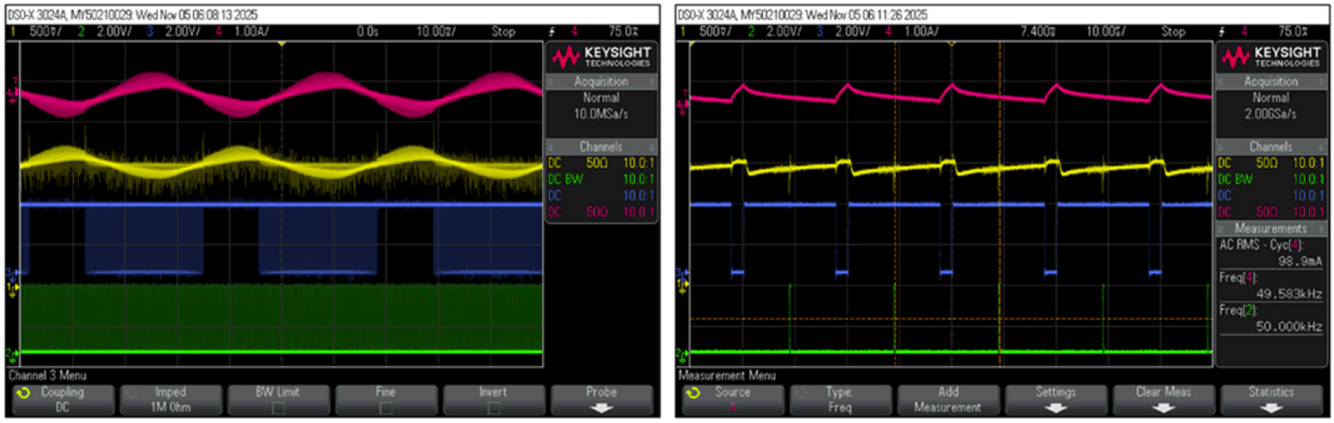


Figure 4-9. TIDA-010992 Current Sense Sampling With 50kHz PWM

4.3.3 Three-Phase Half-Bridge Motor Driver Power Stage Switch Node

Figure 4-10 and Figure 4-11 outline the switching voltage, turn-on and off propagation delay with 0.3A output phase current. There is no obvious transient on the switching node. The turn-on propagation delay of phase C axis 1 is around 88ns and turn-off propagation delay is around 140ns. Figure 4-12 and Figure 4-13 show the slew rate of rising edge and falling edge which are 600V/us and 258V/us respectively. The slew rate of DRV8376 is configurable by SPI. For this reference design, the slew rate is set as 250V/us.

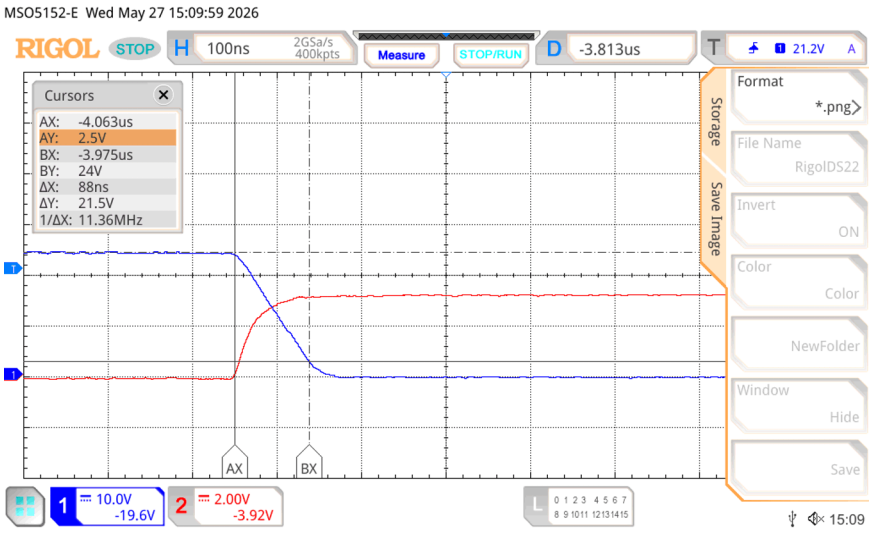


Figure 4-10. Turn-on Propagation Delay

Figure 4-11. Turn-off Propagation Delay

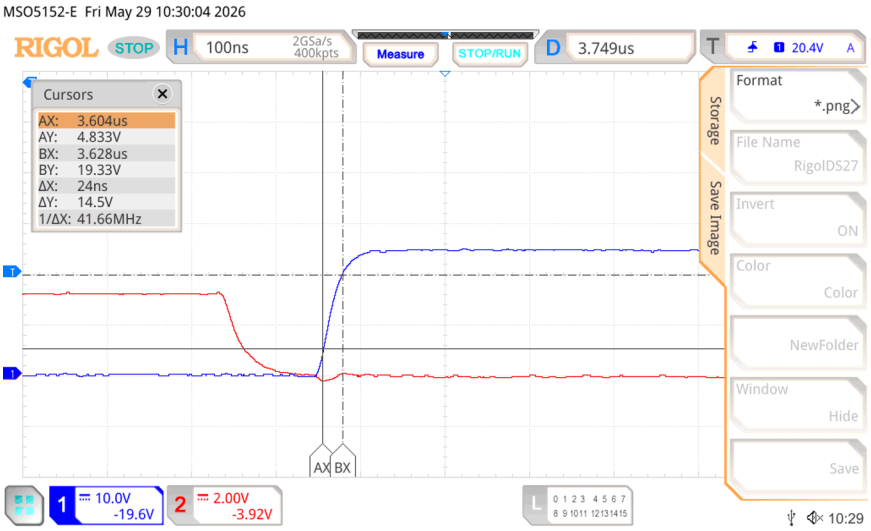


Figure 4-12. Rising Edge Slew Rate

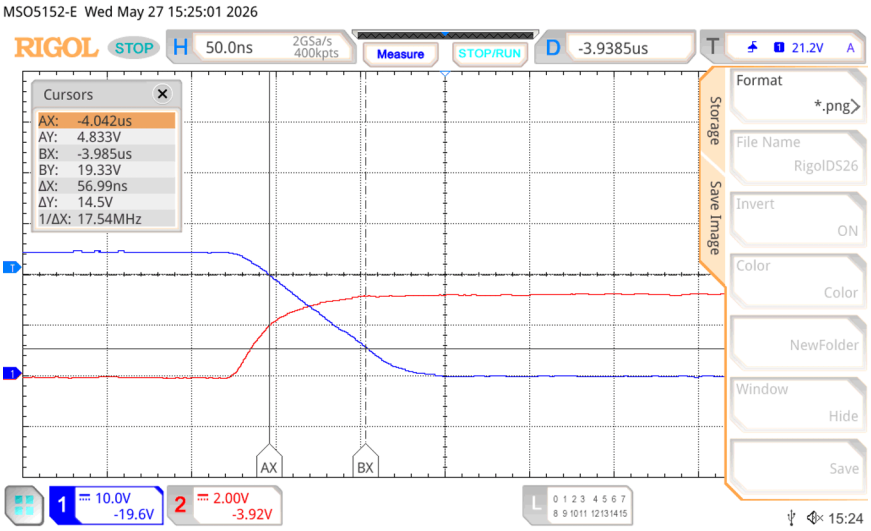


Figure 4-13. Falling Edge Slew Rate

4.3.4 Multi-Axis Motor Control Scheme Verification

Figure 4-14 shows the verification for 6-axis motor control scheme. Each channel represents the motor control FOC loop interrupt service routine (ISR) function for each axis. 6 GPIOs are configured toggling during the beginning and the end of motor control ISRs for each axis. From the test results, all 6-axis FOC loops are within 62.5us cycle time and without any overlap. The FOC loop of speed and current control for each axis will take around 7.41us.

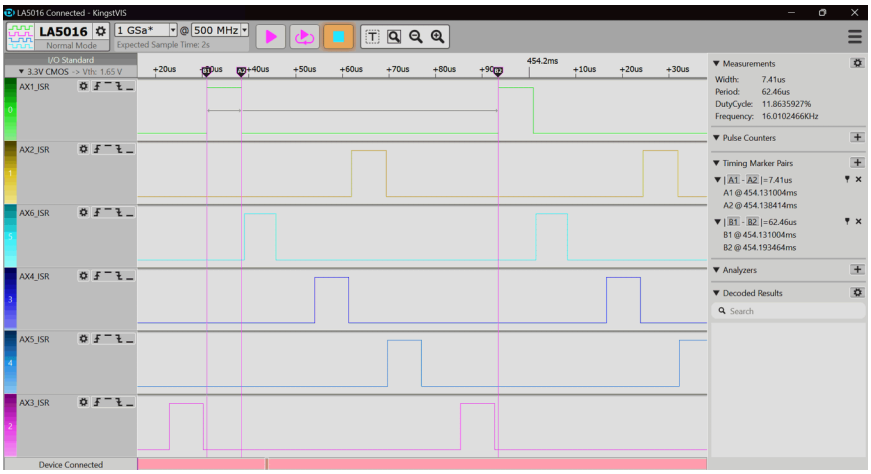


Figure 4-14. Verification of 6-axis Motor Control Sheme

4.3.5 System Thermal Measurements

The thermal measurement testing is done at a lab temperature of 25°C. The TIDA-010992 board is powered by a 24V DC source and connected to 6 standalone motors. The rated current of the motor is 0.4A. We set reference Iq current with 0.3A to spin 6 motors with closed current loop. The PWM carrier frequency operates at 64kHz. The motor speed operates at 5Hz. Figure 4-15 shows the thermal test results, neither a heat sink nor a fan operates, hence only natural convection of the TIDA-010992 PCB applies. The temperature rise of MCU F28P65 is around 31 degrees with room temperature 28.1 degrees and the hottest power stage DRV8376 is axis 5 with 30.3 degrees temperature rise.

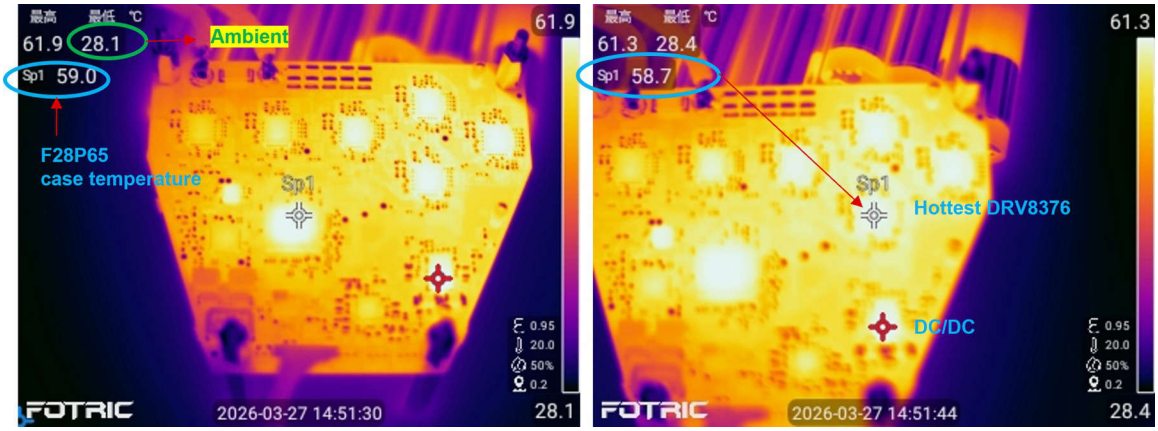


Figure 4-15. TIDA-010992 Temperature Rise Rest Results

5 Design and Documentation Support

5.1 Design Files

5.1.1 Schematics

To download the schematics, see the design files at TIDA-010992.

5.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-010992.

5.1.3 Layer plots

To download the layer plots, see the design files at TIDA-010992.

5.1.4 Altium Project

To download the Altium project files, see the design files CAD/CAE symbol at TIDA-010992.

5.1.5 Gerber Files

To download the Gerber files, see the design files at TIDA-010992.

5.1.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-010992.

5.2 Tools and Software

Tools

CCSTTUDIO	Code Composer Studio™ integrated development environment (IDE): download CCS 12 or 20 version for Microsoft® Windows® or Linux®
C2000-CGT	C28x/CLA code generation tools (CGT) - compiler
SYSCONFIG	Standalone desktop version of SysConfig: download SysConfig 1.26.2 for Microsoft Windows or Linux

Software

C2000 WARE	C2000Ware for C2000 MCUs
C2000 Motor Control SDK	MotorControl software development kit (SDK) for C2000 MCUs

5.3 Documentation Support

1. Texas Instruments, *C2000™ TMS320F28P65x Real-Time Microcontrollers datasheet*
2. Texas Instruments, *C2000™ TMS320F28P65x Real-Time Microcontrollers Technical Reference Manual (TRM)*

5.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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6 About the Author

CHEN GAO is a System Engineer in the Industrial System Robotics team at Texas Instruments and responsible for specifying and developing reference designs for industrial motor drive and robotics.

The authors recognize the excellent contribution from **HAN ZHANG** to support the software development of the TIDA-010992 reference design.

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2025) to Revision A (June 2026)	Page
• Updated entire document for full TIDA-010992 reference design support	2

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