

Cost-Effective IO-Link® Master Module Reference Design



Description

This reference design accelerates the development of IO-Link controller gateways by implementing an 8-port IO-Link gateway that supports up to 400µs cycle time, COM3, 1A per port on L+, and an additional DI/DO. The design supports various Ethernet-based industrial protocols such as EtherCAT®, PROFINET®, EtherNet/IP, and Modbus® transmission control protocol (TCP) using the AM261x integrated industrial communication subsystem (ICSS). The hardware design is tested and developed to meet industry-standard EMI/EMC requirements.

Features

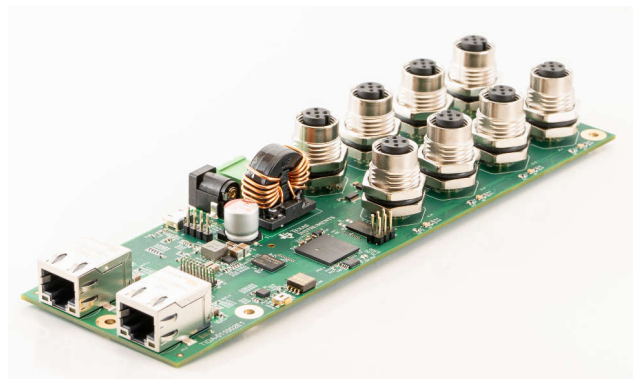
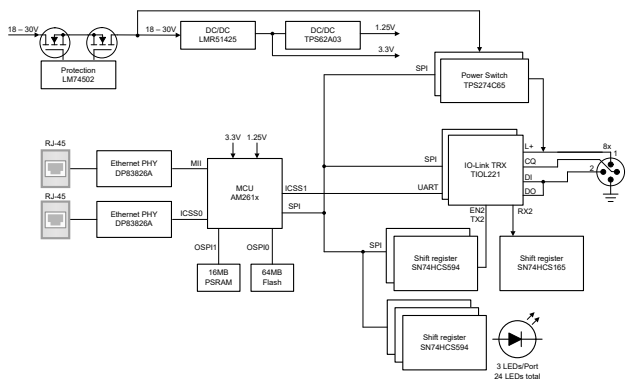
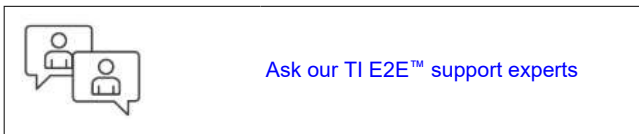
- 8 Port IO-Link controller supporting 1A per port, COM3, 400µs
- 10/100Mbit Multiprotocol Industrial Ethernet
- EtherCAT, Profinet, Ethernet/IP, MQTT, Modbus support
- EMI/EMC tested design

Applications

- [Communication module](#)
- [Stand-alone remote IO](#)

Resources

TIDA-011002	Design Folder
AM2612	Product Folder
DP83826AI	Product Folder
TIOL221	Product Folder
TPS274C65	Product Folder
LMR51425	Product Folder
TPS62A03	Product Folder
LM74502	Product Folder
SN74HCS594	Product Folder
TSM36CA	Product Folder
LMK3C0105	Product Folder



1 System Description

Sensors and actuators are the most basic units of automation, feeding information into and acting on instructions from networked systems. Traditionally, these devices connect to control units through interfaces that provide little intelligence, and thus exchange little or no configuration and diagnostic information. Installing a new device requires configuration by hand at the point of use. Without diagnostics, performing just-in-time preventive maintenance is impossible.

IO-Link (International Electrotechnical Commission [IEC] 61131-9) is an open standards protocol that addresses the need for intelligent control of small devices such as sensors and actuators. This standard provides low speed point-to-point serial communication between a device and a primary controller that normally serves as a gateway to a field bus and PLC. The intelligent link established enables ease of communication for data exchange, configuration, and diagnostics.

An unshielded three-wire cable as long as 20 meters, normally equipped with M12 connectors, establishes an IO-Link connection. Data rates range up to 230kbps with a non-synchronous minimum cycle time of 400 μ s, +10%. Four operating modes support bidirectional input/output (I/O), digital input, digital output and deactivation.

Security mechanisms and deterministic data delivery are not specified. A profile known as the IO Device Description (IODD) contains communication properties; device parameters; identification, process and diagnostic data; and information specifically about the device and manufacturer.

The many advantages of deploying an IO-Link system include standardized wiring, increased data availability, remote monitoring and configuration, simple replacement of devices and advanced diagnostics. IO-Link permits factory managers to receive sensor updates and plan for upcoming maintenance or replacement. Swapping out a sensing or actuation unit that needs replacement and configuring a new one from the PLC through the IO-Link master eliminates manual setup and reduces downtime. Switching production remotely from one configuration to another without visiting the factory floor facilitates easier product customization. Factories can upgrade production lines readily to IO-Link because the IO-Link master is backwards-compatible with existing standard I/O installations and cabling. These capabilities reduce overall costs, make more efficient processes, and increase machine availability.

2 System Overview

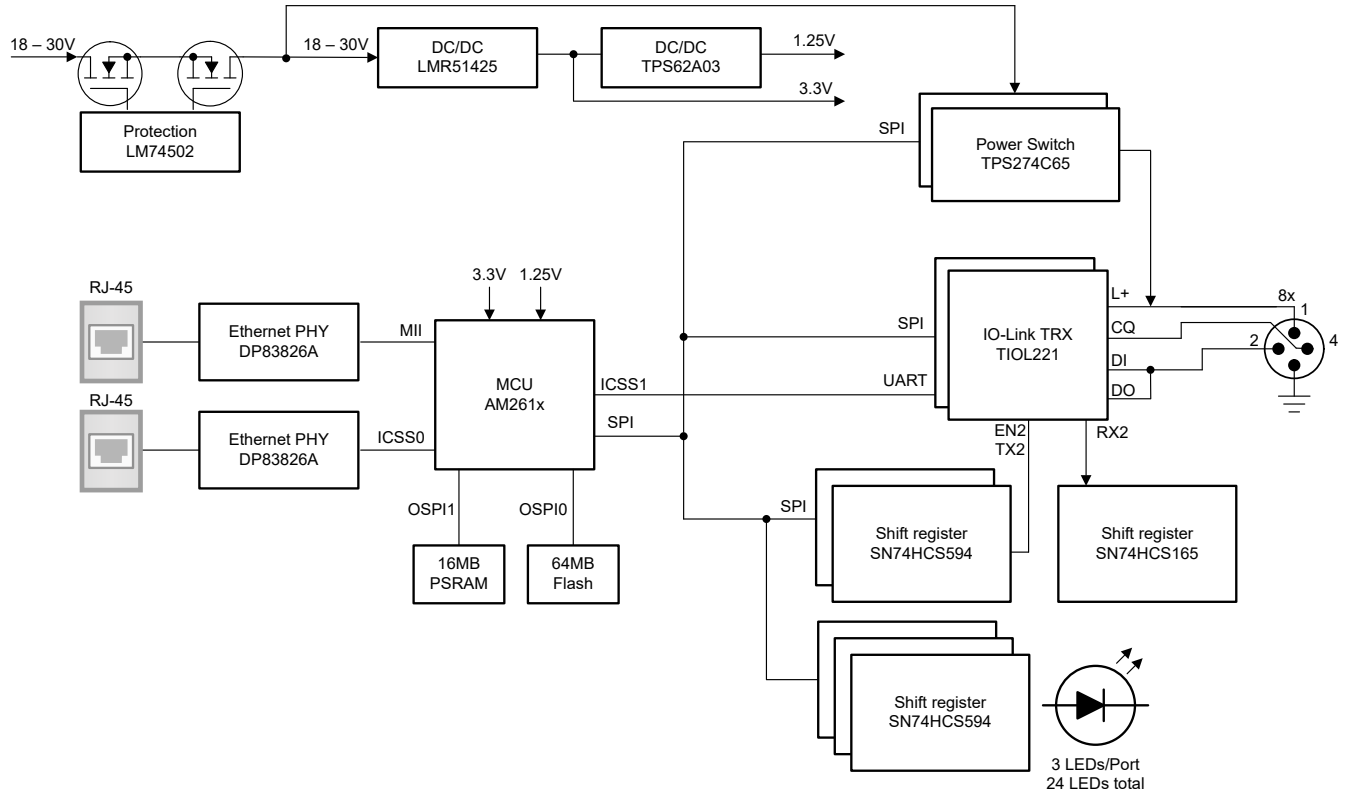


Figure 2-1. Block Diagram

2.1 Design Considerations

Figure 2-2 shows a simple block diagram of the reference design, which can be divided into four major blocks: Power supply, Ethernet Interface, IO-Link interface and processing.

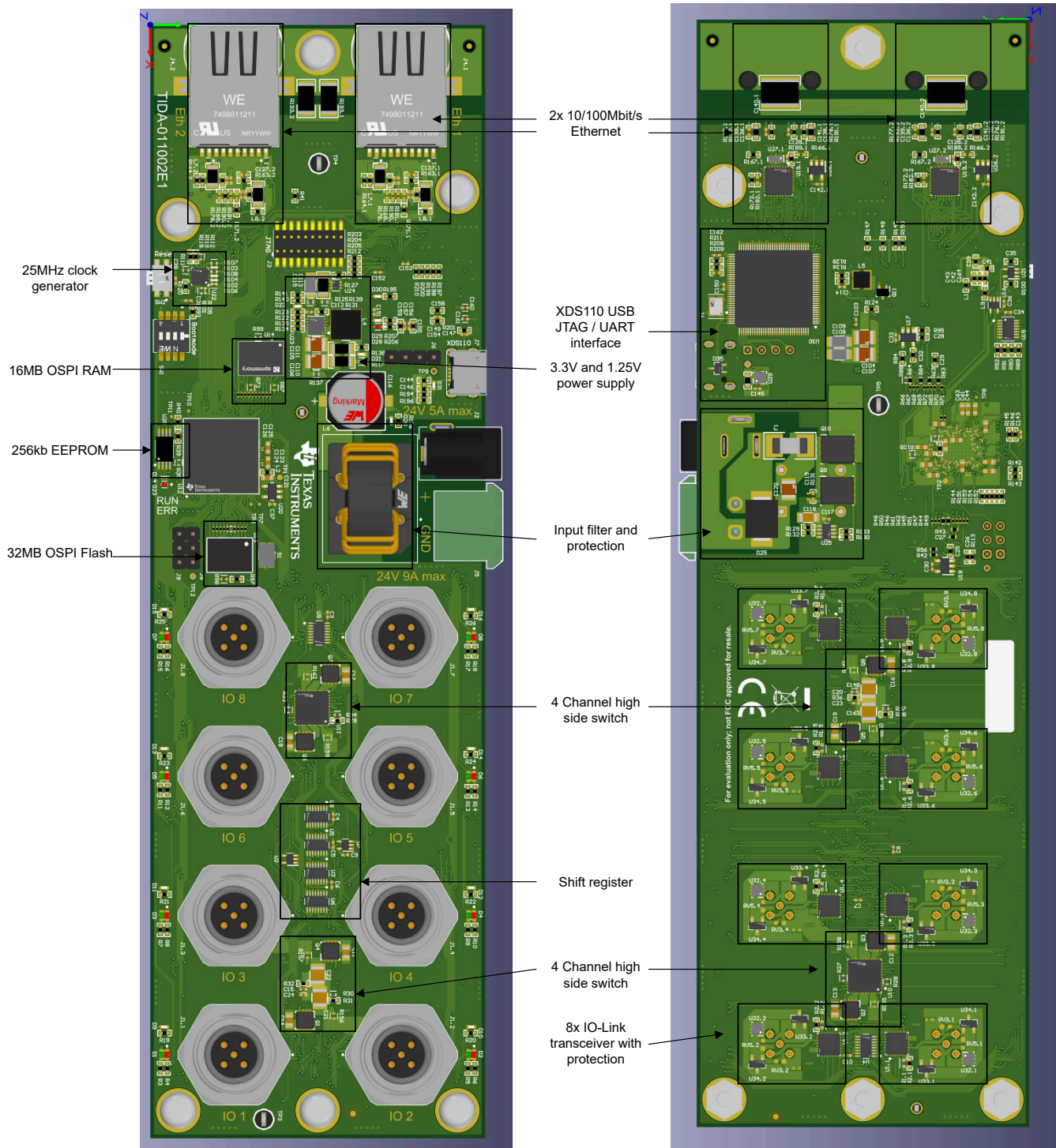


Figure 2-2. Functional Blocks of the Reference Design

Figure 2-2 shows where these blocks are located on the physical board. The power supply is two separate blocks, one implementing the input protection with LM74502 and one implementing the two DC/DC converters with LMR51425 and TPS62A03. The protection need more board space to handle some current. The power supply with the two DC/DC regulators uses a smaller area.

The Ethernet interfaces are implemented using DP83826A PHY and RJ45 connectors with integrated transformers to save space. The two PHYs (and the MCU) are clocked from one common clock source LMK3C0105 with 25MHz.

For the IO-Link ports, one TIOL221 per port is used so that a digital IO per port is also available. Four ports use one TPS274C65 high side switch to provide power on the L+ line so two TPS274C65 devices are needed for 8 ports. This design provides 1A on the L+ line and also implements a reverse current blocking on each output. The TPS274C65 has an SPI and includes an ADC to monitor the current consumption on every port.

An AM261 MCU is used for processing. The AM261 MCU has 16MB of external RAM available and 32MB of flash. The processor has a dual core Arm Cortex R5F with 500MHz. The two internal ICSS of the AM261 implement the IO-Link and any different industrial Ethernet interfaces.

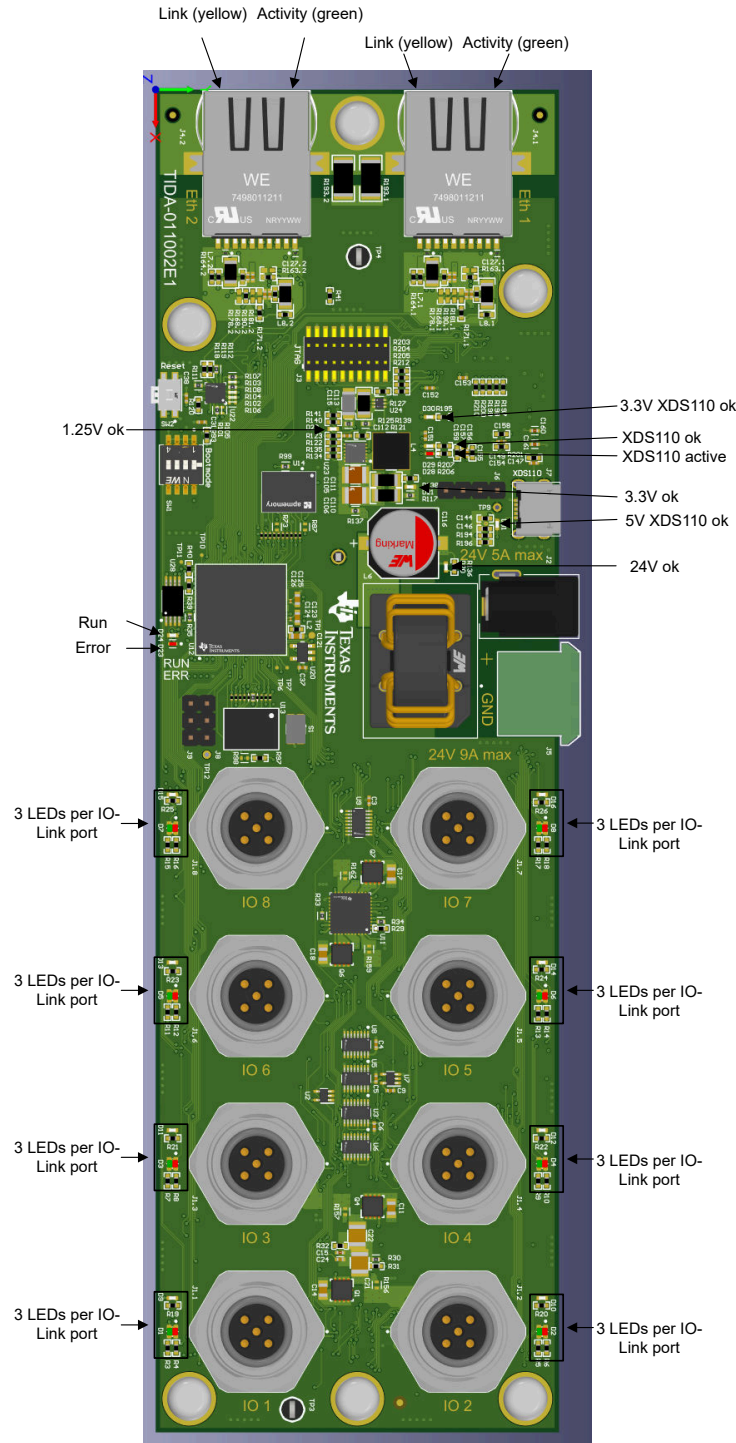


Figure 2-3. LEDs and Intended Use

Some LEDs in this reference design are used to show the hardware status and some can be freely programmed.

LED	Function
D20	24V after protection present
D21	3.3V available
D22	1.25V available
D23	Error LED controlled by AM261 GPIO 13
D24	Status LED controlled by AM261 GPIO 11
D28	Activity LED of XDS110 debugger
D29	Ready LED of XDS110 debugger
D30	3.3V of XDS110 available
D31	5V of XDS110 available
D1 - D16	LEDs next to IO-Link ports, three LEDs per port, freely programmable through shift register
Internal LEDs on RJ45 connector	Link and Activity LEDs (reprogrammable through MDIO registers of Ethernet PHY)

2.2 Highlighted Products

2.2.1 AM2612

The AM261x Sitara® Arm® Microcontrollers are part of Sitara AM26x real-time MCU families designed to meet the complex real-time processing needs of next generation industrial and automotive embedded products. With scalable Arm Cortex® R5F performance and an extensive set of peripherals, AM261x device is designed for a broad range of applications while offering safety features and optimized peripherals for real time control.

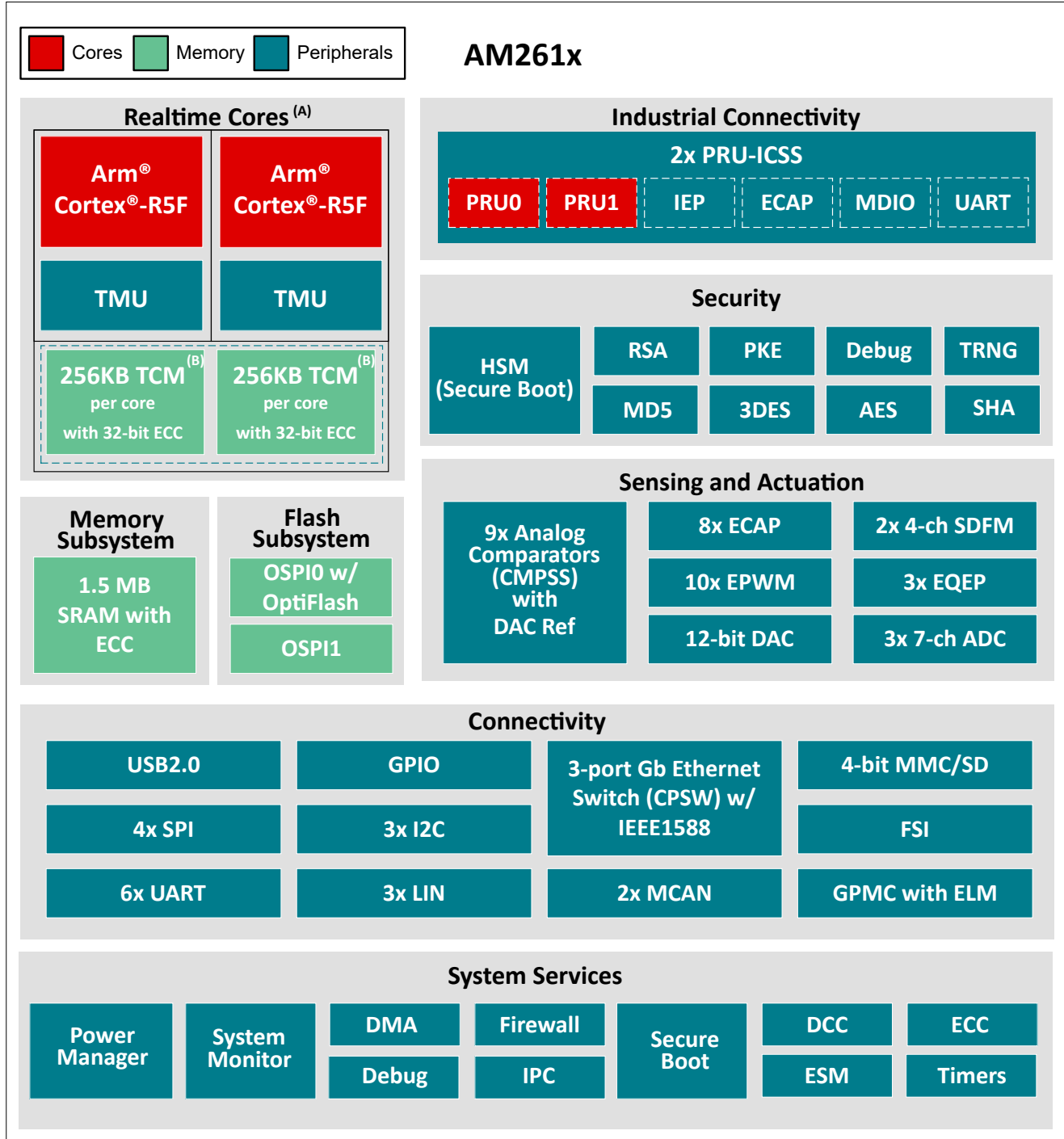


Figure 2-4. AM261x Functional Block Diagram

Key features and benefits:

- Peripherals supporting system level connectivity such as Gigabit Ethernet, USB, OSPI/QSPI, CAN, UARTs, SPI and GPIOs.
- Granular firewalls managed by hardware security manager (HSM) enable developers to implement stringent security minded system design requirements.
- Up to two R5F cores in cluster with 256KB of shared tightly coupled memory (TCM) per core along with 1.5MB of shared SRAM, greatly reducing the need for external memory.

2.2.2 TIOL221

The TIOL221 transceiver integrates dual low-power output drivers with active reverse polarity protection. When the device is connected to an IO-Link master through a three-wire interface, the controller can initiate communication, and exchange data with the remote node while the TIOL221 acts as a complete physical layer for the communication. The device also integrates an auxiliary DI channel.

The device is capable of withstanding up to 1.2kV (500Ω) of IEC 61000-4-5 surge and features integrated reverse polarity protection. In addition to the SPI for configurability and expanded diagnostic capability, a simple pin-programmable interface allows easy interfacing with the controller circuits. The output current limit can be configured using either an external resistor or per-configured limits through the SPI. TIOL221 can be configured to drive wake-up pulse and be used in IO-link master applications. Fault reporting and internal protection functions are provided for undervoltage, overcurrent and overtemperature conditions.

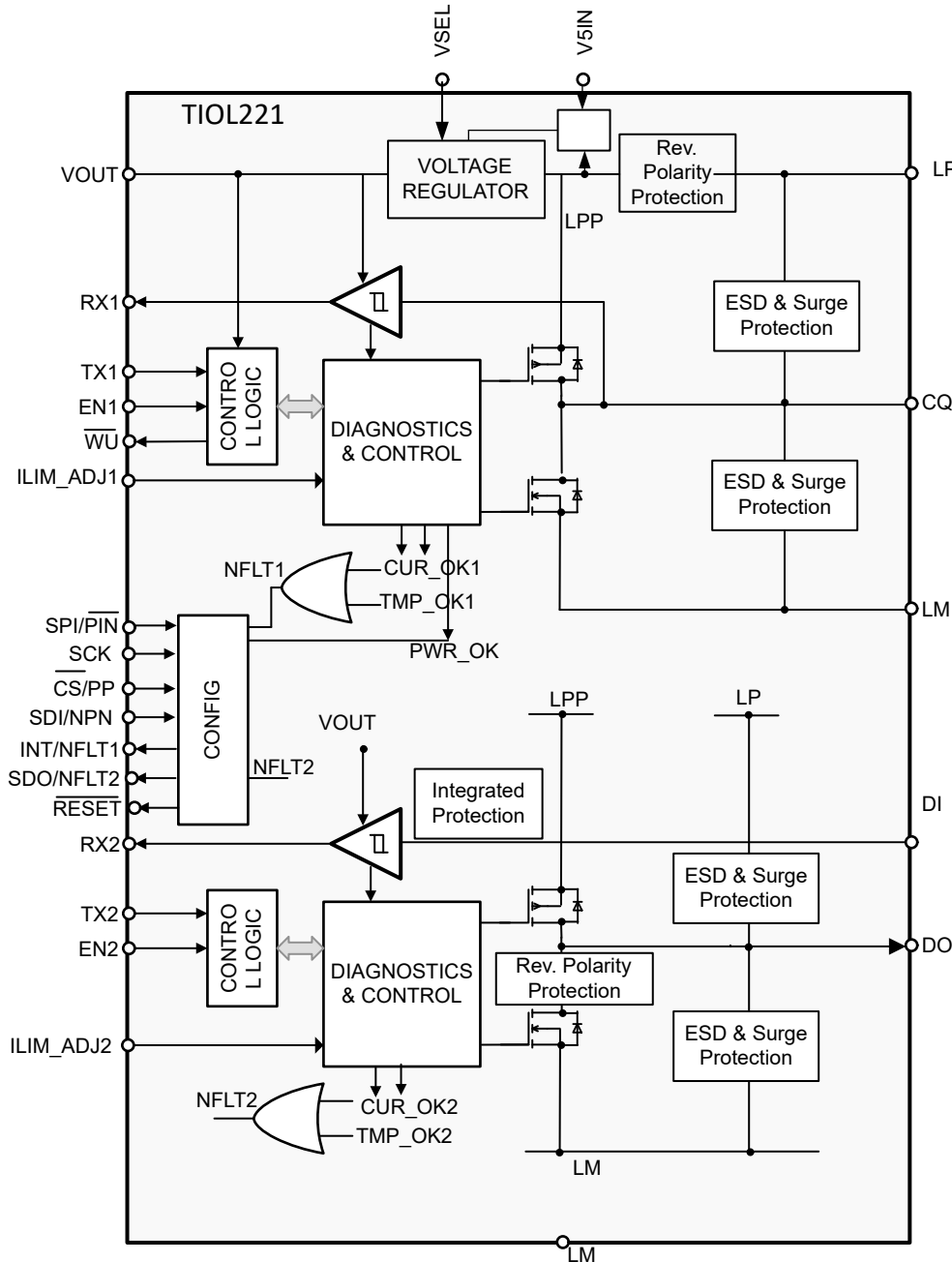


Figure 2-5. Block Diagram

2.2.3 DP83826A

The DP83826Ax offers low and deterministic latency, low power and supports 10BASE-Te, 100BASE-TX Ethernet protocols to meet stringent requirements in real-time industrial Ethernet systems. The device includes hardware bootstraps to achieve fast link-up time, fast link-drop detection modes and dedicated reference CLKOUT to clock synchronize other modules on the systems.

The two configurable modes are BASIC and ENHANCED. BASIC mode is the standard Ethernet mode that uses a common Ethernet pinout. The ENHANCED Ethernet mode supports standard Ethernet mode and multiple industrial Ethernet fieldbus applications with the additional features and hardware bootstraps configuration.

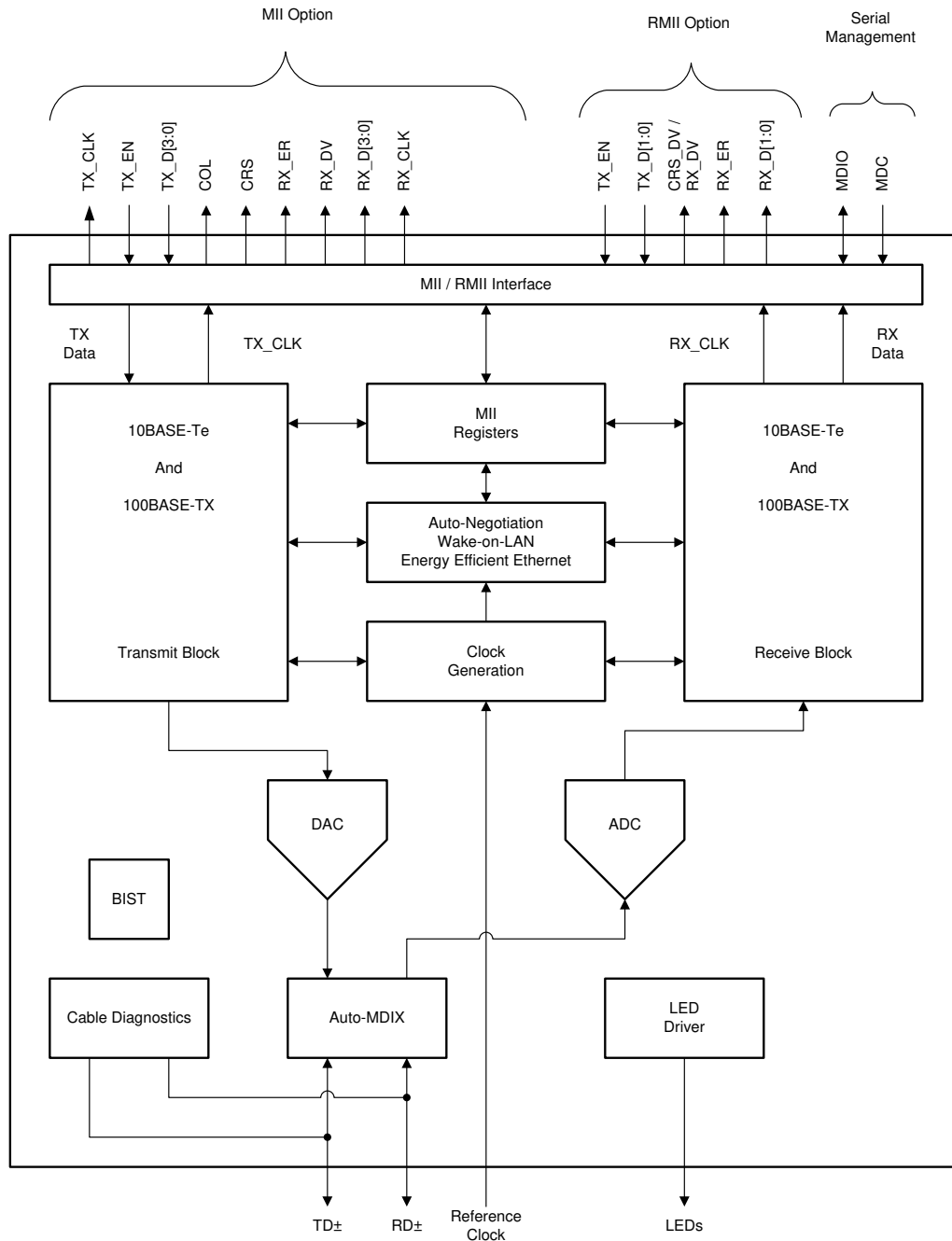


Figure 2-6. Functional Block Diagram

2.2.4 TPS274C65

The TPS274C65xS device is a quad-channel smart high-side switch with a serial interface (SPI) control and is designed to meet the requirements of industrial control systems. The low 72mΩ RDSON minimizes device power dissipation even when providing large output load current. The device integrates protection and diagnostic features to provide system protection even during harmful events like short circuits or load failures. The device protects against faults through a reliable current limit which is adjustable from 250mA to 2.45A to provide protection regardless of output load current. The TPS274C65xS has a configurable inrush current period which sets a higher current limit during turn-on for high inrush current loads, charging capacitive loads faster, or driving incandescent bulbs.

The TPS274C65xS also provides accurate current sense and an integrated analog to digital converter (AS) that allows for improved load diagnostics. By reporting load current digitally, the device allows for communication over any isolation barrier while enabling predictive maintenance and load diagnostics to improve system lifetime. Additional diagnostic features, such as on-state or off-state open load detection and short-to-supply detection, are also integrated.

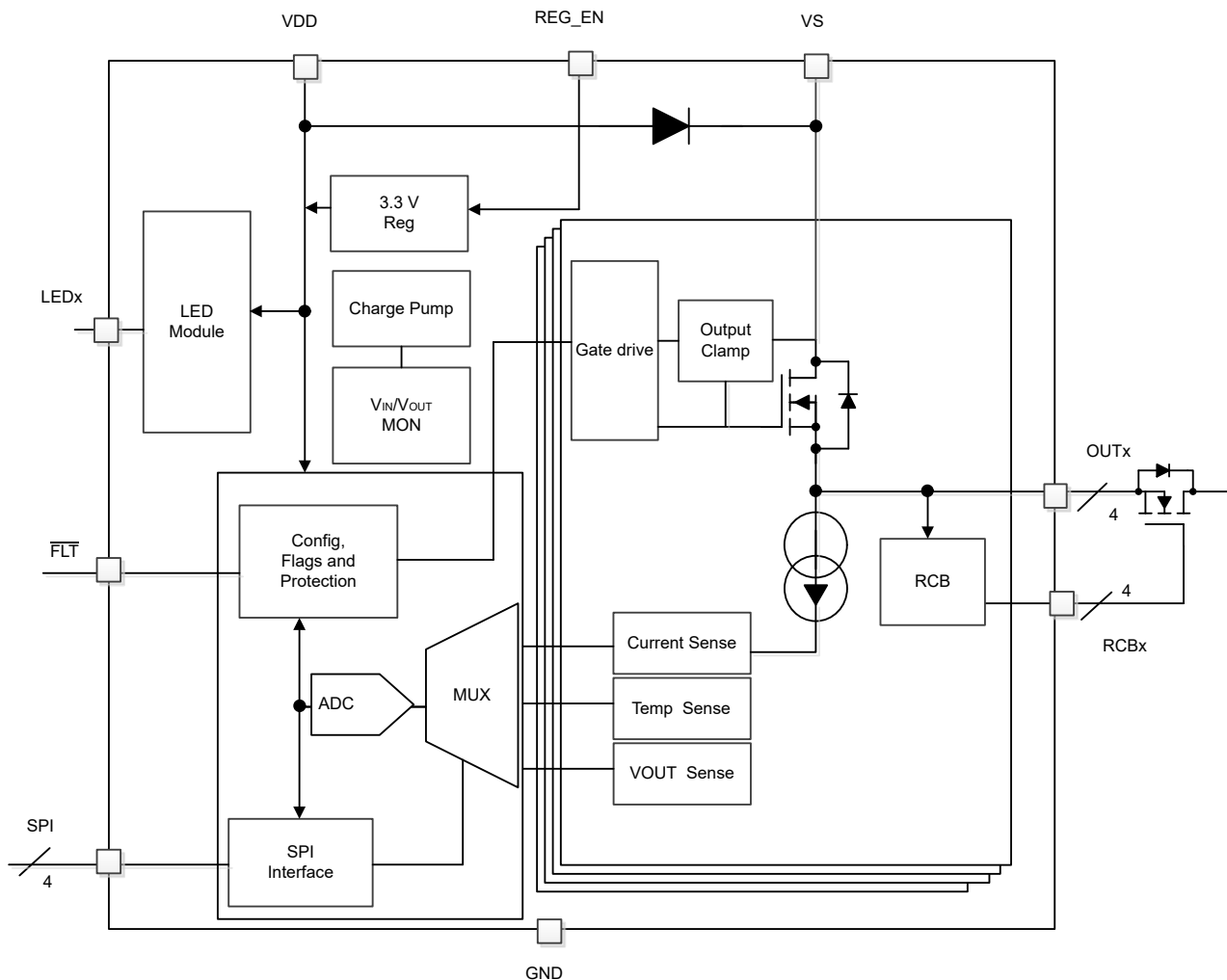


Figure 2-7. Functional Block Diagram

2.2.5 LMK3C0105

The LMK3C0105 is a 5-output reference-less clock generator with SSC support. The device is based on TI proprietary Bulk Acoustic Wave (BAW) technology and provides ± 25 ppm clock outputs without any crystal or external clock reference. The device can provide 5 SSC clocks, 5 non-SSC clocks, or a mix of SSC and non-SSC clocks at the same time. Up to three different output frequencies can be generated across the five outputs. Each output channel can select either FOD as the frequency source to generate four LVCMOS clocks. The REF_CTRL pin functions as a fifth LVCMOS clock output, and can select either FOD as the source.

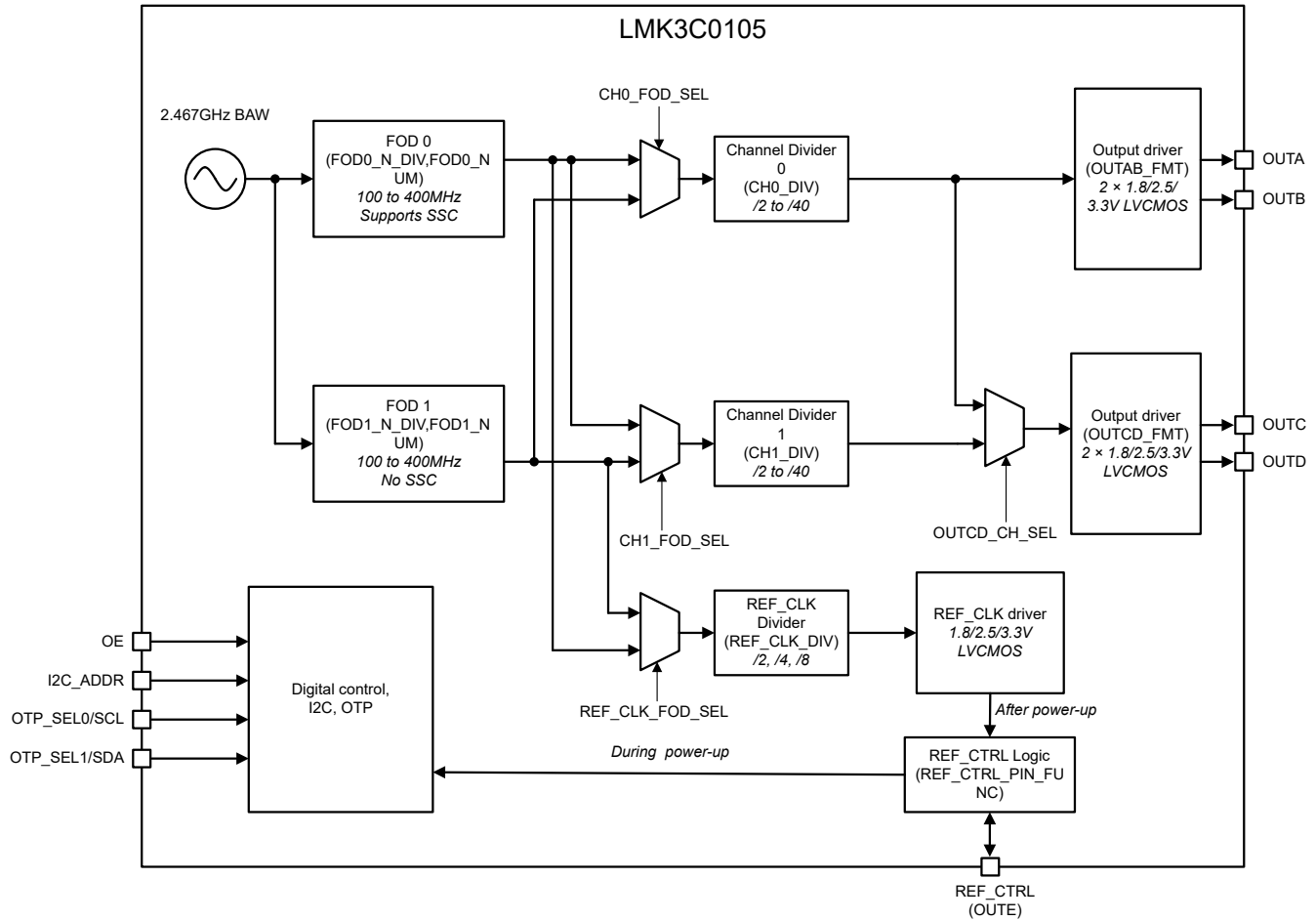


Figure 2-8. LMK3C0105 Functional Block Diagram

2.2.6 LM74502

The LM74502 and LM74502H are controllers which operate in conjunction with an external back-to-back connected N-channel MOSFETs to provide a low loss reverse polarity protection and load disconnect device. The device can also be configured to drive the high side MOSFET as a load switch with overvoltage protection. The wide supply input range of 3.2V to 65V can control many popular DC bus voltages such as 12V, 24V and 48V input systems.

The device can withstand and protect the loads from negative supply voltages down to -65V. The LM74502 and LM74502H do not have reverse current blocking and are only designed for input reverse polarity protection.

The LM74502 controller provides a charge pump gate drive for an external N-channel MOSFET. with the enable pin low, the controller is off and draws approximately 1µA of current, thus offering low system current when put into sleep mode. LM74502 and LM74502H offers programmable overvoltage and undervoltage protection which cuts off the load from the input source in case of these fault events. The devices are available in a 2.9mm × 1.6mm 8-pin DDF package and are specified over a -40°C to +125°C temperature range.

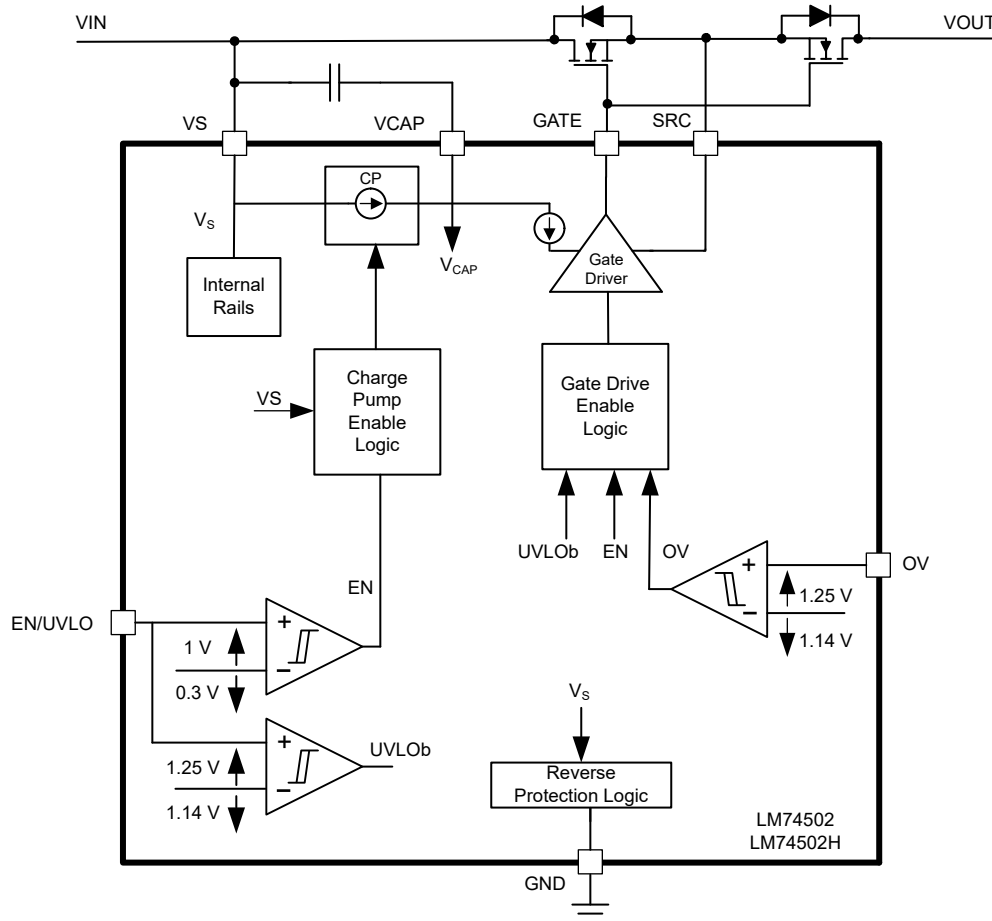


Figure 2-9. Functional Block Diagram

2.2.7 LMR51425

The LMR514x5 is a wide-VIN, easy-to-use, synchronous buck converter capable of driving up to 2.5A or 3.5A load current. With a wide input range of 4V to 36V, the device is designed for a wide range of industrial applications for power conditioning from an unregulated source.

The LMR514x5 features adjustable switching frequency from 200kHz to 1.1MHz with an external resistor, which provides the flexibility to optimize either efficiency or external component size. The device has pulse frequency modulation (PFM version) to realize high efficiency at light load, and forced pulse width modulation (FPWM version) to achieve constant frequency, and small output voltage ripple over the full load range. Soft-start and compensation circuits are implemented internally, which allows the device to be used with minimum external components.

The device has built-in protection features, such as cycle-by-cycle current limit, hiccup mode short-circuit protection, and thermal shutdown in case of excessive power dissipation. The LMR514x5 is available in a WSON-12 package.

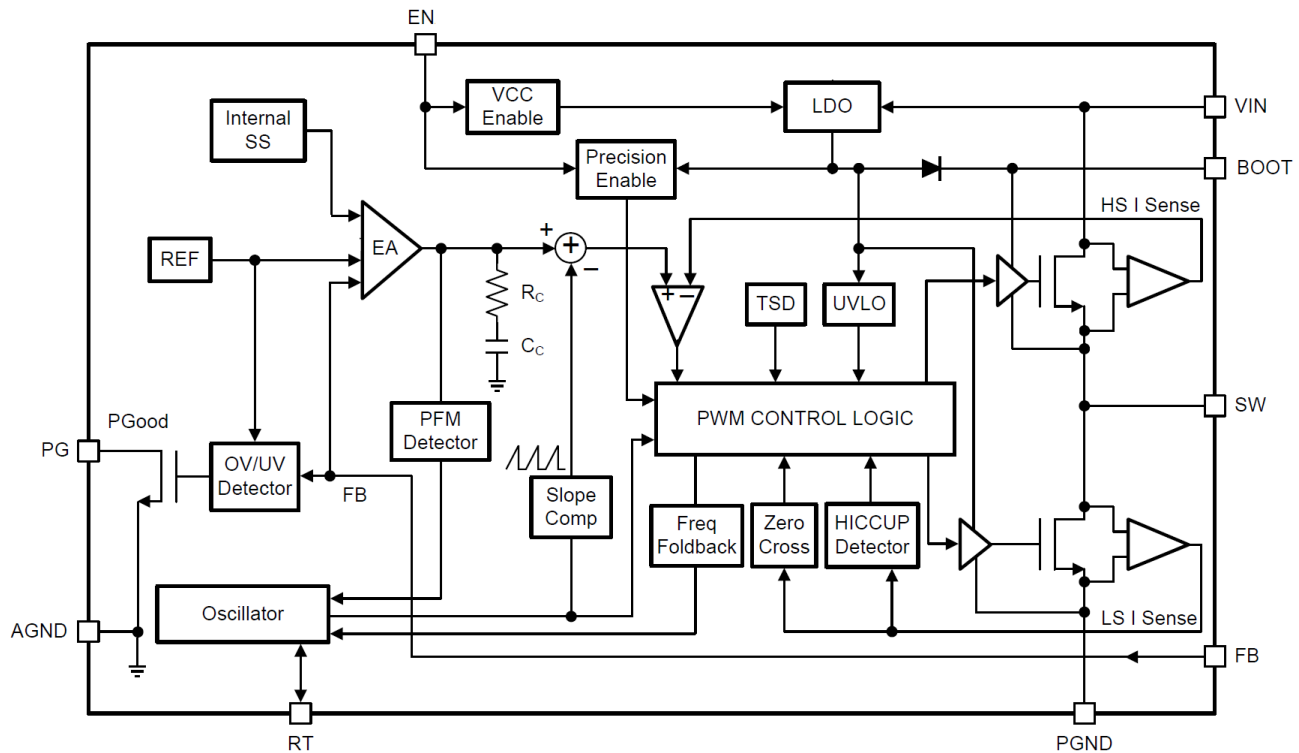


Figure 2-10. Functional Block Diagram

2.2.8 TPS62A03

The TPS62A03 and TPS62A03A are synchronous, step-down, buck DC/DC converters designed for high efficiency and compact design size. The devices integrate switches capable of delivering an output current up to 3A. At medium to heavy loads, the devices operate in pulse width modulation (PWM) mode with 2.2MHz switching frequency. At light load, the TPS62A03 automatically enters power save mode (PSM) maintaining high efficiency over the entire load current range. The TPS62A03A variant of this device operates in PWM mode across the whole load current range with a fixed switching frequency. In shutdown, the current consumption is minimal for both devices.

The TPS62A03 and TPS62A03A provide an adjustable output voltage through an external resistor divider. An internal soft-start circuit limits the inrush current during start-up. Overcurrent protection and thermal shutdown protect device and application under fault conditions. A power good signal indicates that the output voltage is in correct regulation.

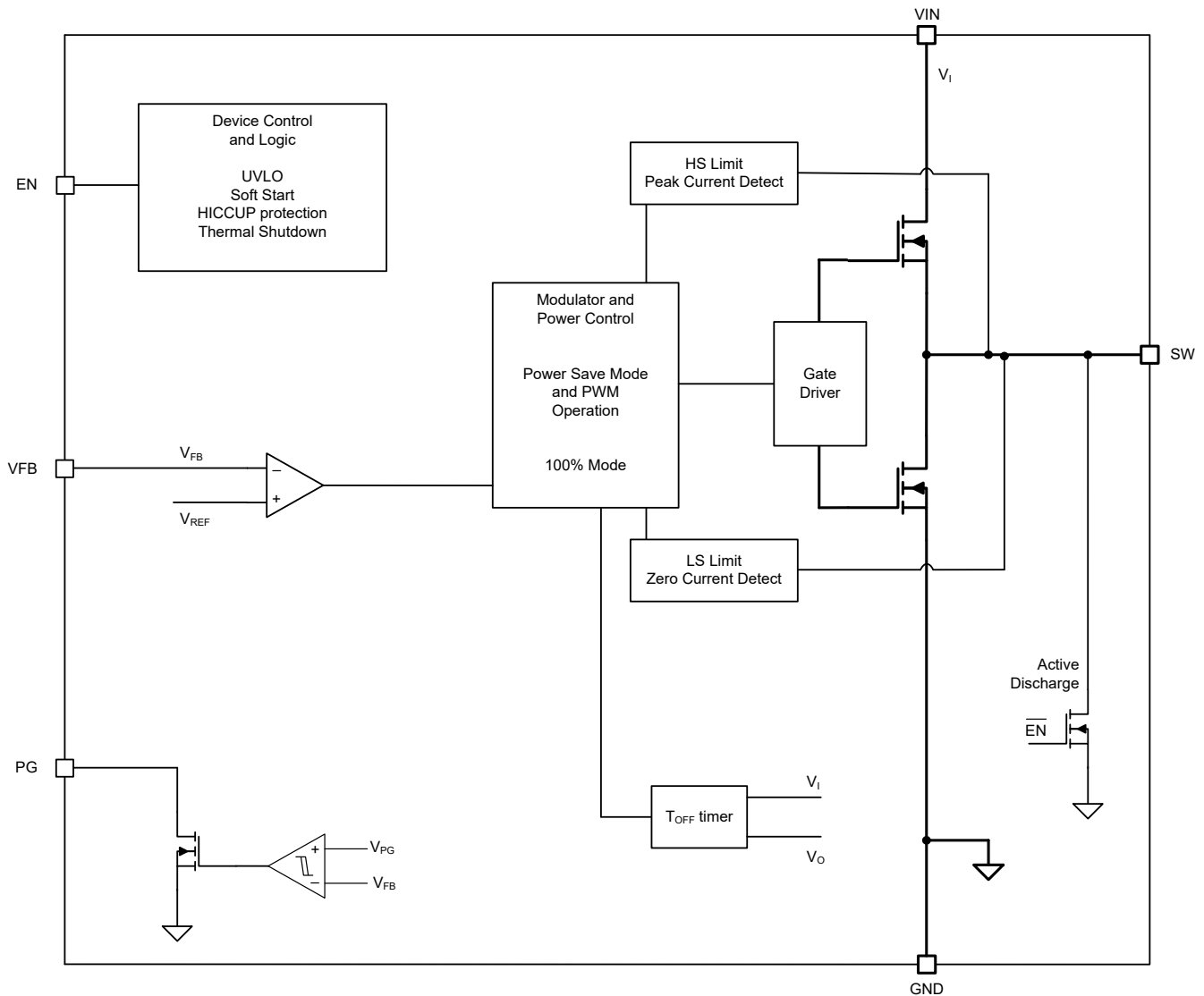


Figure 2-11. Functional Block Diagram

2.2.9 TSM36CA

The TSM36CA is a 36V, bidirectional TVS protection diode designed for clamping harmful transients such as ESD and surge. The TSM36CA robustly shunts up to 20A of IEC 61000-4-5 fault current to protect systems from high power transients or lightning strikes. The TSM36CA device is rated to dissipate ESD strikes up to $\pm 30\text{kV}$ (contact and air gap discharge) which exceeds the maximum level specified in the IEC 61000-4-2 international standard (Level 4).

Additionally, the TSM36CA is available in a small leaded SOT-23 (DBZ) package which is reduced in size by approximately 50% compared to the industry standard SMA package. The extremely low device leakage and capacitance puts minimal impact on the protected line.

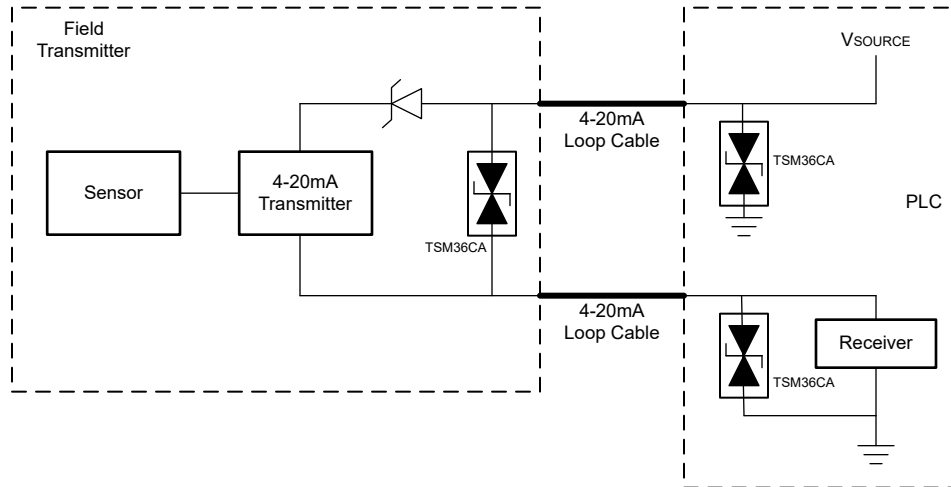


Figure 2-12. Typical Application Diagram

2.2.10 TVS3300

The TVS3300 robustly shunts up to 35A of IEC 61000-4-5 fault current to protect systems from high power transients or lightning strikes. The device offers an option to address to the common industrial signal line EMC requirement to survive up to 1kV IEC 61000-4-5 open circuit voltage coupled through a 42Ω impedance. The TVS3300 uses a unique feedback mechanism to provide precise flat clamping during a fault, keeping system exposure below 40V. The tight voltage regulation allows designers to confidently select system components with a lower voltage tolerance, lowering system costs and complexity without sacrificing robustness.

In addition, the TVS3300 is available in small 1mm × 1.1mm WCSP and 2mm × 2mm SON footprints which are designed for space constrained applications, offering up to a 90% reduction in size compared to industry standard SMA and SMB packages. The extremely low device leakage and capacitance has a minimal effect on the protected line. To provide robust protection over the lifetime of the product, TI tests the TVS3300 against 4000 repetitive surge strikes at high temperature with no shift in device performance.

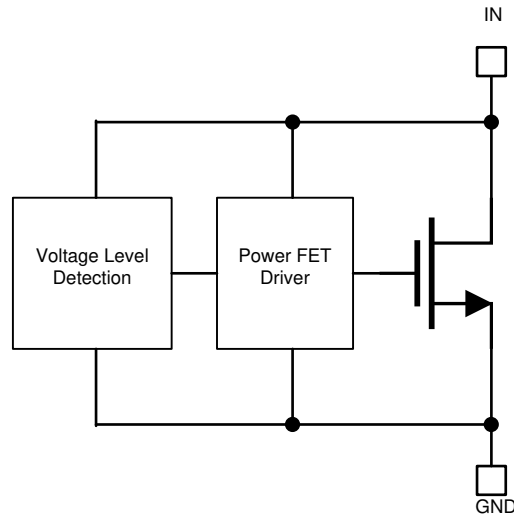


Figure 2-13. Functional Block Diagram

2.2.11 SN74HCS594

The SN74HCS594 device contains an 8-bit, serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. All inputs include Schmitt triggers which eliminates any erroneous data outputs due to slow, edged, or noisy input signals. The storage register has parallel outputs. Separate clocks and direct overriding clear (SRCLR, RCLR) inputs are provided for both the shift and storage register. A serial output (QH') is provided for cascading.

Both the shift register (SRCLK) and storage register (RCLK) clocks are positive edge triggered. If both clocks are connected together, the shift register is one count pulse ahead of the storage register.

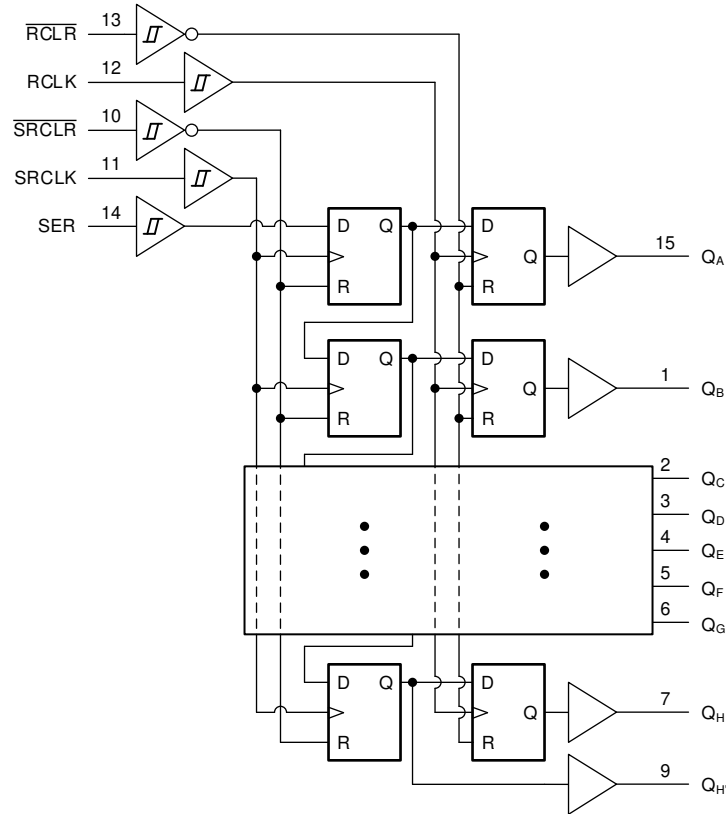


Figure 2-14. Logic Diagram (Positive Logic) for SN74HCS594

2.2.12 SN74HCS165

The SN74HCS165 is a parallel- or serial-in, serial-out 8-bit shift register with Schmitt-trigger inputs.

This device has two modes of operation: load data and shift data.

When the shift or load (SH/LD) input is held in the low state, the internal registers are loaded with data from the eight lettered inputs (A-H). This operation is asynchronous. In this state, the output (Q) has the same state as the input H, while the inverted output (\bar{Q}) has the opposite state.

When the shift or load (SH/LD) input is held in the high state, the internal registers hold the current state until a clock pulse is received. On the rising edge of the clock (CLK) input, data from the serial input loads into the first register, and the data in the internal registers shifts by one place. The initial value on the last register is deleted. The output (Q) is always in the same state as the last register, and the inverted output (\bar{Q}) has the opposite state. The clock inhibit (CLK INH) input can be held high to prevent clock pulses from being detected. CLK and CLK INH are interchangeable inputs.

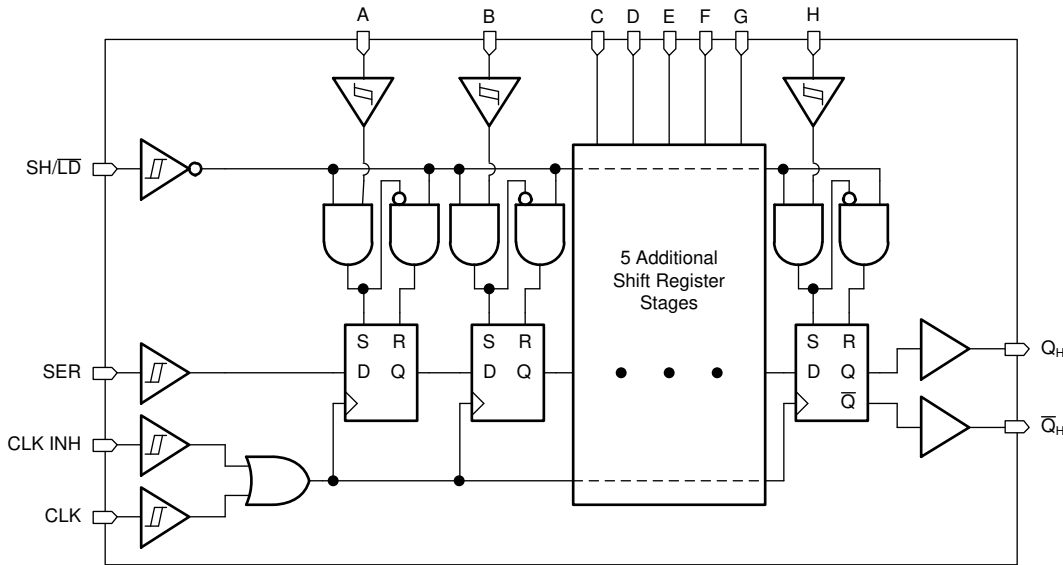


Figure 2-15. Logic Diagram (Positive Logic) for SN74HCS165

2.2.13 ESD204

The low clamping and high differential bandwidth provided by ESD204 enables the device to cleanly pass high speed signals while providing robust protection to downstream devices. With a low capacitance of 0.55pF per channel, this device is designed for protecting high-speed interfaces up to 6Gbps such as HDMI 2.0, HDMI 1.4, USB 3.0 and Ethernet 1G. The low dynamic resistance and low clamping voltage maintains system level protection against transient events.

The ESD204 is offered in the industry standard USON-10 (DQA) package. The package features flow-through routing and 0.5mm pin pitch easing implementation and reducing design time.

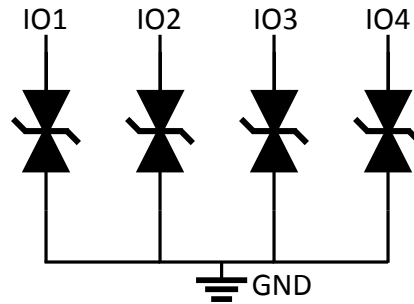


Figure 2-16. Functional Block Diagram

2.2.14 ESD441

The ESD441 is a unidirectional ESD protection diode for protecting data lines and other I/O ports. The ESD441 is rated to dissipate ESD strikes up to $\pm 30\text{kV}$ per the IEC 61000-4-2 international standard (greater than Level 4).

This device features a 1pF (typical) IO capacitance enabling high-speed interfaces protection for protocols such as USB 2.0. The extremely low dynamic resistance (0.1Ω) and clamping voltage (7.6V at 16TLP) is specified for system level protection against transient events.

The 30kV ESD rating and 6A surge provides robust transient protection in a tiny package for protecting 5.5V power rails in portable electronics and other space constrained applications such as wearables.

The ESD441 is offered in the industry standard 0201 and 0402 package.



Figure 2-17. Functional Block Diagram

2.2.15 TPD2E2U06

The TPD2E2U06 is a dual-channel low capacitance TVS diode ESD protection device. The device offers $\pm 25\text{kV}$ contact and $\pm 30\text{kV}$ air-gap ESD protection in accordance with the IEC 61000-4-2 standard. The 1.5pF line capacitance of the TPD2E2U06 makes the device an excellent choice for a range of applications.

Typical application interfaces are USB 2.0, LVDS, and I2C.

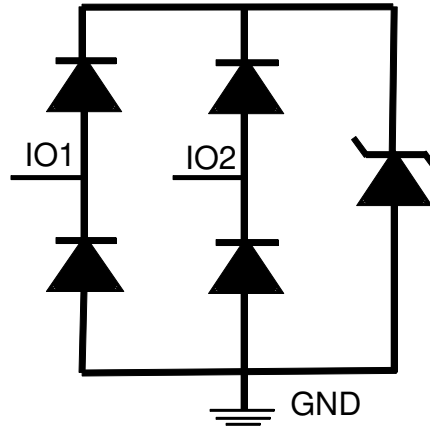


Figure 2-18. Functional Block Diagram

2.2.16 TPS7A3701

The TPS7A37 belongs to a family of LDO regulators that use an NMOS pass transistor to achieve ultra-low dropout performance and reverse current protection. These features combined with an enable input make the TPS7A37 an excellent choice for portable applications. This regulator family offers a wide selection of fixed output voltage versions and an adjustable output version. All versions have thermal and over-current protection, including foldback current limit.

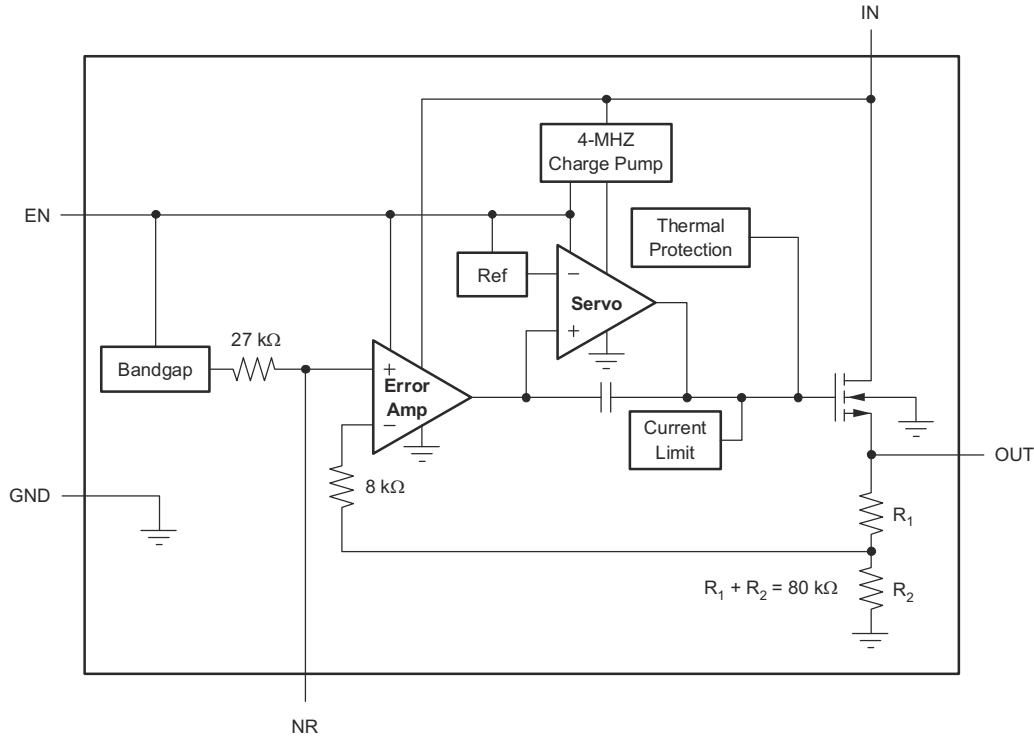


Figure 2-19. Fixed Voltage Version

2.2.17 MSP432E401

The SimpleLink™ MSP432E401Y Arm Cortex-M4 microcontroller (MCU) provides top performance and advanced integration. The MSP432E4 product family is positioned for cost-effective applications requiring significant control processing and connectivity capabilities such as the following:

- Industrial communication equipment
- Network appliances, gateways, and adapters
- Residential and commercial site monitoring and control
- Remote connectivity and monitoring
- Security and access systems
- HMI control panels
- Factory automation control
- Test and measurement equipment
- Fire and security systems
- Motion control and power inversion
- Medical instrumentation
- Gaming equipment
- Electronic point-of-sale (POS) displays
- Smart energy and smart grid equipment
- Intelligent lighting control
- Vehicle tracking

The MSP432E401Y MCU integrates many communication features in a new class of highly connected designs that can support critical, real-time control with a balance between performance and power. The MCU features integrated communication peripherals and other high-performance analog and digital functions to offer a strong foundation for many different target uses, from human-machine interface to networked system management controllers.

The MSP432E401Y MCU offers access to development tools from Arm, system-on-chip (SoC) infrastructure, and a large user community. Additionally, this MCU uses the Thumb-compatible Thumb-2 instruction set from Arm to reduce memory requirements and cost.

Finally, when using the SimpleLink SDK, the MSP432E401Y MCU is code-compatible with all members of the SimpleLink series, providing flexibility to fit precise needs.

TI offers the following tools to help get to market quickly:

- Evaluation and development boards
- Support documentation like white papers and application notes
- An easy-to-use peripheral driver library
- A strong support, sales, and distributor network

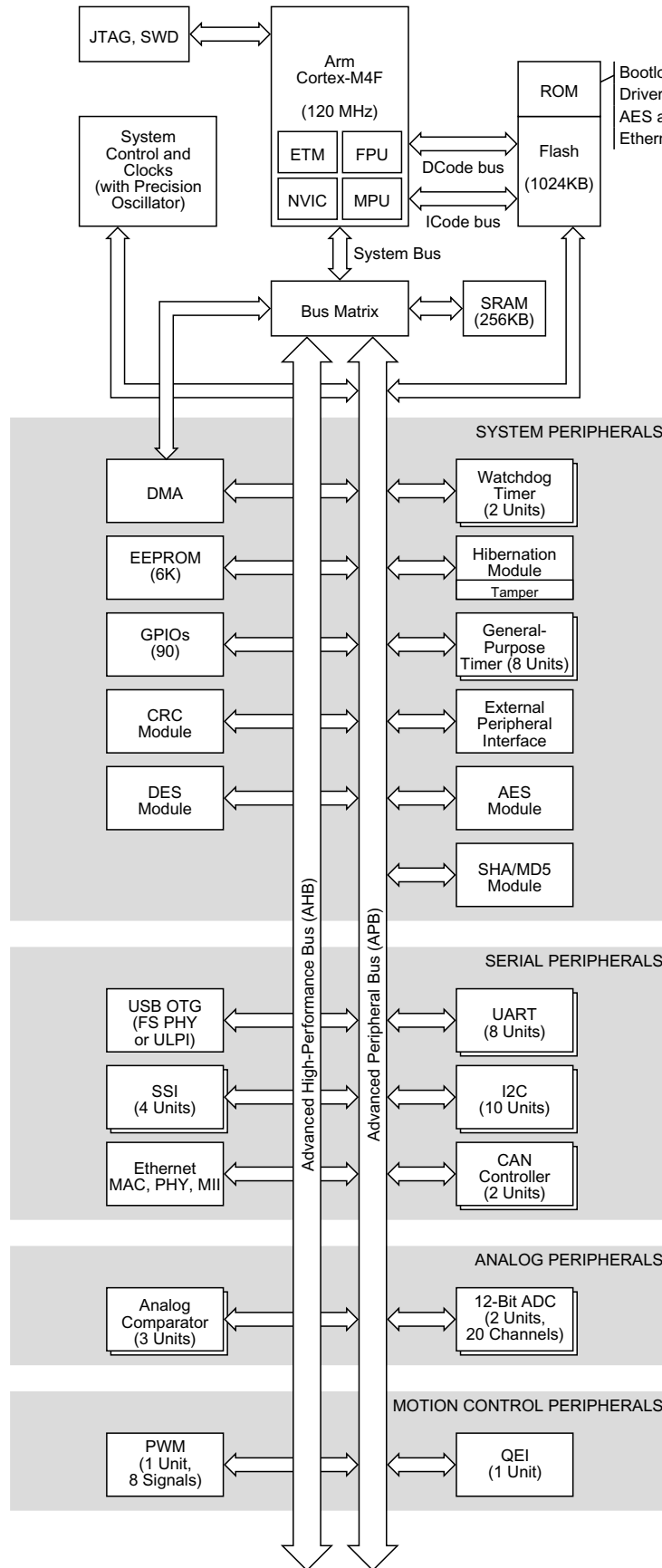


Figure 2-20. High-Level Block Diagram

2.2.18 CSD18540Q5B

This 1.8mΩ, 60V NexFET™ power MOSFET is designed to minimize losses in power conversion applications with a SON 5mm × 6mm package.

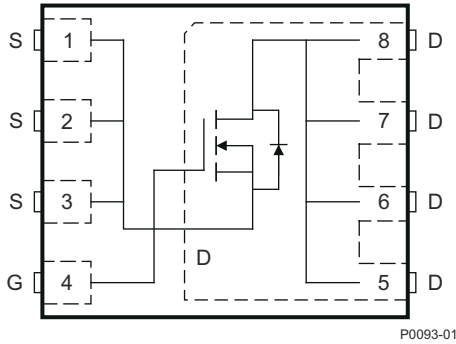


Figure 2-21. Top View

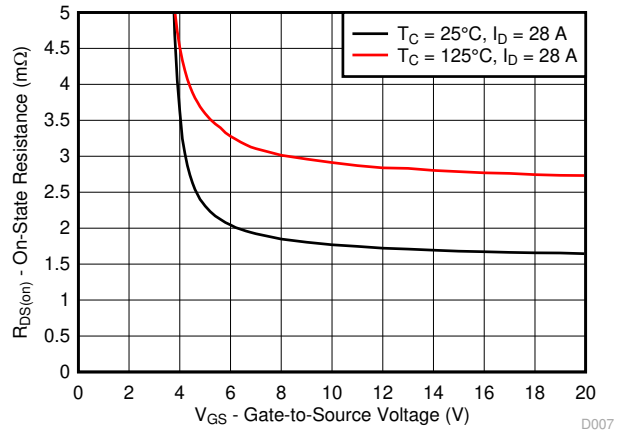


Figure 2-22. RDS(on) vs VGS

2.2.19 CSD18543Q3A

This 60V, 8.1mΩ, SON 3.3mm × 3.3mm NexFET™ power MOSFET is designed to minimize losses in power conversion applications.

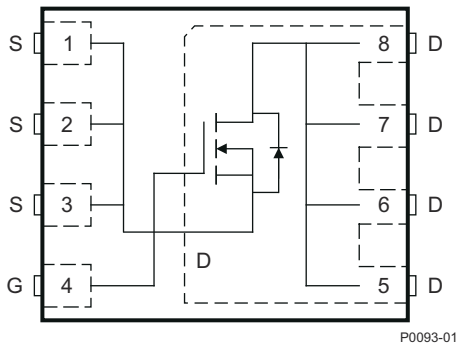


Figure 2-23. Top View

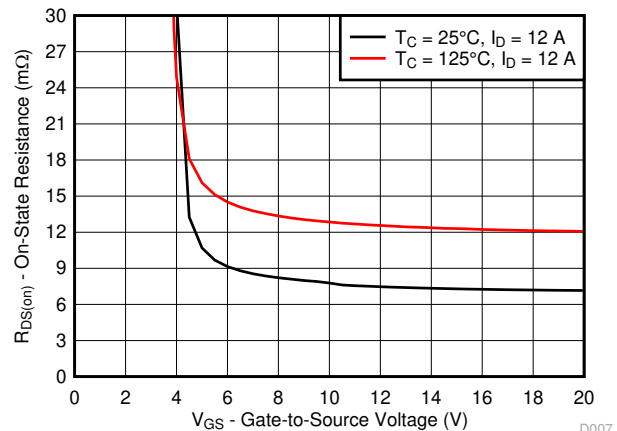


Figure 2-24. RDS(on) vs VGS

3 System Design Theory

This section describes the hardware architecture and the key implementations of the reference design including component selections, layout hints and EMC guidelines.

3.1 Power Supply and Protection

For design simplicity and cost-efficiency, this design does not use a PMIC and uses a minimal number of power rails. All parts operate either directly on the input voltage (IO-Link transceiver, high side switches) or on a 3.3V rail (Ethernet PHYs, Flash, RAM, shift registers, clocking). The CPU core requires 1.25V and needs a separate regulator. The 1.8V needed for the CPU are generated internally by the CPU from the 3.3V and does not require an additional DC/DC or LDO.

This simplifies the power tree to the block diagram shown below. With not using a PMIC, the user also needs to take care of the power sequence and releasing the CPU from reset when the power is stable. Figure 3-1 shows the designed power sequence as well.

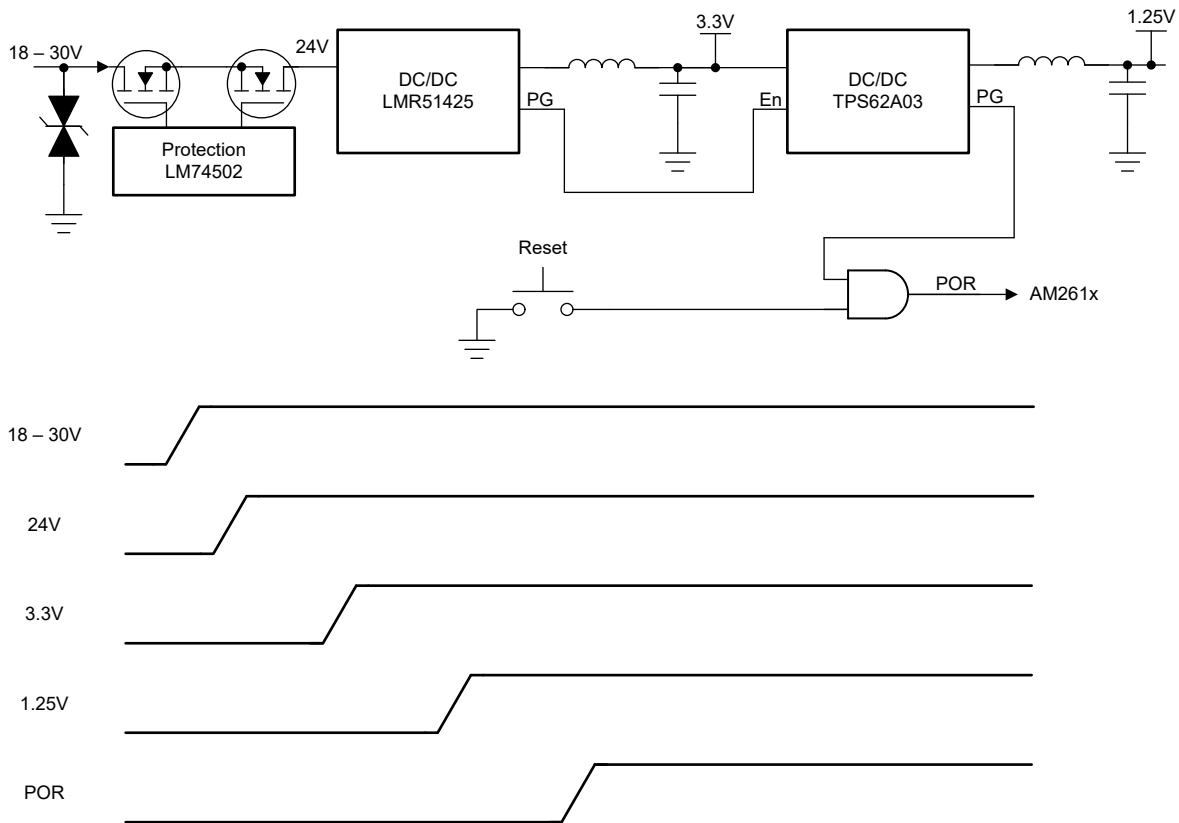


Figure 3-1. Power Tree and Reset Generation

3.1.1 LM74502 Input Protection

The LM74502 drives two FETs, that have to pass the complete current, with 8 ports allowing an L+ current of 1A each, this adds up to more than 8A. CSD18540Q5B is designed in for this and CSD18531Q5A is tested as well as an lower current option.

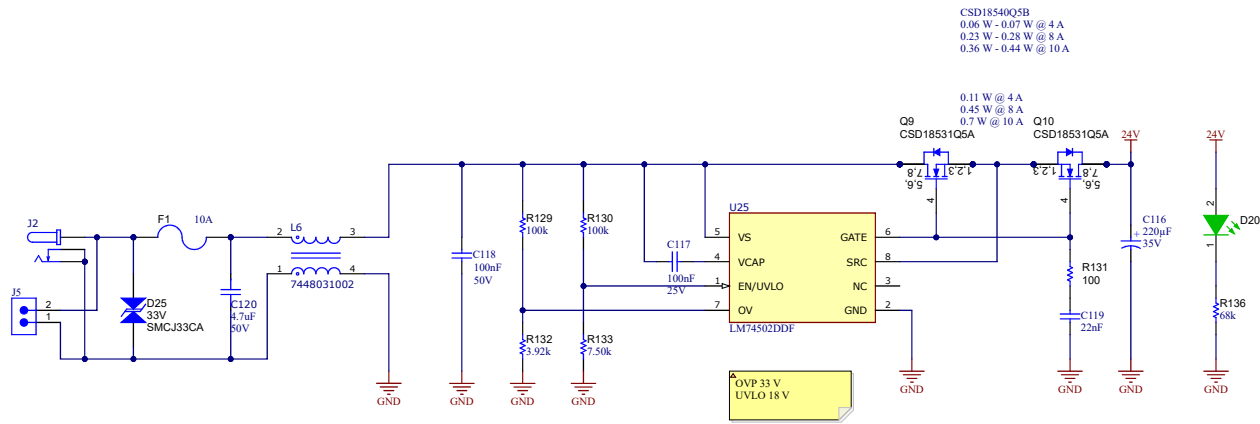


Figure 3-2. Input Protection with LM74502

The LM74502 is programmed to turn the system on when the voltage is at least 18V and to turn off if the voltage increases above 33V. When voltages are above 33V, such as during a surge event or significant over voltage, a TVS diode clamps to a safe level to prevent damage to the LM74502 and the FETs.

To make a smooth start-up, the slew rate on the gate of the FETs is limited. The FETs operate in the linear region for a certain time when the slew rate is limited. Make sure to operate the FET within the SOA. However, there is no significant current drawn when the system starts up. At start-up only the capacitors need to be charged, the remaining system is in the range of 100mA at the beginning. The high current operation starts after the CPU initializes the high side switches and turns the output on. The user controls this operation and can delay the operation until after the FETs have fully turned on.

The common mode filter inductor is selected to have a good attenuation of the first DC/DC's switching frequency. The first DC/DC is operating in FPWM mode with 500kHz, and the common mode inductor has a specified attenuation of 26dB. Also the common mode filter needs to be able to handle the maximum current. With a maximum current rated at 10A, the selected inductor is fine for the application.

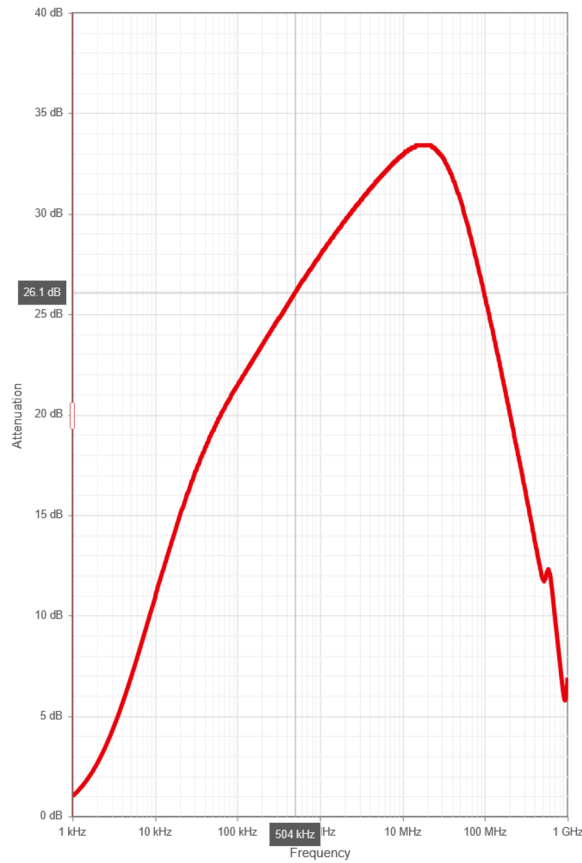


Figure 3-3. Attenuation of CMC Filter 7448031002

By having a capacitor also on the input side of the common mode filter, the differential leakage inductance help to build a differential mode filter. [Figure 4-46](#) and [Figure 4-47](#) shows that filtering meets the requirements.

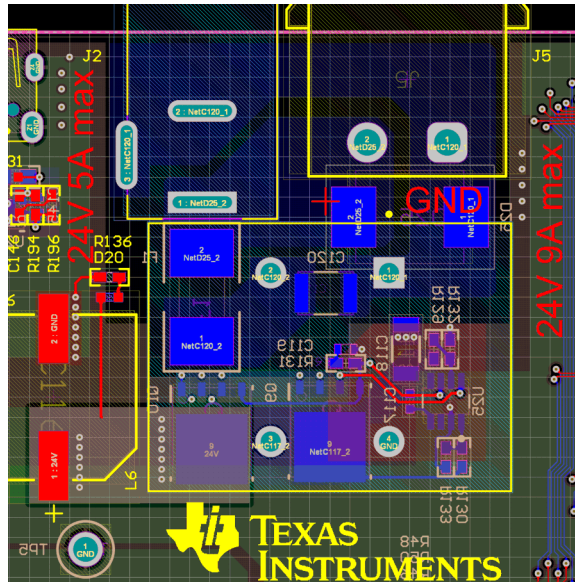


Figure 3-4. Layout of the Input Protection

[Figure 3-4](#) shows the layout of the LM74502 and input filter part. There are two parallel power connectors for ease of use. One of these connectors is a barrel jack, as there are many wall plug adapters available. No special

power supply is needed, so using the connectors during development is easy. The barrel jack is limited to 5A, so a second connector that can handle more current is placed. Both connectors can be used during testing.

The planes of the PCB cross half of the inductor and no planes overlapping the inductor when going to the connector-side of the common mode inductor. This design minimizes any parasitic capacitance between the internal planes and the DC connector to prevent HF noise on the GND or other planes from bypassing the filter.

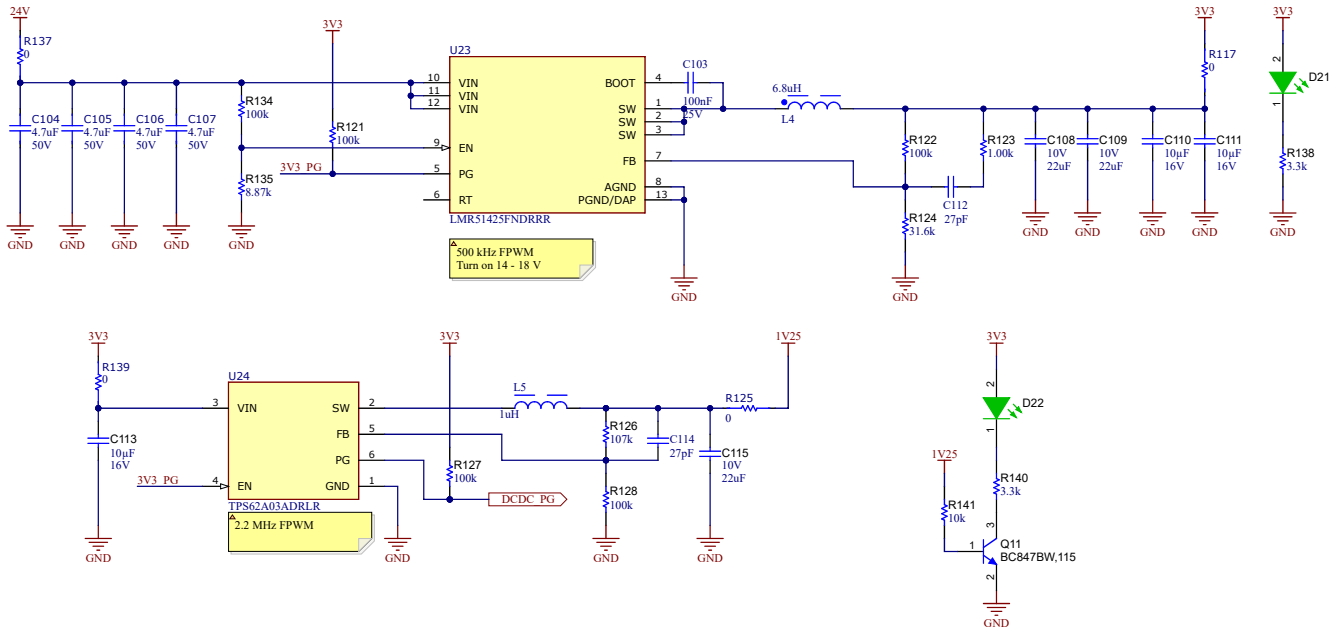


Figure 3-5. Power Supply with LMR51425 and TPS62A03

The schematic shows both DC/DC regulators. LMR51425 in a variant running at 500kHz in FPWM mode is used to step 24V down to 3.3V directly. The design includes a feed forward network in the feedback path to make the current step response a bit faster.

The capacitors selected are size 1206 and 1210. This design uses multiple capacitors so that the derated capacitance meets the designed capacitance. Because the power good signal (open drain) is used for power sequencing and enables the 1.25V converter TPS62A03, the design needs a pull up resistor to work as intended.

Input and outputs are connected to the system through 0Ω resistors to disconnect so that the DC/DC can be disconnected from the system and tested separately and also to have a footprint available if additional filter with a ferrite bead is needed.

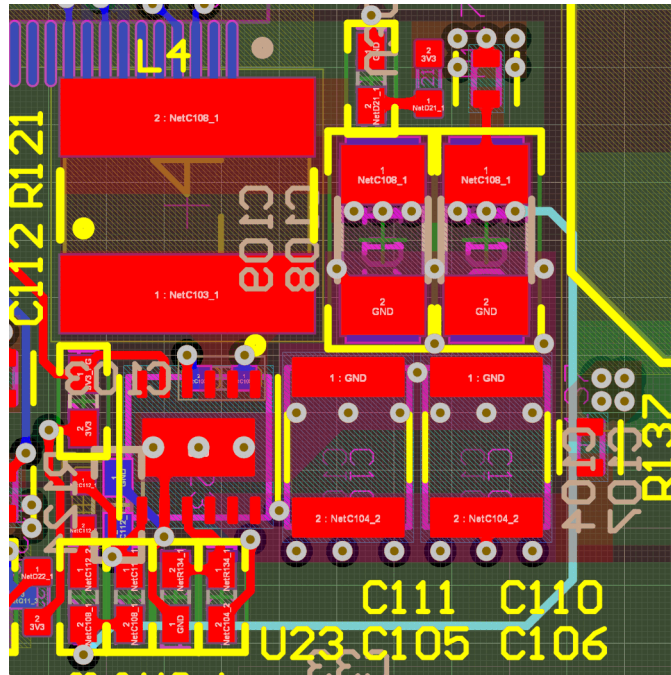


Figure 3-6. LMR51425 Layout

Figure 3-6 shows the layout of the LMR51425 DC/DC regulator. The capacitors on input and output are placed next to each other, and close to the input pins of the DC/DC and the output side of the inductor. The size of the capacitors and the inductor helps keep the current loop very small. There are capacitors on both side of the PCB which are connected to each other with numerous vias. The planes are drawn and connected in a way that the current on input and output side has to pass by the capacitors. The inductor has a start of winding on the IC side, so the noisy part is minimal and the winding helps shielding the switching noise. These functions reduce radiated EMI from the DC/DC.

The TPS62A03 supplies the CPU core and therefore has to meet tight load step tolerances. The 1.25V rail can accept 1.188V to 1.32V and can have a peak current of 1.5A. The TPS62A03 variant selected here is operating in FPWM mode as FPWM mode is behaving better for load transients. The filtering capacitors at the DC/DC and especially at the CPU helps to stay within the limits. Pre-test with this device has shown the power rail to stay within the given limits.

The TPS62A03 gets enabled when the 3.3V rail is stable and the power good is released. The power good of the TPS62A03 releases the CPU from reset.

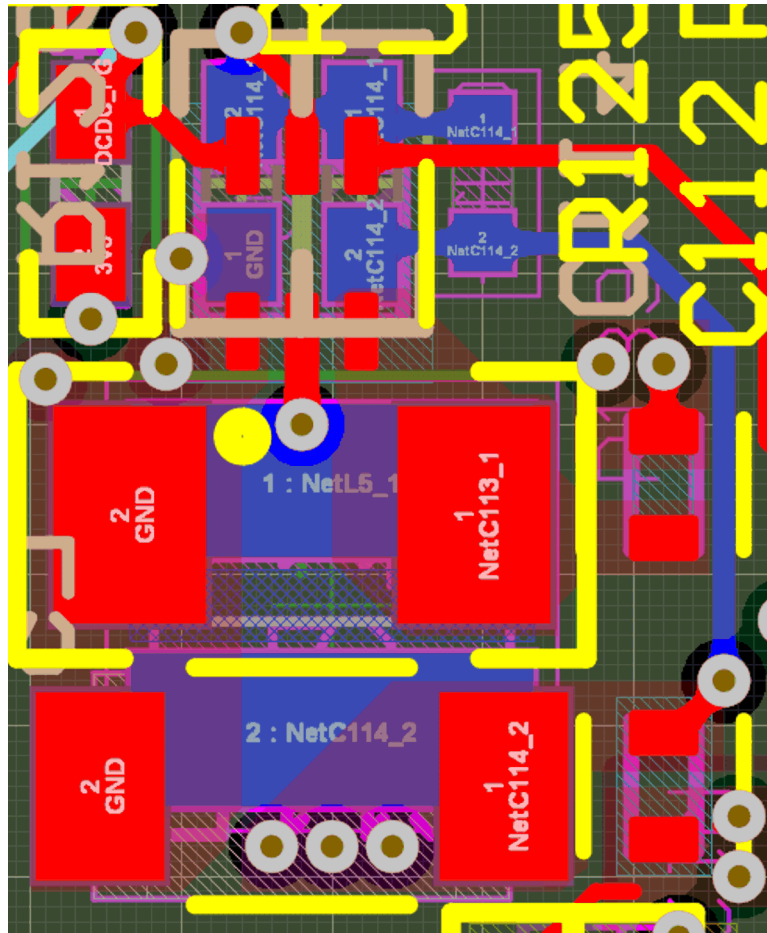


Figure 3-7. TPS62A03 Layout

The layout follows the same rules as any switching regulator. In this design, the inductor is placed on the bottom side and the capacitors are on top so that the size of the current loop is small.

3.2 Ethernet

Two DP83826A PHYs are used to implement Industrial Ethernet. To have more flexibility in configuration, the devices are configured to enhanced mode. The PHYs are configured to have fast link drop enabled and use MII mode. Check that both PHYs have different addresses on the MDIO bus.

A few key mechanisms make the circuit more robust. [Figure 3-8](#) shows the Media-dependent interface MDI connection from the PHY to the network cable. Because this connection leaves the board, the connection must be protected so the PHY cannot be damaged or interfered from the outside. Also, the connection does not bring out noise from the board.

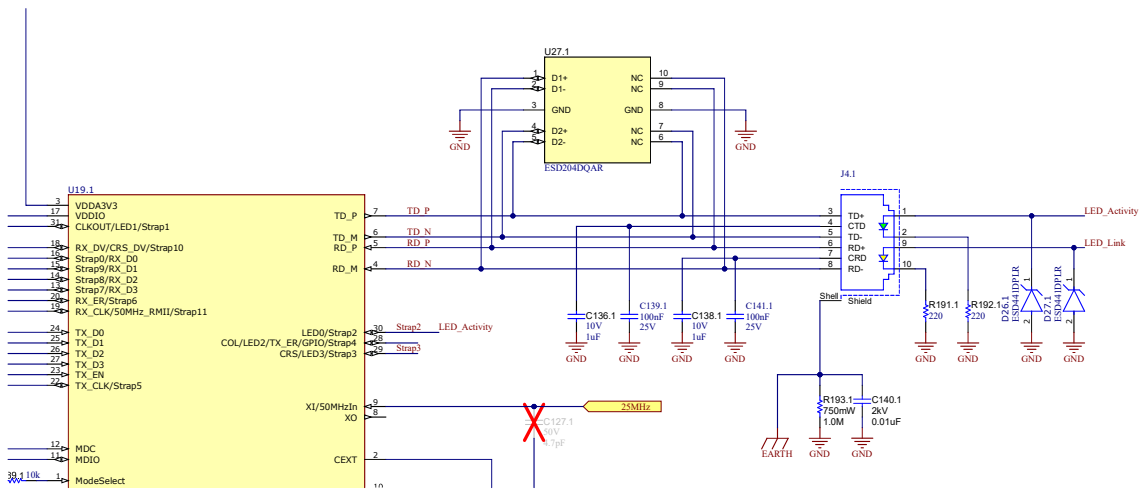


Figure 3-8. Ethernet MDI Protection

The connector J4 includes an Ethernet transformer and common mode choke on both sides of the transformer, so the connector improves the signal integrity of the Ethernet signal. Also the J4 connector includes the termination on the cable side.

The transformer also provides some protection against common mode signals from the outside, such as burst and ESD by having an isolation between primary and secondary side. But the transformer has a parasitic capacitance, allowing these pulses to travel to the PHY because the bandwidth of these signals is very high. The burst is approximately 100MHz and ESD is approximately 1GHz. To clamp the noise, an ESD diode U27.1 is used. The pinout of this ESD diode allows the routing of the Ethernet signals through without any stubs or additional vias. Figure 3-9 shows the routing.

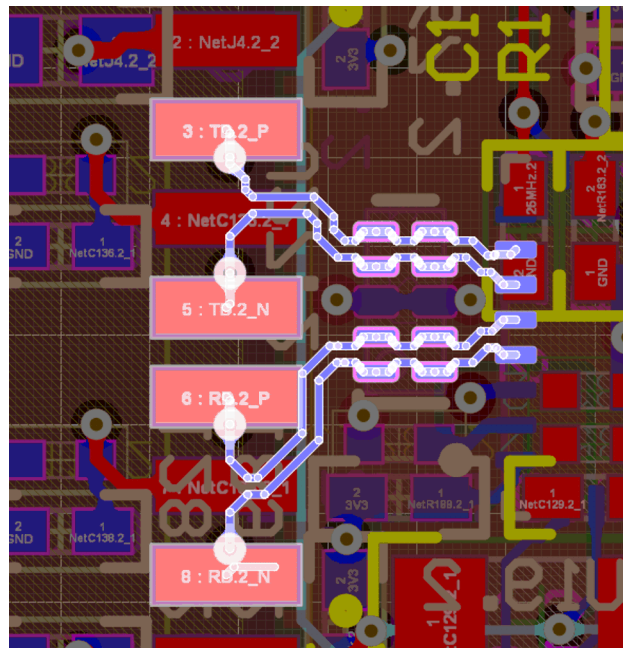


Figure 3-9. ESD Diode Placement and MDI Routing

As an ESD pulse can also get inside the board through the LEDs next to the connector, the LED lines are also clamped with ESD diodes, D26.1 and D27.1 so the PHY does not get damaged or issues a reset.

C140.1 and R192.1 are important for an HF connection between the system GND and the cable shield. The capacitor shorts the isolation barrier for high frequency noise and can charge up over time. R192.1 is important to discharge the capacitor. Figure 3-10 shows that the capacitor size. A large capacitor that can provide a very

low impedance short at high frequencies is recommended. Avoid long and thin traces. To connect an internal layer, use multiple vias. The placement of the resistor is not critical. The resistor and trace spacing can manage the high voltages that can occur during EFT bursts.

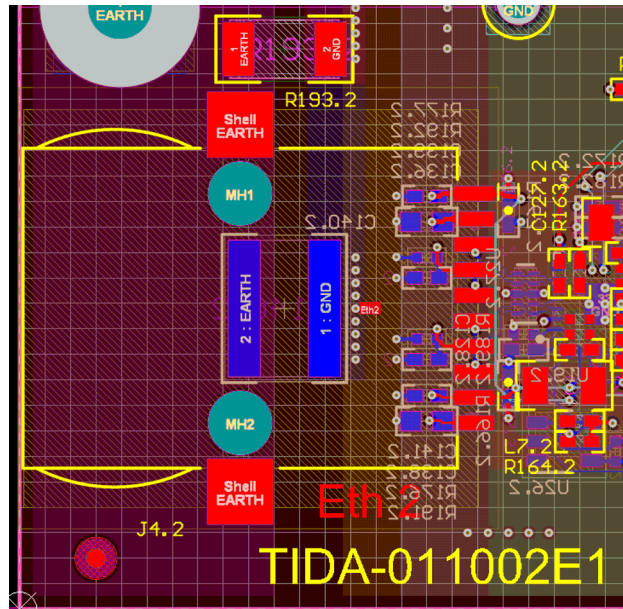


Figure 3-10. Ethernet EMI Capacitor Placement

Figure 3-8 shows how an optional small capacitor is used to load the clock line and reduce slew rate if needed. In this case, tests have shown the capacitor is not needed.

Figure 3-11 shows the option to have small capacitors on the reset line of the Ethernet PHYs. Assemble these capacitors as needed to increase ESD robustness. A ESD pulse in a plane below the board couples into all traces and can disturb the signals. Long traces with weak driver, such a small capacitor, can help to keep the level stable and prevent a reset. Place the capacitor close to the input of the device.

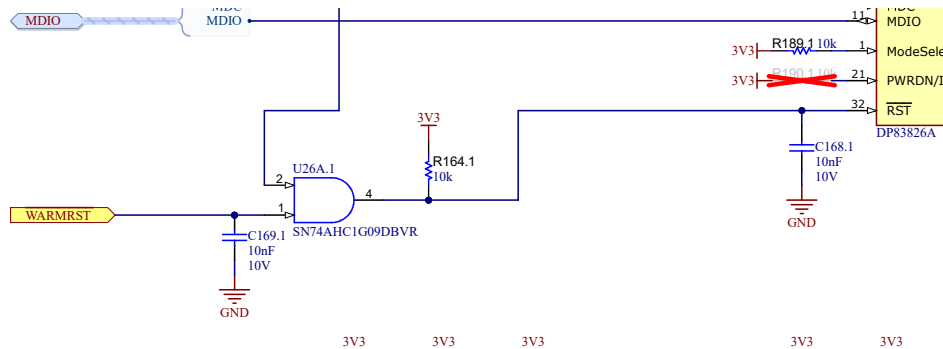


Figure 3-11. Capacitors on Reset increase ESD Robustness

For filtering the power supply of the Ethernet PHY, see Figure 3-12. Consider having a set of capacitors with different sizes and a ferrite bead. Depending on the impedance over frequency of the capacitors, a single capacitor is sufficient.

Note

The ferrite beads can be tested during EMC tests if necessary, but ferrite beads reduce the noise coming from the PHY going into the power tree of the system.

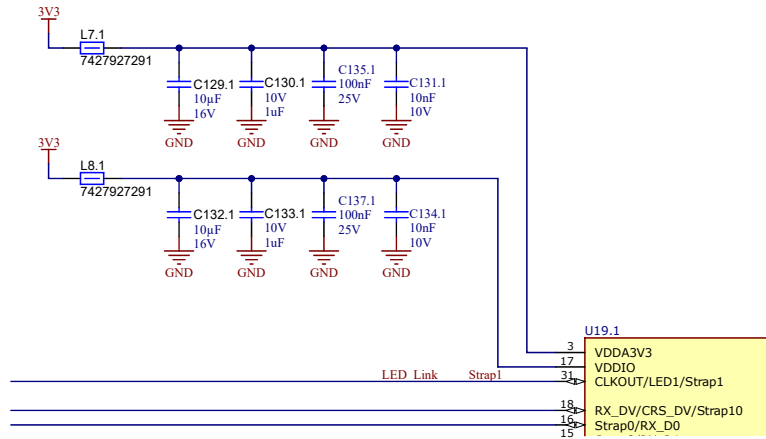


Figure 3-12. Filtering on Power Supply of Ethernet PHY

Route the power supply traces through the capacitors so that all the current must bypass the capacitors. This routing keeps parasitics as small as possible.

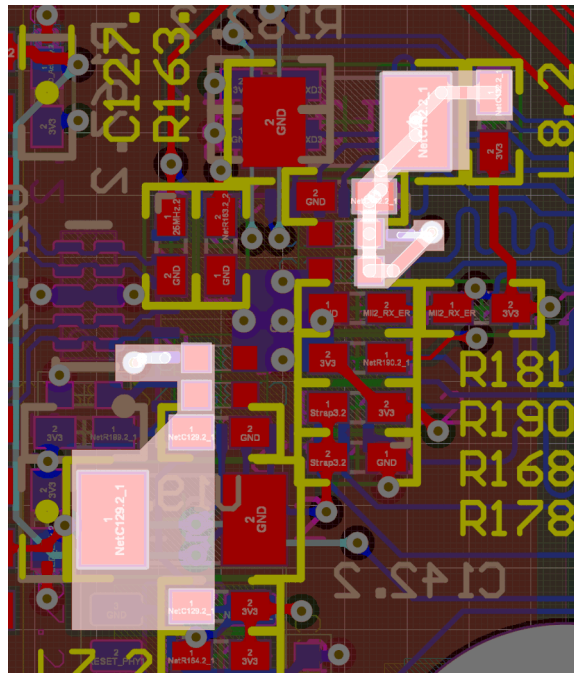


Figure 3-13. Routing Powerlines through Capacitors

3.3 IO-Link HSS

To control the L+ lines of the connected IO-Link devices, two TPS274C65 are used. The high side switches are configured to operate in addressed SPI, so both devices can be accessed with one CS, only the address send through SPI is different.

Figure 3-14 shows how the device is connected, both devices are connected the same way, only resistors R38 and R131 are different to set the different addresses. The high side switches offers the option to have a reverse current blocking through an external FET. Here are CSD18543Q3A used for this function. If this is not needed, the FETs can be removed and shorted.

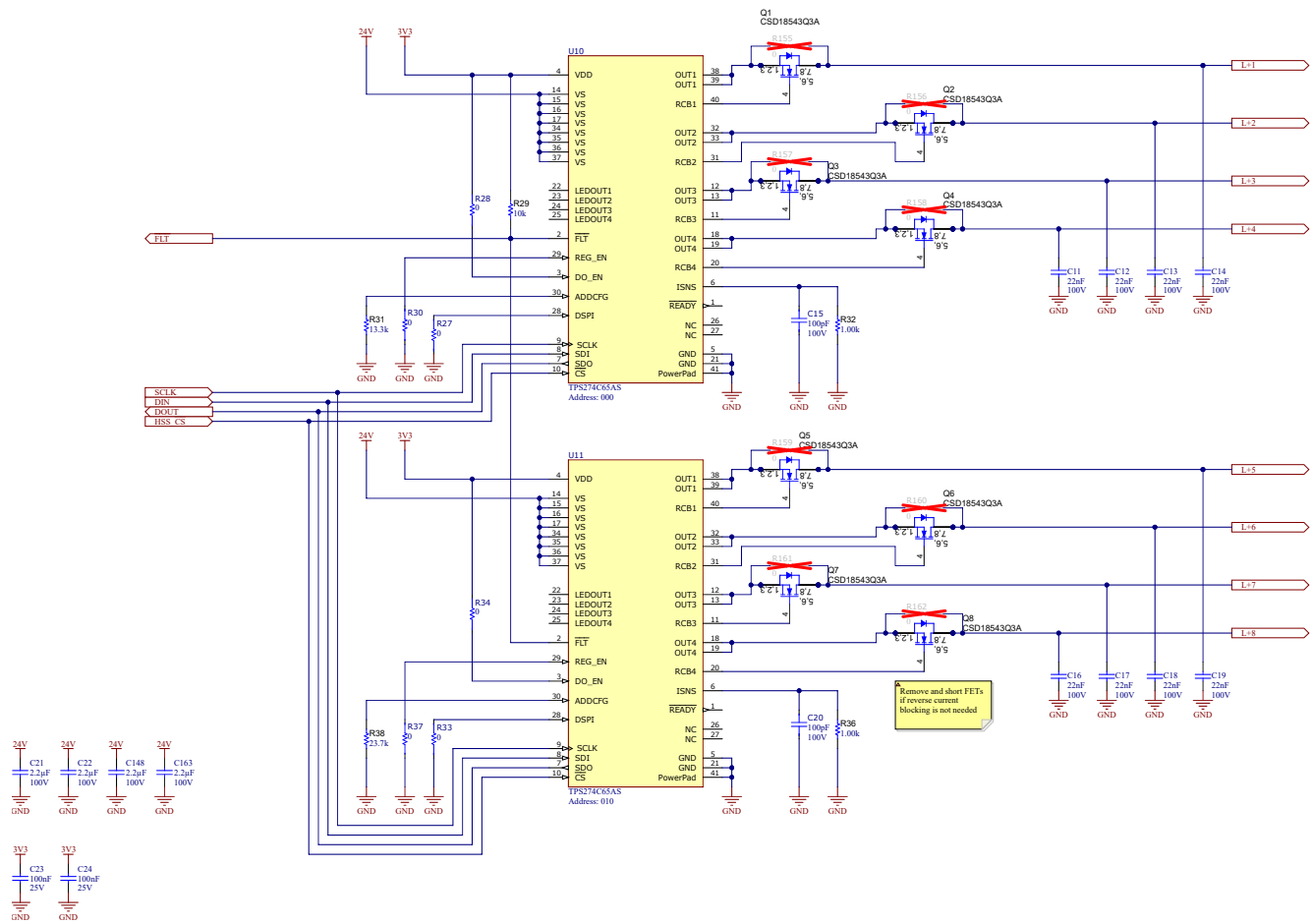


Figure 3-14. High Side Switches

3.4 Shift Registers for LEDs and Digital IO

To save GPIOs on the processor, the digital IOs and the LEDs of the IO-Link ports are controlled through a shift register chain. Although the digital IOs can be read and set through the SPI of the TIOL221, doing so requires more software overhead than using one SPI transfer because every TIOL221 SPI has separate chip select pins.

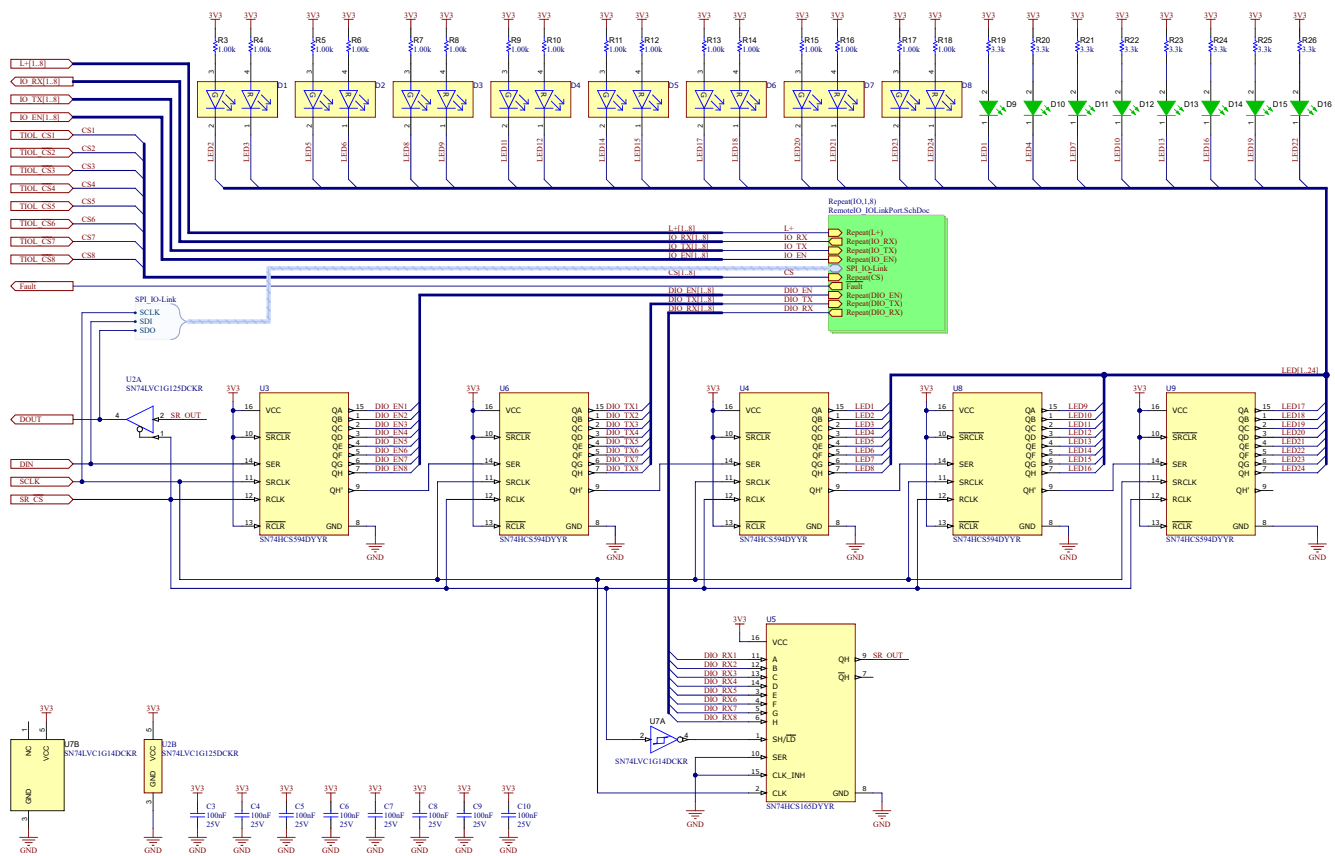


Figure 3-15. Shift Registers are Used for Controlling All LEDs and DIO

Figure 3-15 shows the shift register chain. Five SN74HCS594 are connected to build a 40 bit register for 24 LEDs, the digital IO Enable signal and the DIO output signal. To read back the level of the DIO line, the RX signal of all TIOL221 is connected to a SN74HCS165 shift register. The level of the DIO inputs is latched when the CS goes low (U7 is needed to have the correct logic) and remains stable during the SPI transfer. Because this SPI shares the DIN and DOUT signals with other SPI peripherals on the board, the DOUT has to be in a tri-state condition this is achieved by using U2 when CS is high.

3.5 Protection of IO-Link

The IO-Link port does not need much protection, but a small capacitor of 1nF to GND on the CQ and DI/DO line helps to improve noise sensitivity. To protect the port against surge, use additional diodes as needed. In this design, a combination of TVS3300 and TSM36 are used and tested. Footprints are also available to add MOVs.

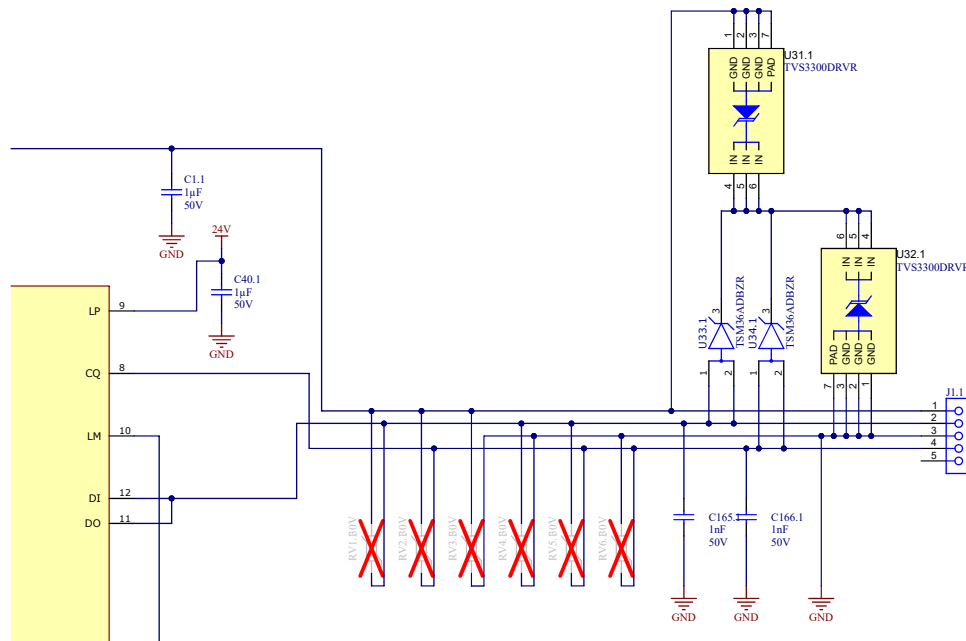


Figure 3-16. Diodes and Capacitors at the IO-Link Port for Protection

3.6 CPU and Boot

For booting the processor, the SOP pins need to be set correctly depending on where to boot from. The switch SW1 is connected at reset through U15 and provides the relevant configuration to the processor.

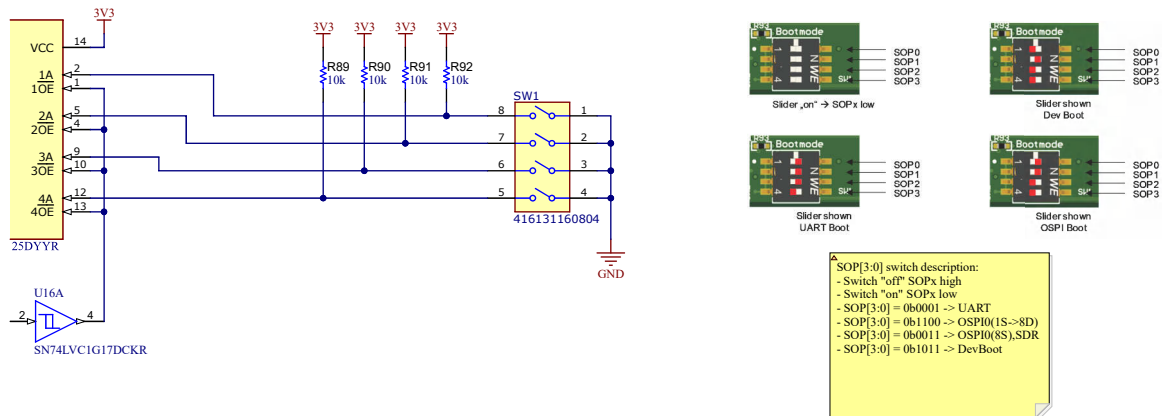


Figure 3-17. Boot Mode Switches

Boot Device	SW1 (1 = on, 0 = off)
UART	1110
Dev Boot	0100
OSPI	1100

Because the reference design uses a larger flash than the AM261 EVM and all the software examples, the bootloader related files from SDK need to be modified so the `ti_board_open_close.c` file generated by `syscfg` looks as shown below. This configuration allows booting in high speed OSPI mode with up to 133MHz.

```

/* FLASH Attrs */
Flash_Attrs gFlashAttrs_MX25LM51245GXDI00 =
{

```

```

        .flashName = "MX25LM51245GXDI00",
        .deviceId = 0x853A,
        .manufacturerId = 0xC2,
        .flashSize = 67108864,
        .blockCount = 1024,
        .blockSize = 65536,
        .pageCount = 256,
        .pageSize = 256,
        .sectorCount = 16384,
        .sectorSize = 4096,
        .phyTuningOffset = 0x80000,
};

/* FLASH DevConfig */
Flash_DevConfig gFlashDevCfg_MX25LM51245GXDI00 =
{
    .cmdExtType = OSPI_CMD_EXT_TYPE_INVERSE,
    .enable4BAddr = TRUE,
    .addrByteSupport = 2,
    .fourByteAddrEnSeq = 0x20,
    .cmdWren = 0x06,
    .cmdRdsr = 0x05,
    .srwip = (1 << 0),
    .srwel = (1 << 1),
    .xspiwipRdCmd = 0x05,
    .xspiwipReg = 0x00000000,
    .xspiwipBit = (1 << 0),
    .resetType = 0x10,
    .eraseCfg = {
        .blockSize = 65536,
        .sectorSize = 4096,
        .cmdBlockErase3B = 0xD8,
        .cmdBlockErase4B = 0xDC,
        .cmdSectorErase3B = 0x20,
        .cmdSectorErase4B = 0x21,
        .cmdChipErase = 0xC7,
    },
    .idCfg = {
        .cmd = 0x9F, /* Constant */
        .numBytes = 3,
        .dummy4 = 0,
        .dummy8 = 20,
        .addrSize = 0
    },
    .protocolCfg = {
        .protocol = FLASH_CFG_PROTO_8D_8D_8D,
        .isDtr = TRUE,
        .cmdRd = 0xEE,
        .cmdWr = 0x12,
        .modeClksCmd = 0,
        .modeClksRd = 0,
        .dummyClksCmd = 20,
        .dummyClksRd = 20,
        .enableType = 0,
        .enableSeq = 0x04,
        .protoCfg = {
            .isAddrReg = TRUE,
            .cmdRegRd = 0x71,
            .cmdRegWr = 0x72,
            .cfgReg = 0x00000000,
            .shift = 0,
            .mask = 0x00,
            .cfgRegBitP = 0,
        },
        .strDtrCfg = {
            .isAddrReg = TRUE,
            .cmdRegRd = 0x71,
            .cmdRegWr = 0x72,
            .cfgReg = 0x00000000,
            .shift = 1,
            .mask = 0x00,
            .cfgRegBitP = 1,
        },
        .dummyCfg = {
            .isAddrReg = TRUE,
            .cmdRegRd = 0x71,
            .cmdRegWr = 0x72,
            .cfgReg = 0x00000003,
        }
    }
};

```

```
        .shift = 0,  
        .mask = 0x01,  
        .cfgRegBitP = 3,  
    },  
},  
.flashwriteTimeout = 152,  
.flashBusyTimeout = 76000000,  
};
```

The processor includes two ICSS that implement IO-Link and industrial Ethernet. All eight IO-Link ports are handled by one ICSS. The Ethernet interfaces with the second processor. For details about the available stacks for AM261, refer to the [Industrial Communications SDK release notes](#).

4 Hardware, Software, Testing Requirements, and Test Results

4.1 Hardware Requirements

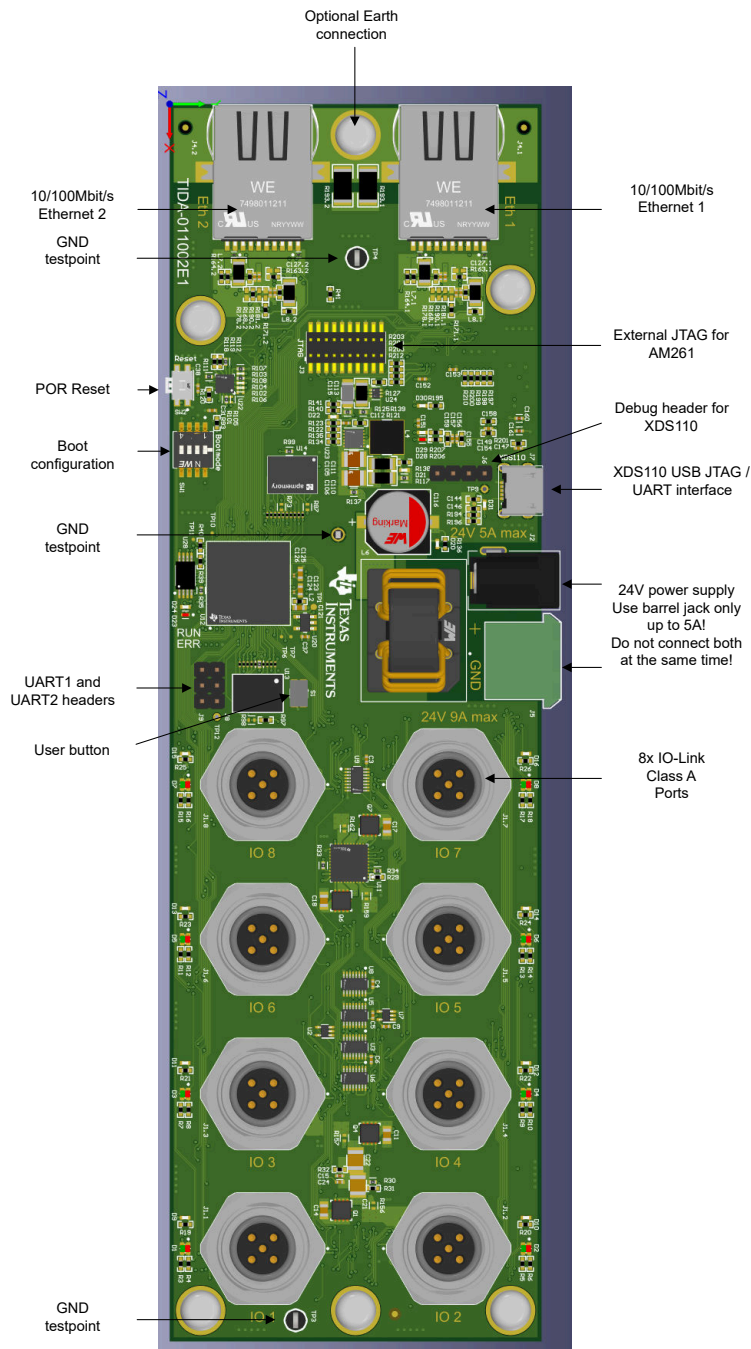


Figure 4-1. Interfaces and Connectors of the Reference Design

Figure 4-1 shows the hardware used for testing the reference design. Software is loaded to the design through USB using the integrated XDS110. This XDS110 allows JTAG access to load and debug the CPU, but also provides access to one of the UARTs. This UART can be used for programming the integrated OSPI flash. When the boot configuration is set to UART boot, the `uart_uniflash.py` (which is part of the `mcu_plus_sdk` for AM261) can be used for programming the flash. Afterwards a program can be started from the OSPI flash without any additional user interaction.

For some tests a IO-Link device is connected to any of the 8 IO-Link ports and a PC is connected to the RJ45 connector to get data from the reference design.

4.2 Software Requirements

The reference design uses the IO-Link Master Demo from the industrial comms SDK, with a slight modification, so the high side switch can be turned on. For some tests additional firmware functions are implemented to read back the ADC values from the high side switch.

4.3 Test Setup

The specific connections and setup for the different tests are described in the test result section.

4.4 Test Results

4.4.1 High Side Switch TPS274C65

The turn on behavior of the high side switch responsible for driving the L+ line of the IO-Link ports is tested with different loads. Here an electronic load set to 1A, an RC parallel connection of 150Ω and 1000μF, a short and a typical IO-Link device (SICK OD1000 distance sensor) is used for testing. All these tests are repeated with 20V and 30V supply voltage. For all tests the high side switch is configured to a current limit of 1A (ILIM_REG = 0x8), the inrush current limit is set to the same level (INRUSH_LIMIT = 0) and the inrush current delay is set to 10ms (ILIM_DURATION = 0x5). The delay should not be visible in the current measurement. Some tests are done with and without auto retry (AUTO_RETRY_DIS).

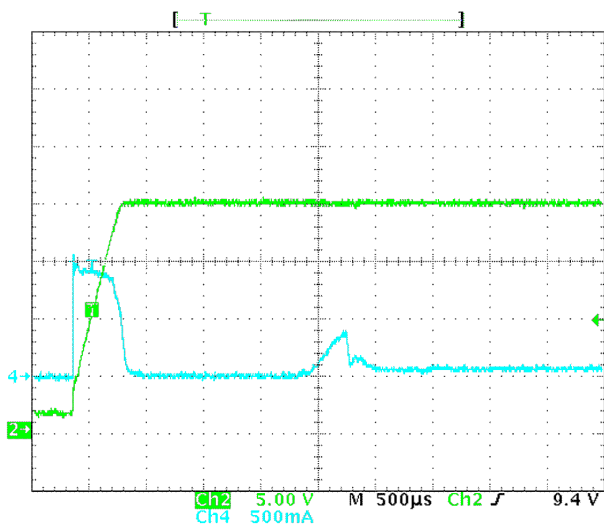


Figure 4-2. Turn on Behavior with Connected SICK OD1000 Sensor at 20V

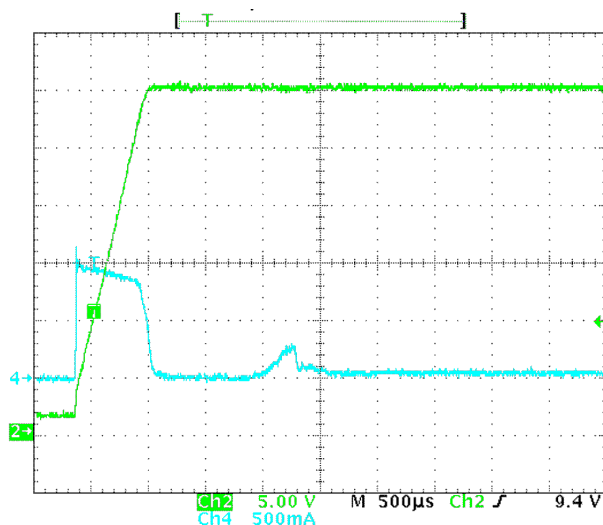


Figure 4-3. Turn on Behavior with Connected SICK OD1000 Sensor at 30V

Figure 4-2 and Figure 4-3 show the startup with connected sensor, for about 500μs the current limit is hit and the voltage rises linearly to 20V respectively 30V. During this time, most likely the sensors internal capacitors are charged and the sensor starts to operate afterward. The TPS274C65 drives the current without any interruptions or restarts.

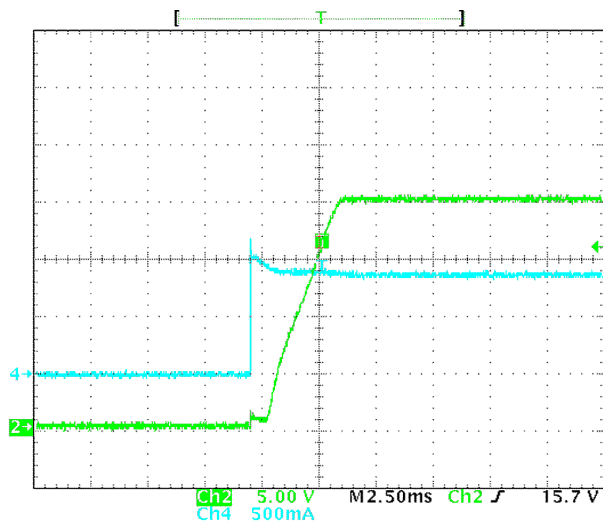


Figure 4-4. Turn on Behavior into Electronic Load at 20V

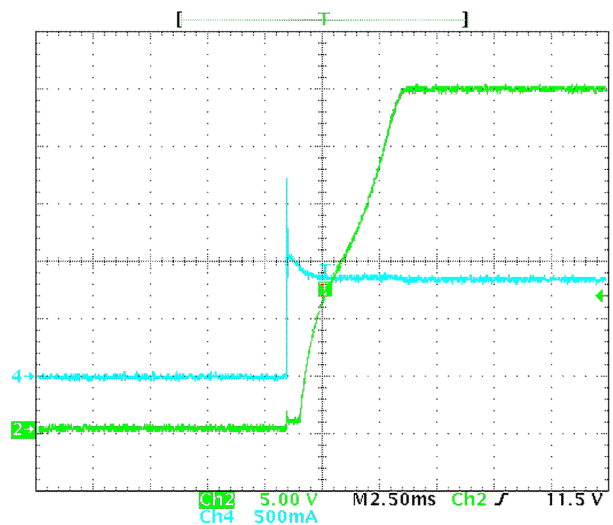


Figure 4-5. Turn on Behavior into Electronic Load at 30V

Figure 4-4 and Figure 4-5 show that the output voltage rises within 2.5 to 4ms to the nominal value when testing with an electronic load. The electronic load kicks in already at a very low voltage and with a fast rise time. The internal capacitance of the electronic load limits the slew rate.

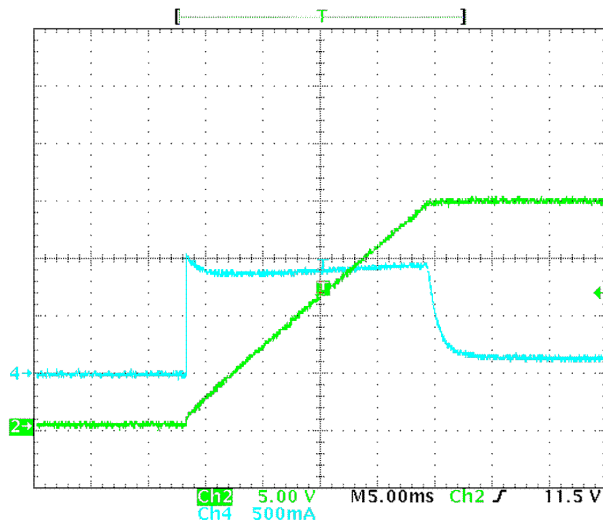


Figure 4-6. Turn on behavior into RC parallel network at 20V

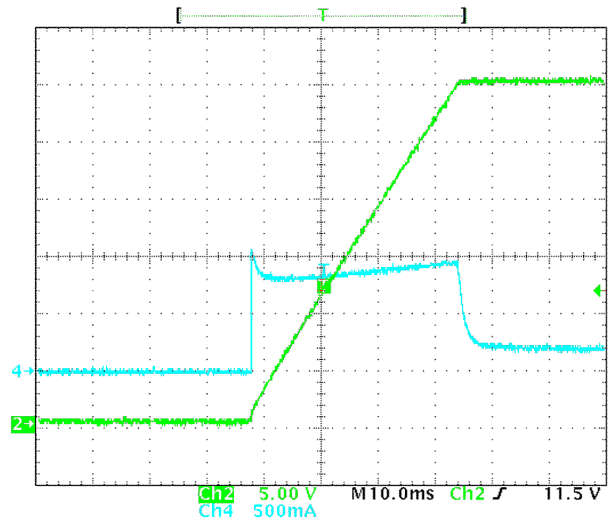


Figure 4-7. Turn on behavior into RC parallel network at 30V

This test explores how the high side switch behaves with a high inrush current and if the device provides at least 20mA of current. A RC network with 1000 μ F and 150 Ω is tested. Figure 4-6 and Figure 4-7 show the results. The high side switch reaches the current limit for about 22ms to 40ms and during this time providing more than 20mA without interrupting the current flow.

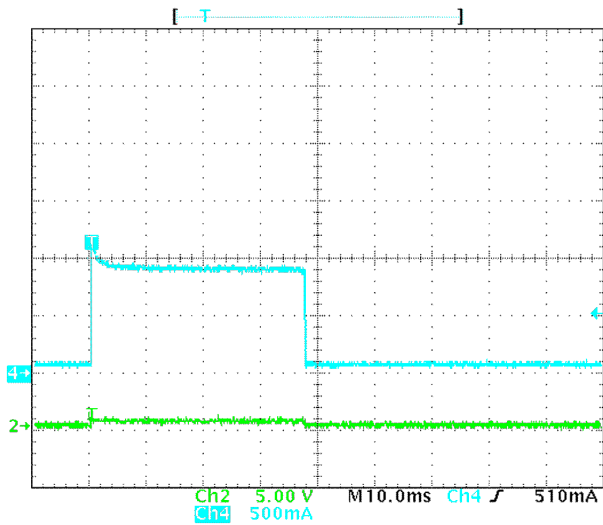


Figure 4-8. Turn on into Short Circuit With Disabled Auto Retry at 20V

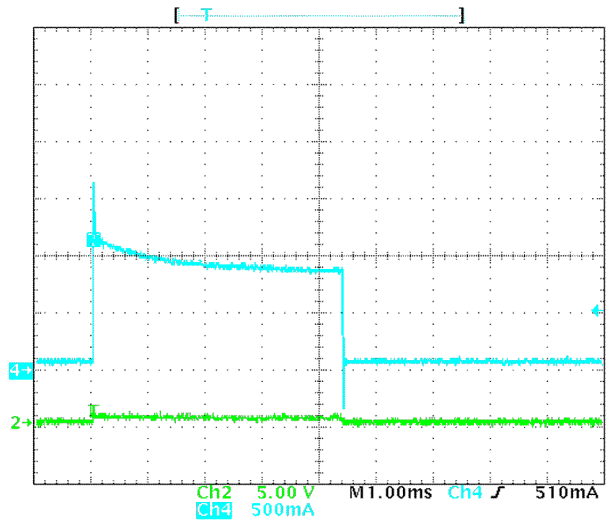


Figure 4-9. Turn on into Short Circuit with Disabled Auto Retry at 30V

Figure 4-8 and Figure 4-9 show how the high side switch behaves when **turning** in on into a short. The switch drives 1A for 37ms at 20V and for 4.4ms at 30V. The output voltage increases slightly because the wiring and the shunt of the multimeter is in series are included in the measurement.

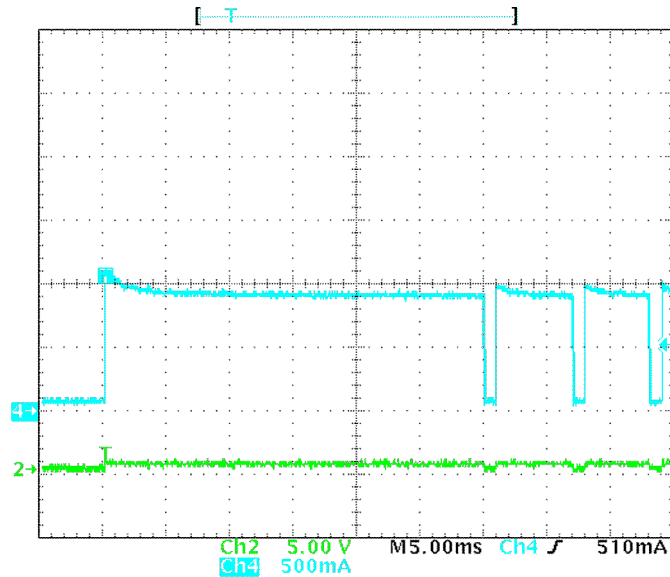


Figure 4-10. Turn on into Short Circuit with Auto-retry at 20V

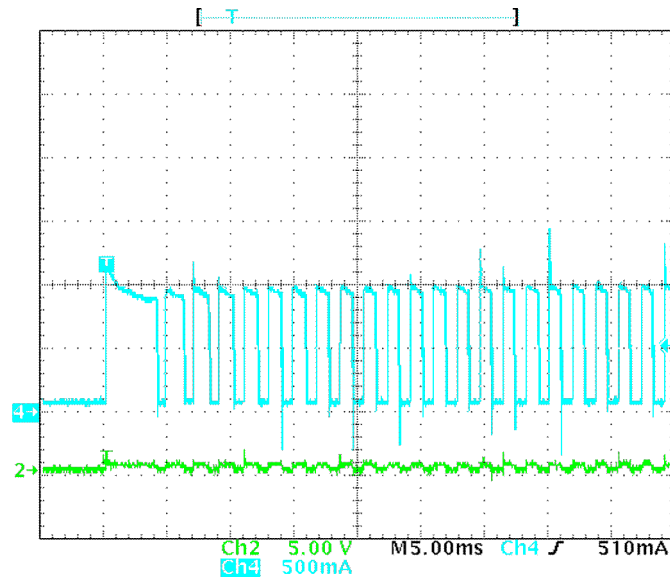


Figure 4-11. Turn on into Short Circuit with Auto-retry at 30V

Figure 4-10 and Figure 4-11 show how the device behaves when auto-retry is enabled and is turned on into a short. As before, the device drives the constant current for a certain time and then starts to toggle between on and off. The off time is in both cases the same because the device needs to cool down. The on time depends on the supply voltage. The device needs to handle a much higher power dissipation when using 30V than with 20V, so the device reaches critical temperature much faster and turns off faster.

The next tests show how the high side switch acts during normal operation, with a current of 1A flowing when a sudden short is applied.

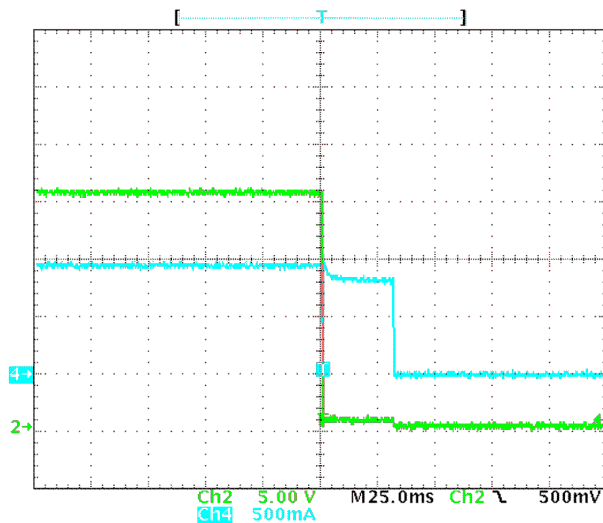


Figure 4-12. Short at 20V, without Auto Retry

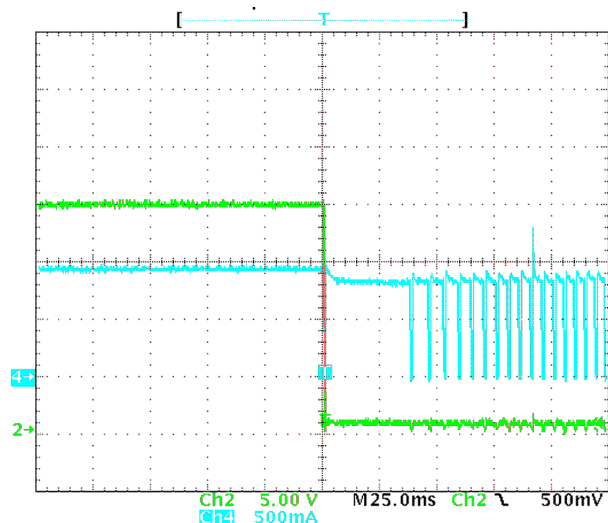


Figure 4-13. Short at 20V, with Auto Retry

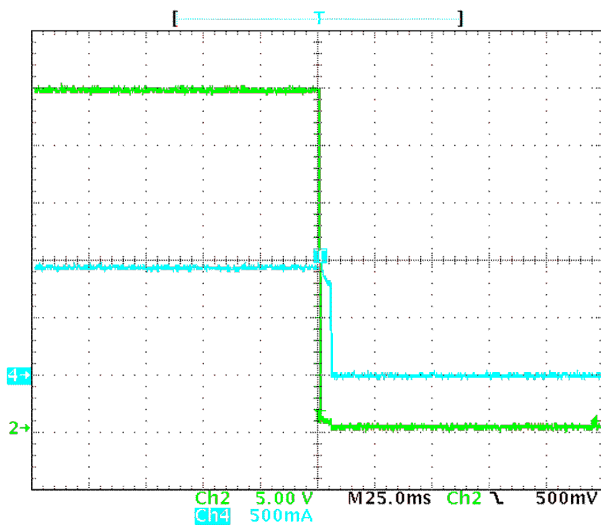


Figure 4-14. Short at 30V, without Auto Retry

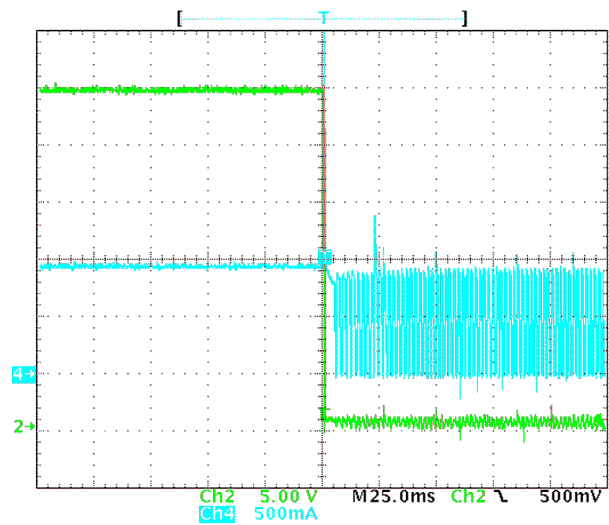


Figure 4-15. Short at 30V, with Auto Retry

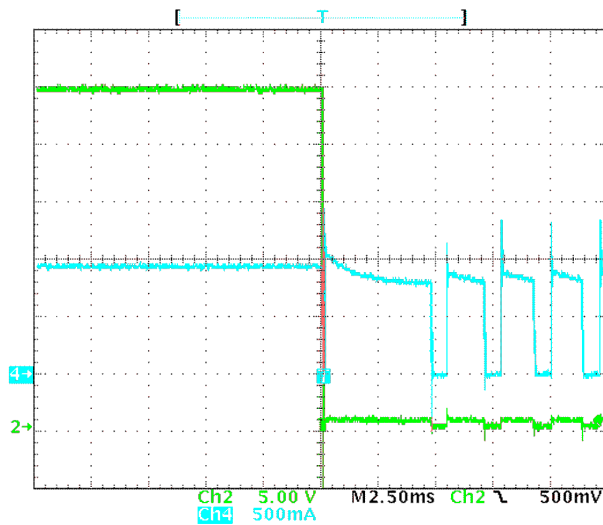


Figure 4-16. Short at 30V, with Auto Retry, Faster Timebase

The high side switch limits the current to about 1A and keeps the current flowing for a certain time until the switch turns off. As expected, the timing of current limit and retry depends on the power supply voltage. Higher the supply voltage leads to higher power dissipation during current limit and shorter time.

Figure 4-17 and Figure 4-18 show the next two tests. These tests are done by applying a short without having an initial current flow. Interestingly, the device switches off almost immediately when the short is applied and takes about 100 μ s until the device is regulating the current to the set level.

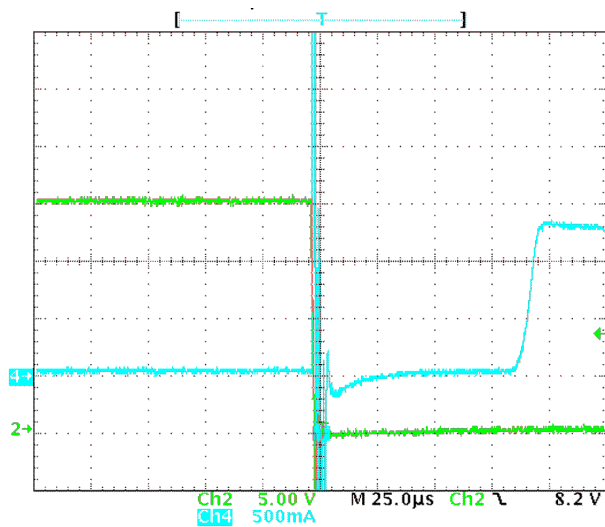


Figure 4-17. Short at 20V

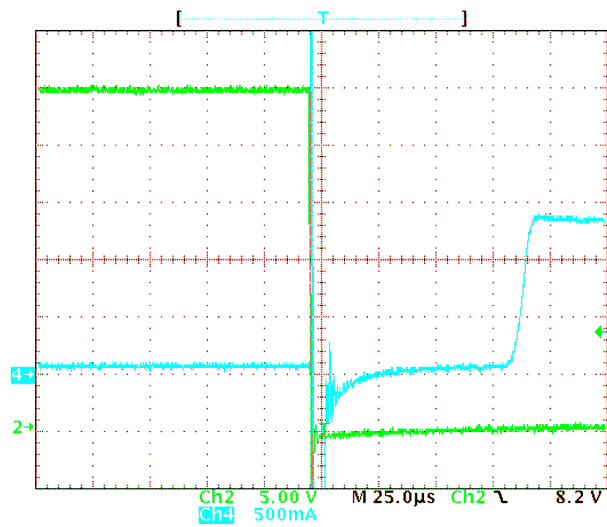


Figure 4-18. Short at 30V

The thermal behavior of the high side switch when all channels are loaded with 1A was also tested. For this test, all four channels were loaded with an electronic load and rest until a thermal stability is reached. In both configurations, the device heats up to approximately 42°C. All tests are conducted at room temperature and without a housing.

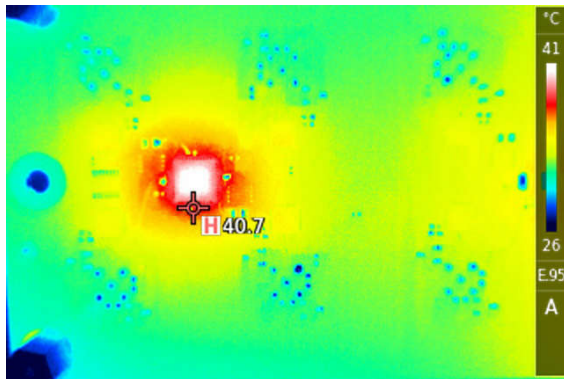


Figure 4-19. Thermal Image at 20V with 4x 1A Output Current

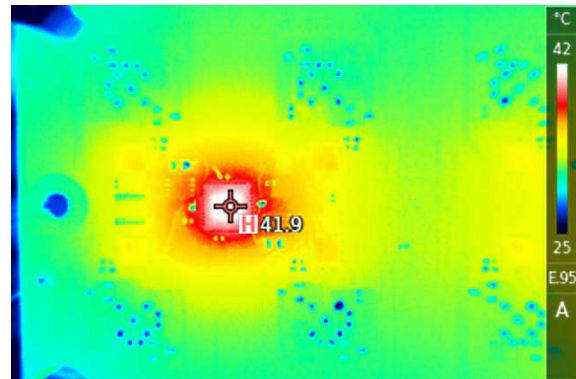


Figure 4-20. Thermal Image at 30V with 4x 1A Output Current

Figure 4-21 shows the current measurement function of the high side switch. The x-axis shows the current drawn from the device, the y axis shows the current reported by the device and the offset.

A similar test is done with the voltage measurement function. Figure 4-22 shows the limited internal voltage sense which causes the curve distortion.

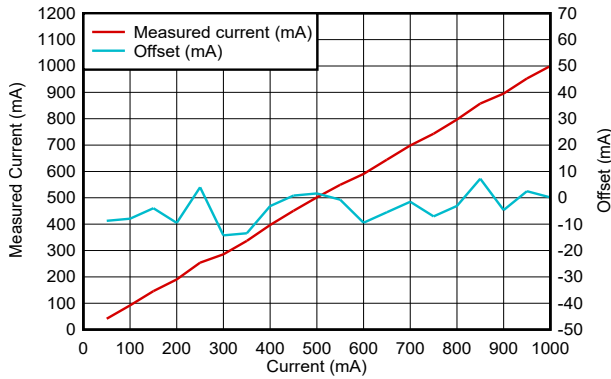


Figure 4-21. Current Measurement

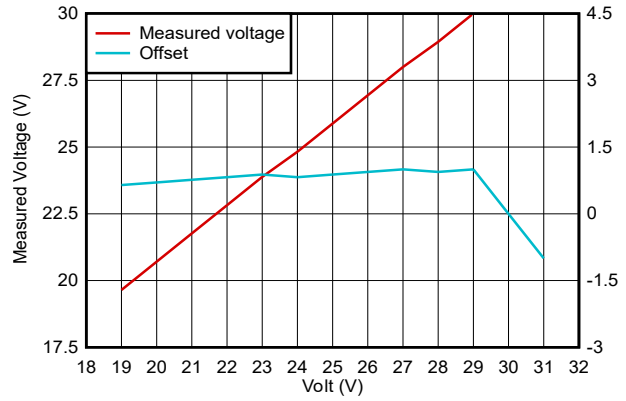
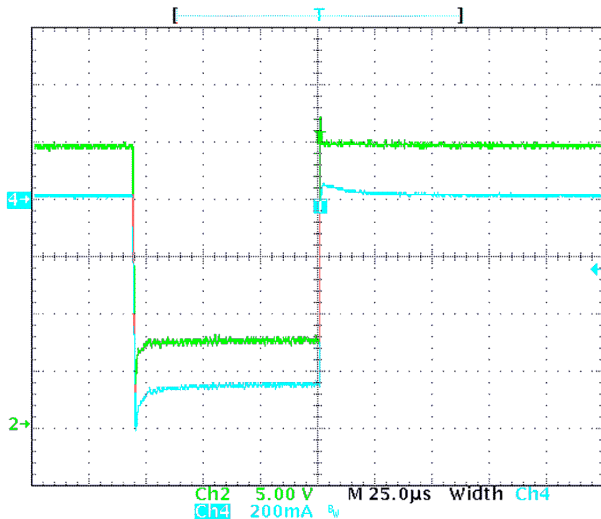


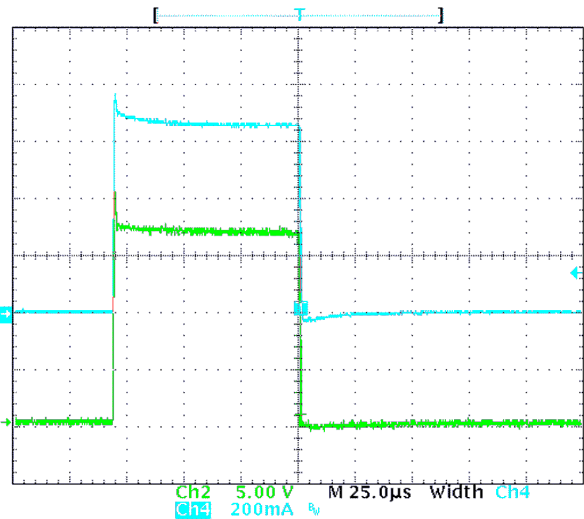
Figure 4-22. Voltage Measurement

4.4.2 TIOL221

To be able to start a IO-Link communication, driving the CQ line with at least 500mA to issue a wake-up signal to the connected IO-Link device is critical. Test this function by connecting a 22Ω resistor between CQ and L- (CQ and L+ to test low side driver). This configuration brings the TIOL221 output driver in the current limit including tolerances. The maximum current is also observed. Figure 4-23 and Figure 4-24 show the current drive capability exceeds 500mA which is required to drive a proper wake-up. The pulse length is within the tolerances.



Green = CQ Voltage Blue = CQ current



Green = CQ Voltage Blue = CQ current

Figure 4-23. CQ Line Low Side Driver Wake Pulse

Figure 4-24. CQ Line High Side Driver Wake Pulse

The TIOL221 also includes weak pull up and down current sources on the inputs, CQ and DI with 50µA strength. Figure 4-25 shows an example of one of these current sinks. This example shows the weak pull down current source on the CQ line and is different from the 5mA IO-Link pull down current sink tested in Figure 4-26. This current sink is specified to pull down 5mA at minimum and typically 8.5mA. At 8.45mA, the test comes very close to the typical value.

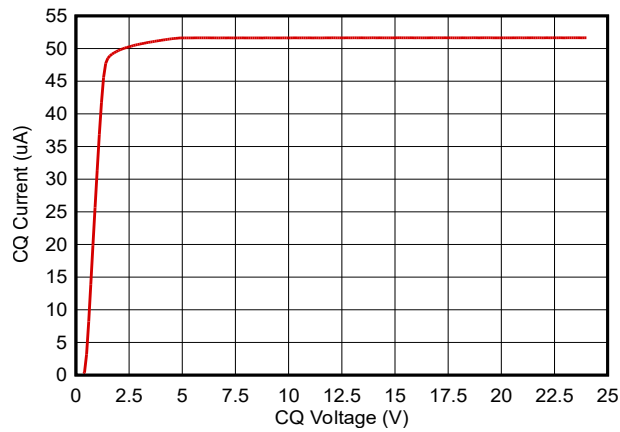


Figure 4-25. CQ 50µA Weak Pull Down

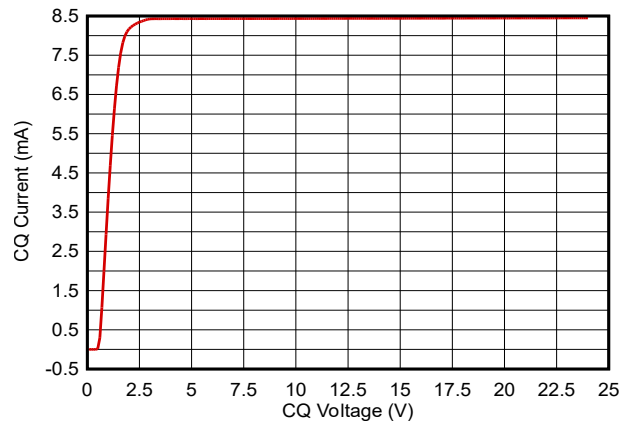


Figure 4-26. CQ IO-Link Pull Down

Figure 4-27 through Figure 4-30 shows the behavior of the digital output channel with different current limits is tested. The DO line is loaded with an electronic load and the current is increased until the voltage drops. As expected, the device keeps the voltage at 24V when the current is below the set current limit. At a certain point the voltage drops sharply and the current is not increasing further.

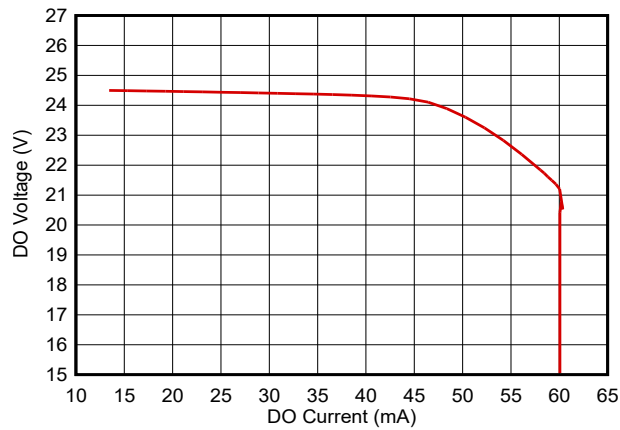


Figure 4-27. DO Driver Current Limit at 35mA Setting

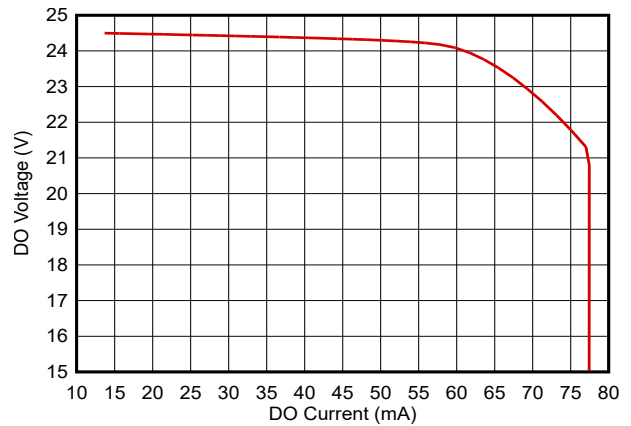


Figure 4-28. DO Driver Current Limit at 50mA Setting

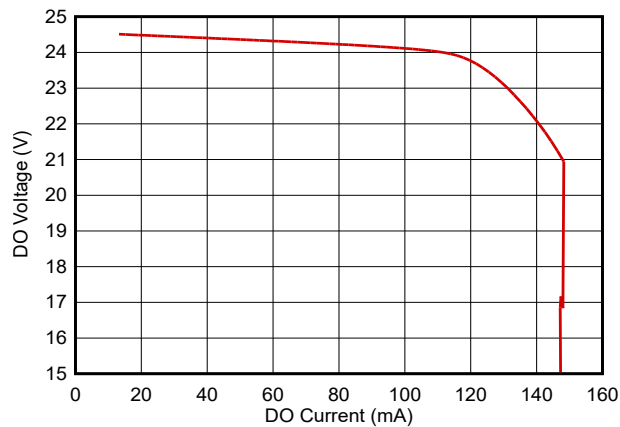


Figure 4-29. DO Driver Current Limit at 100mA Setting

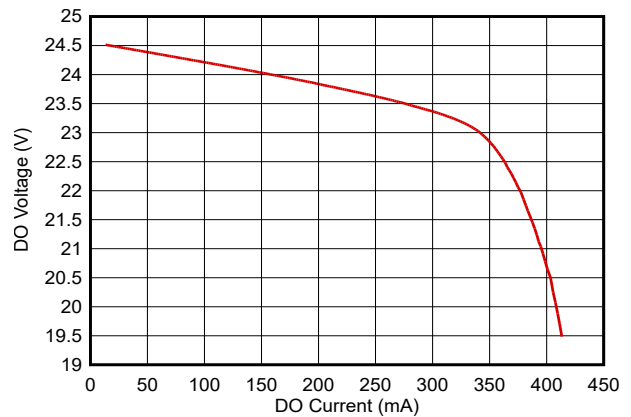


Figure 4-30. DO Driver Current Limit at 300mA Setting

4.4.3 Input Protection and Start-up

The reference design includes a protection against reverse voltage, over voltage, under voltage. This protection also provides a inrush current limitation and EMI filtering.

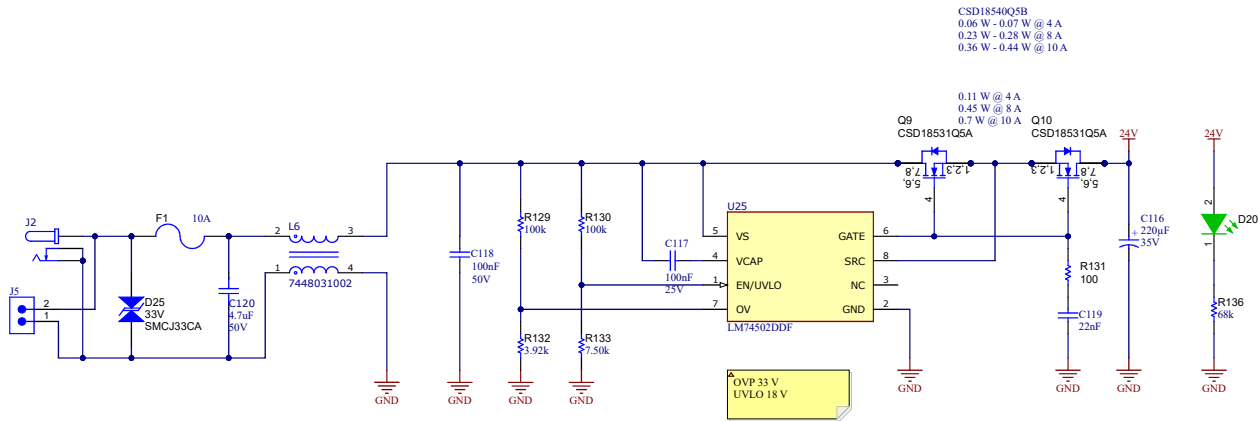


Figure 4-31. Input Protection

All tests are done only including the schematic snippet shown in Figure 4-31.

Looking at the inrush behavior, Figure 4-32 through Figure 4-37 show how the internal 24V rail rises after voltage is applied, the inrush current and when the reset of the CPU is released at different input voltages. Therefore the input voltage is applied at J5 with fast rise time (hot plugged), the current is measured using a current clamp, the other voltages are senses in the circuit.

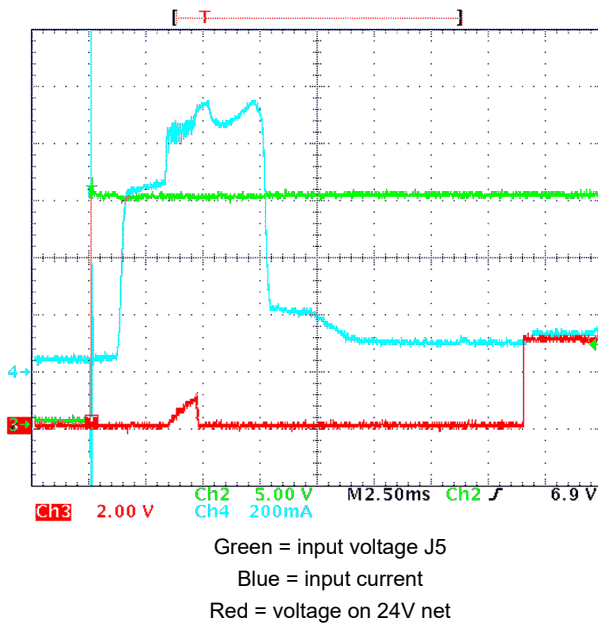


Figure 4-32. Power Up at 20V until CPU Reset Released

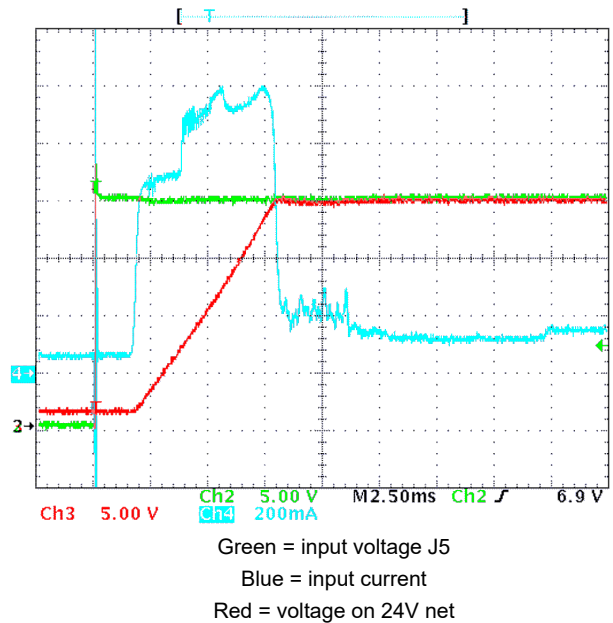
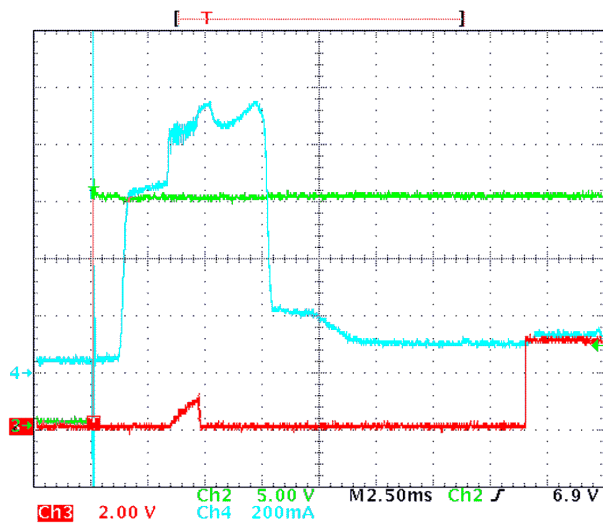
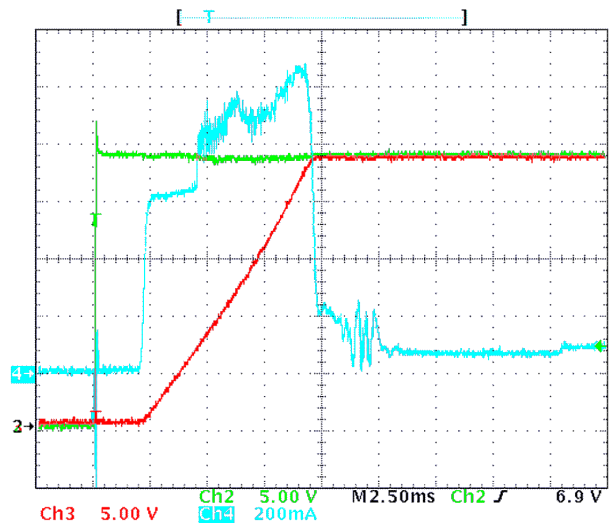


Figure 4-33. Inrush at 20V



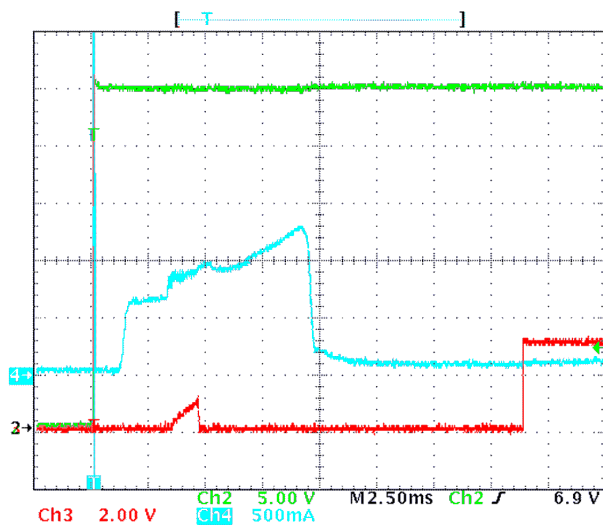
Green = input voltage J5
Blue = input current
Red = reset signal

Figure 4-34. Power Up at 24V Until CPU Reset Released



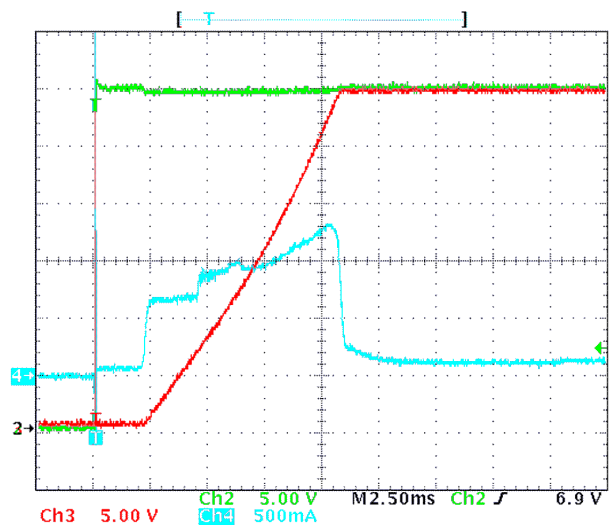
Green = input voltage J5
Blue = input current
Red = voltage on 24V net

Figure 4-35. Inrush at 24V



Green = input voltage J5
Blue = input current
Red = reset signal

Figure 4-36. Power up at 30V until CPU reset released



Green = input voltage J5
Blue = input current
Red = voltage on 24V net

Figure 4-37. Inrush at 30V

In the plots above, the hotplugging together with C120 causes the spike in current at the trigger point. Afterward, the input capacitor C116 (and the ones close to the first DC/DC) get charged, causing an inrush current. When looking closely at the current, it is also visible when the reset is released, as it increases the input current. After inrush is completed and the internal 24V rail has reached 18V, the internal DC/DC converters start up one after the other as seen in [Figure 4-38](#).

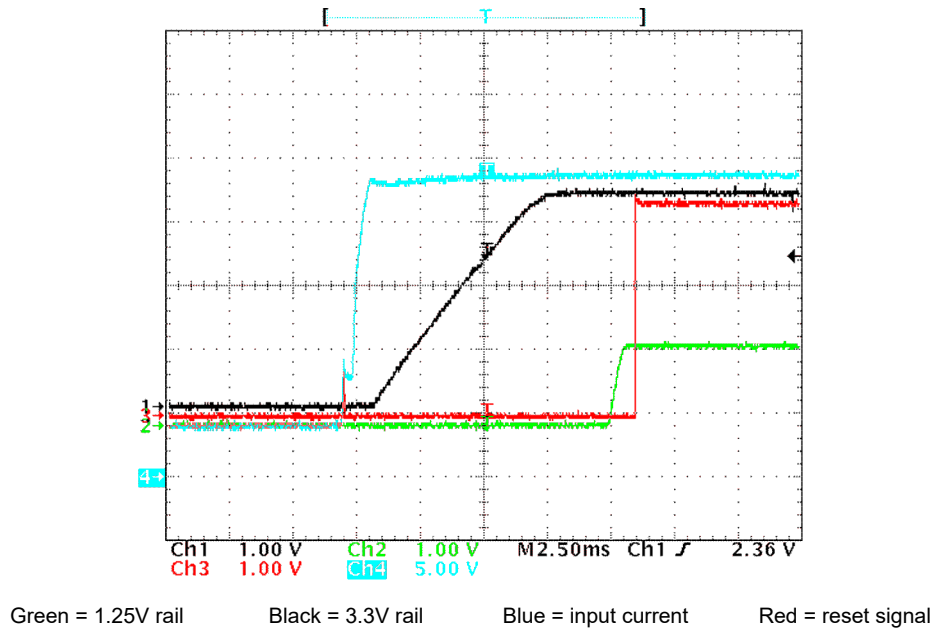


Figure 4-38. Startup of DC/DC Converters Until Reset is Released

The following table summarizes the resulting slew rates, inrush peak currents and timings until CPU starts.

Supply Voltage	Rise Time Internal 24V	Time to CPU Start	Peak Current
20V	5ms	18ms	900mA
24V	7.5ms	18ms	1.1A
30V	8ms	18ms	1.3A

Beside the timing, also the voltages of the under and over voltage protection are verified and listed in table below. The voltage levels are in the designed range, also the hysteresis is as expected withing the given tolerances.

UVLO nominal 90mV hysteresis, voltage divider R130/R133, $100k/7.5k$, $0.09V / (7.5k/(100k + 7.5k)) = 1.29V$

OVLO nominal 100mV hysteresis, voltage divider R129/R132, $100k/3.92k$, $0.1V / (3.92k/(100k+3.92k)) = 2.65V$

Test Case	Voltage Level
Under voltage falling	16.3V
Under voltage rising	17.5V
Under voltage hysteresis	1.2V
Over voltage rising	33.2V
Over voltage falling	30.7V
Over voltage hysteresis	2.5V

The two pass FETs Q9 and Q10 need to carry the whole current of the board. If all ports are loaded with 1A, this current adds up to a bit more than 8A, causing some power dissipation. The thermal image below shows the FET to heat up to 70°C at room ambient temperature when loaded with 9A. Depending on the application and ambient/housing, this amount can be too much.

If the system is loaded only with 5A, the FET heats up to less than 50°C. Depending on the designed in simultaneity factor this still can be a way to go. Otherwise a different FET such as CSD18540Q5B can be used to bring down the power dissipation.

Also keep in mind the power dissipation of the fuse. The 10A fuse here is specified with 7.3mΩ, and a typical voltage drop of 110mV. This causes another 730mW to 1.1W. Which is more than the CSD18531Q5A FET.

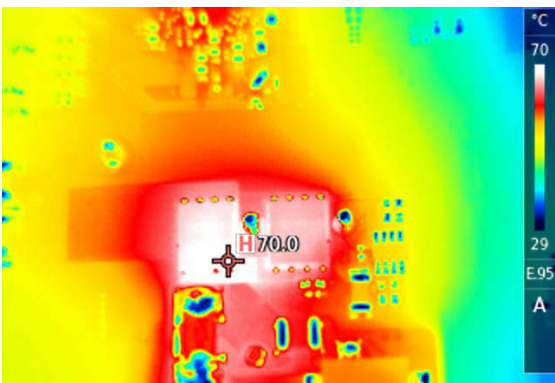


Figure 4-39. CSD18531Q5A Loaded with 9A

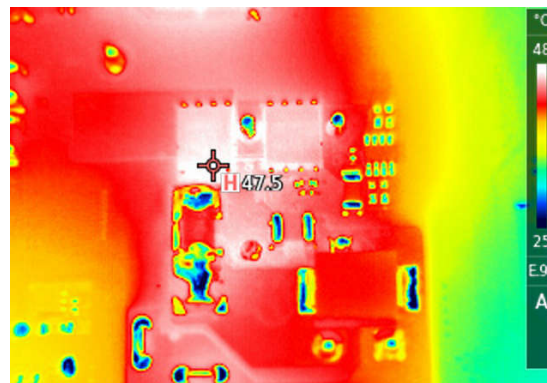


Figure 4-40. CSD18531Q5A Loaded with 5A

Figure 4-41 shows the area with CSD18540Q5B is about 20K cooler than with CSD18531Q5A when loaded with 9A, which is expected. With 5A load, the difference is not that significant.

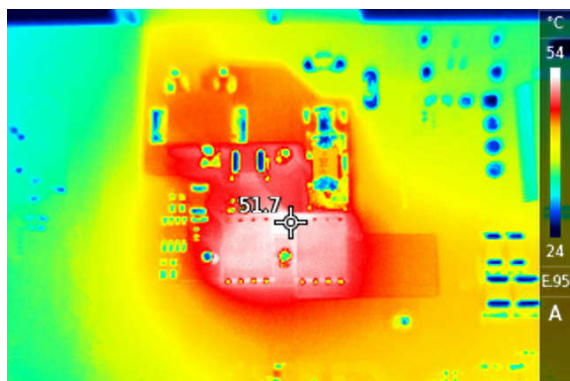


Figure 4-41. CSD18540Q5B Loaded with 9A

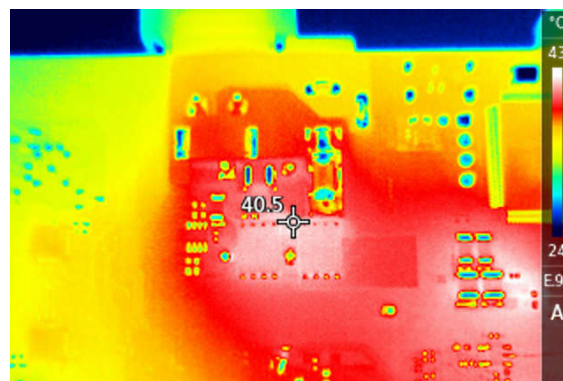


Figure 4-42. CSD18540Q5B Loaded with 5A

4.4.4 EMC/EMI Compliance

This reference design is tested to meet EMI and EMC requirements for an IO-Link Master product. This section describes the test details.

Specification	Test	Class	Limits	Result	Details
CISPR 32	Radiated EMI		Class B	PASS	Link to section CISPR 32 - Radiated Emissions
EN61000-6-3	DC-IN		EN61000-6-3 EMCL AC	PASS	EN61000-6-3 - Conducted Emissions
EN61000-6-3	Ethernet		EN61000-6-3 EMCL AC	PASS	EN61000-6-3 - Conducted Emissions
IEC 61000-4-2	ESD	A	6kV CD, 15kV HCP at 1Hz	PASS	IEC 61000-4-2 - Electrostatic Discharge (ESD)
EN 61000-4-3	Radiated Immunity	A	80MHz–1GHz 20V/m 1GHz–6GHz 10V/m	PASS	EN 61000-4-3 - Radiated Immunity
IEC 61000-4-4	DC-IN	A	2kV	PASS	IEC 61000-4-4 Burst / EFT
IEC 61000-4-4	Ethernet	A	2kV crit.A / 3kV crit.B	PASS	IEC 61000-4-4 Burst / EFT
IEC 61000-4-4	IO-Link	A	2kV	PASS	IEC 61000-4-4 Burst / EFT

Specification	Test	Class	Limits	Result	Details
IEC 61000-4-5	Shielded Ethernet	A	500/1000/2000 V	PASS	IEC 61000-4-5 Surge
IEC 61000-4-5	IO-Link		500V line to line, 2kV line to Earth, 42Ω	PASS	IEC 61000-4-5 Surge
IEC 61000-4-6	DC-IN	A	150kHz–80MHz 20V/m	PASS	IEC 61000-4-6 Conducted Immunity
IEC 61000-4-6	IO-Link	A	150kHz–80MHz 20V/m	PASS	IEC 61000-4-6 Conducted Immunity
IEC 61000-4-6	Ethernet	A	150kHz–80MHz 20V/m	PASS	IEC 61000-4-6 Conducted Immunity

4.4.5 CISPR 32–Radiated Emissions

To test the emissions of the TIDA-011002 reference design, the board and additional IO-Link sensor is placed inside the chamber. Both Ethernet ports are converted to fiber using two media converters. The Ethernet signal is brought out of the chamber. Power is supplied from an external 24V power supply. An IO-Link communication to the sensor is established and the process data is transmitted through Ethernet to a PC outside. In addition, Ethernet traffic is generated using iperf3, as both Ethernet ports are acting as a switch, both ports are fully loaded this way.

Figure 4-44 shows the setup in the chamber.

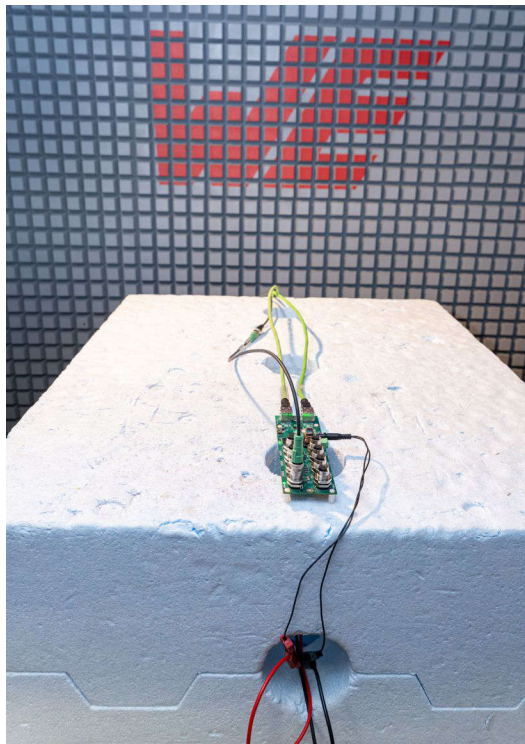


Figure 4-43. Radiated Emissions Results

Now with the complete setup running, these measurements were made.

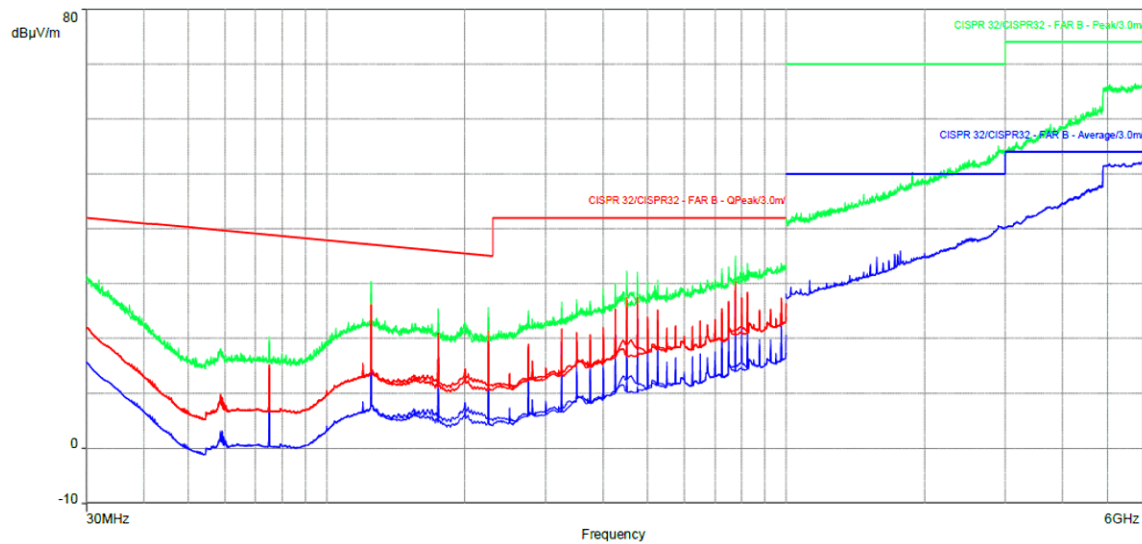


Figure 4-44. Radiated Emissions Setup in Test Chamber

The reference design is well below the CISPR32 class B limit and meets these requirements. The remaining visible frequencies are multiple of 25MHz and most likely caused by the traces from the oscillator going to processor and the two Ethernet PHYs. Shielding the traces in an inner layer can reduce the emissions further.

4.4.6 EN61000-6-3–Conducted Emissions

During this test, the energy the DUT emits on the ports to the outside is measured. To measure the energy, the Ethernet ports and the DC input are connected through coupling networks. The reference design is configured to establish an IO-Link communication and the Ethernet ports are fully loaded using iperf3. Figure 4-45 shows the test setup. The two CDNs for the Ethernet ports are in the foreground and the LISN connected to the DC port is in the back. A IO-Link sensor is connected to one of the ports. This test is done on the Ethernet ports and on the power supply. The test setup remains the same, the CDN outputs not used for a measurement are 50Ω terminated.

For this type of equipment, no limit for the emissions on the power supply is given, so a rather stringent limit is taken for the measurements.

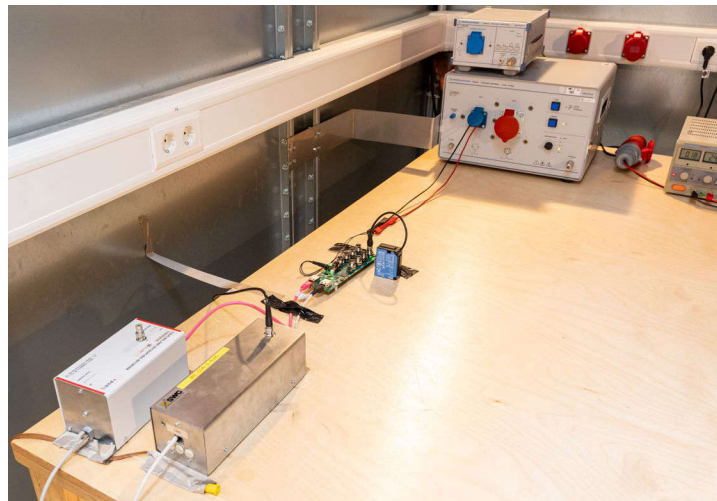


Figure 4-45. Conducted Emissions Setup

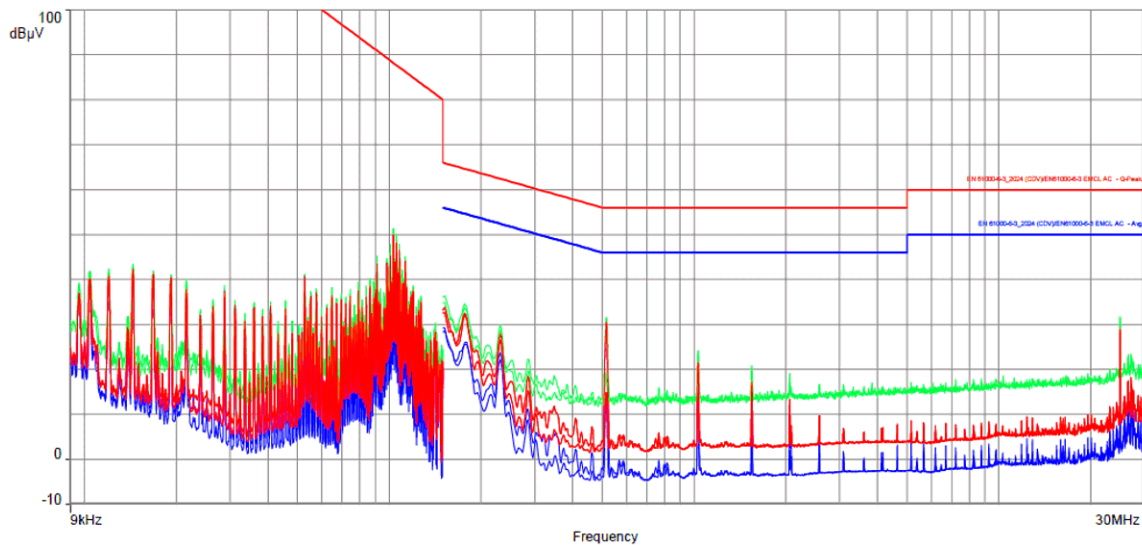


Figure 4-46. Conducted Emissions DC Port without Earth Connection

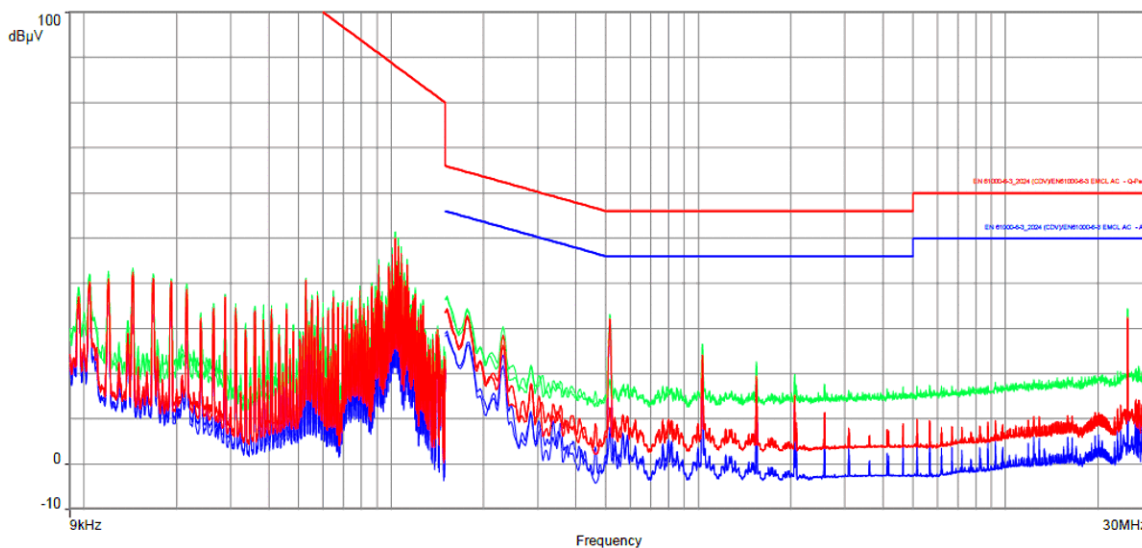


Figure 4-47. Conducted Emissions DC Port with Earth

Figure 4-46 and Figure 4-47 show the conducted emissions on the DC port, both lines (24V and GND) with functional earth connected and without. There is no significant difference between the two measurements. The peak at 25MHz is about 5dB higher with earth connected but still almost 30dB below the limit.

The noise is below 150kHz, and the peaks show up every 2.5kHz, which equals the frequency of process data exchange. The system is configured to exchange process data every 400µs --> 2.5kHz.

The switching frequency of the first DC/DC converter of 500kHz is visible but suppressed well.

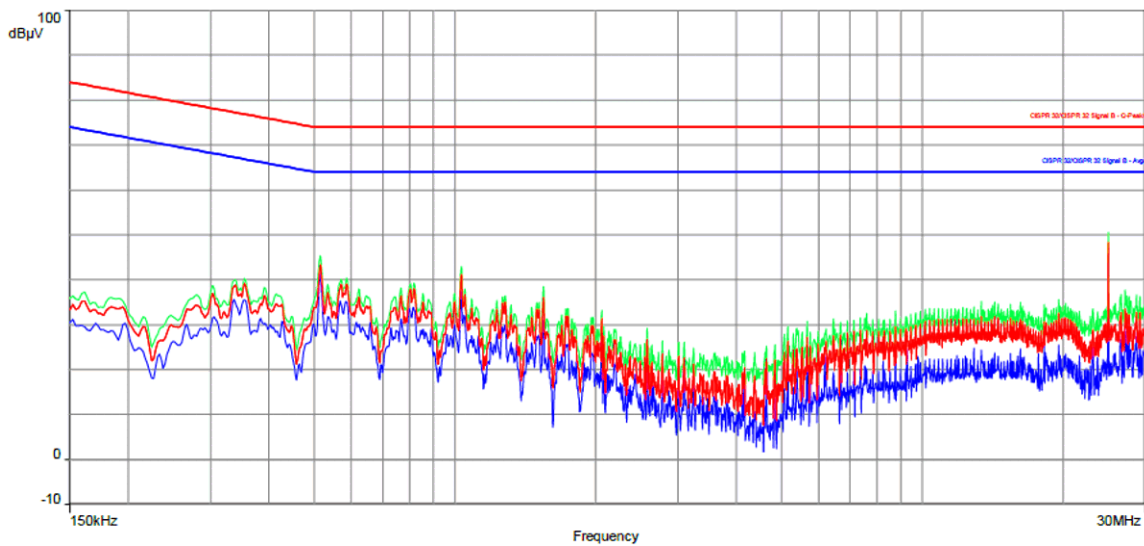


Figure 4-48. Conducted Emissions on Ethernet Port

Figure 4-48 show the emitted voltage on the ethernet port which is the same on the shield of both Ethernet ports. The shield also shows no problems. The 25MHz clock is visible but more than 20dB below the limit.

4.4.7 IEC 61000-4-2–Electrostatic Discharge (ESD)

For this test, the communication on both Ethernet and IO-Link is active and the failure rate is monitored. The reference design is powered from a battery. Figure 4-49 and Figure 4-50 show the setup.

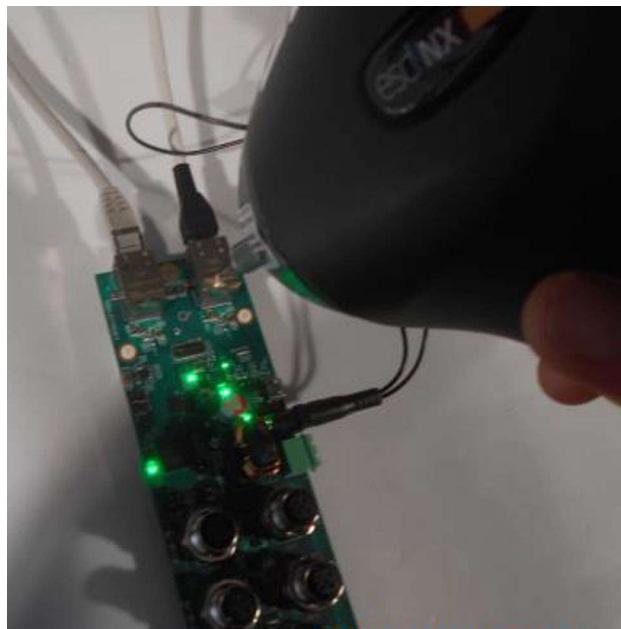


Figure 4-49. ESD Contact Discharge into Ethernet Port

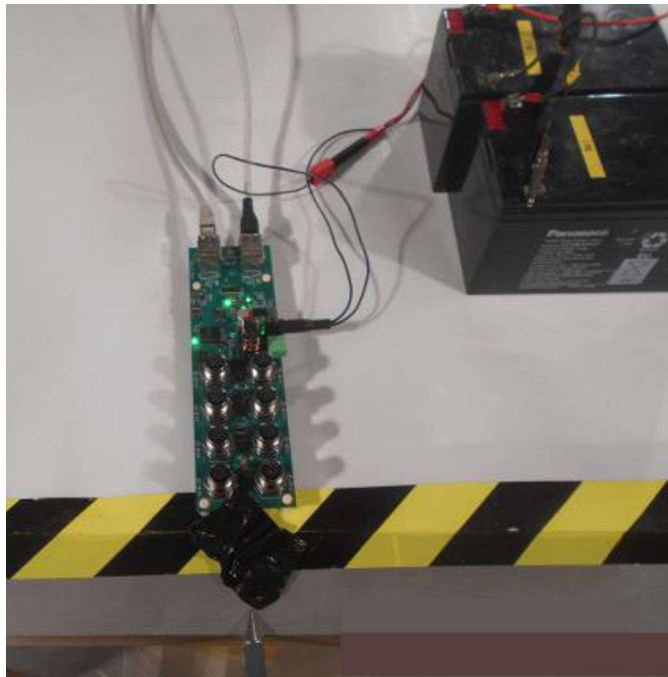


Figure 4-50. ESD Discharge into Horizontal Coupling Plane (HCP)

The reference design is expected to handle $\pm 6\text{kV}$ at 1Hz repetition rate into the Ethernet Ports without losing link or any data. With the HCP, the design can handle $\pm 15\text{kV}$ without data or link loss. In both cases, class A performance is met and the requirements given in the IO-Link standard are exceeded.

The small capacitor of 4.7nF on the reset line placed close to the PHY plays a significant role in meeting these requirements.

4.4.8 EN 61000-4-3–Radiated Immunity

To test the radiated immunity, the setup is very similar to the radiated emission test setup. This time the antenna is used for emitting HF to the reference design. The Ethernet connection and the IO-Link connection is observed and no errors were seen. For the test, 20V/m were used from 80MHz to 1GHz and 10V/m from 1GHz to 6GHz. These levels exceed the levels given by the IO-Link specification.

4.4.9 IEC 61000-4-4 Burst / EFT

For all burst tests the overall setup looks similar, IO-Link and Ethernet is active and monitored for errors. The difference is where the pulses are applied. For this test, 5kHz and 100kHz pulses are used.

4.4.9.1 DC Port

The first test is done on the DC port. The burst is applied using the internal coupling network of the generator. In some cases, the inductance of the coupling network can prevent the internal power supply in the reference design from starting up. The undervoltage protection, a large inrush current, and the inductance causes some oscillation. Prevent oscillation by applying a 1000 μF capacitor capacitance at the output of the coupling network, as shown in [Figure 4-52](#)

The Ethernet lines going to a laptop for data test and monitoring are decoupled using ferrite clamps to reduce the voltage seen at the laptop and reduce the impact of this equipment.

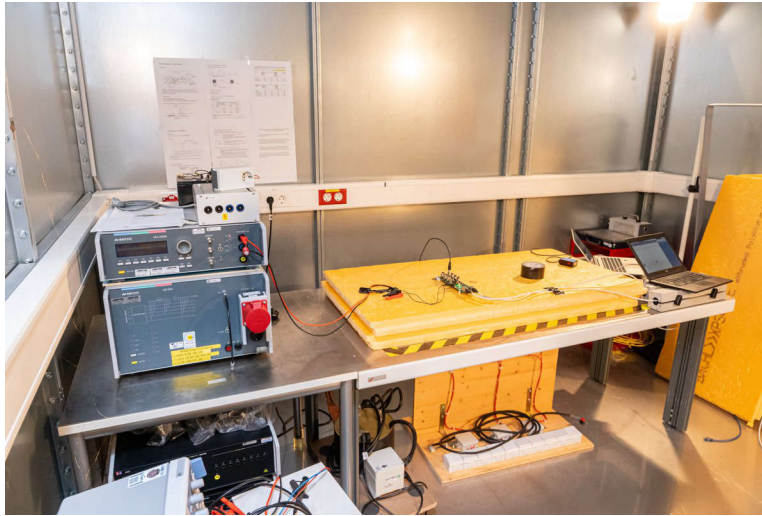


Figure 4-51. Burst Test on DC Port



Figure 4-52. Additional Capacitance on Coupling Network

Without Earth connection and pulses applied as common mode signal to both power supply lines, the communication on IO-Link and Ethernet is stable with 2kV and meeting class A performance.

With Earth connection, the IO-Link communication is working with 1kV meeting class A, but interrupts at 2kV, which results in class B performance. Improve the performance by decoupling the CQ line of the transceiver with a 1nF capacitor to GND. This setup can also achieve class A performance with 2kV.

4.4.9.2 Ethernet

The burst test is also done on the Ethernet port, as shown in [Figure 4-53](#). The burst is now coupled into the system using a capacitive clamp. Again the laptops are decoupled using ferrites.

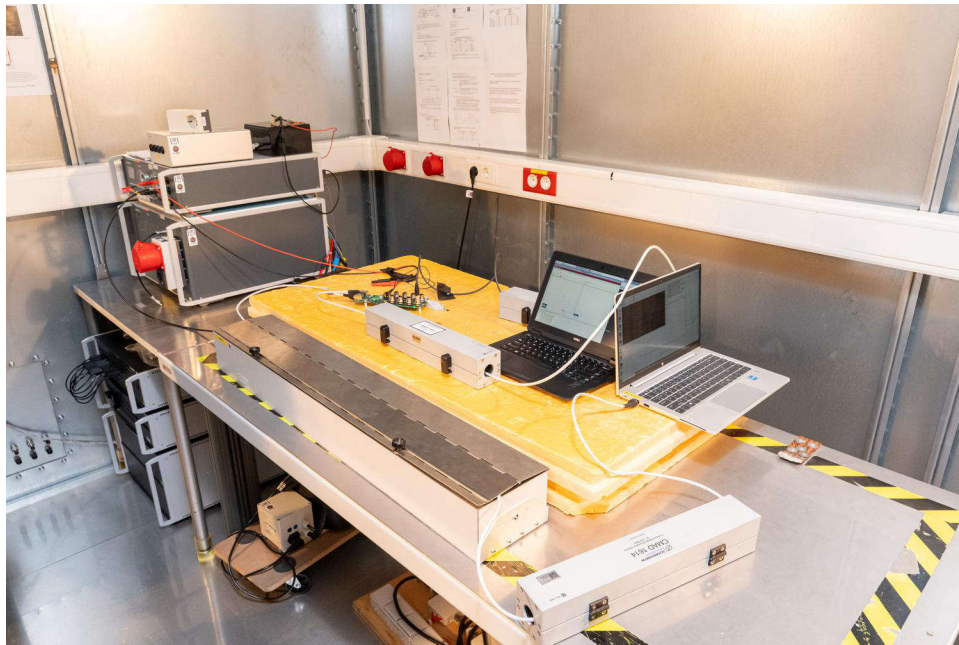


Figure 4-53. Burst Test on Ethernet Port

The Ethernet communication is error-free with 2kV, meeting class A performance. At 3kV, corrupted packets are observed, resulting in a lower data rate. Depending on the application protocols (retransmission if cycle time allows) used, these results can be classified as class A performance, but we defined these results as class B performance. No link drop was seen at this voltage. The auxiliary equipment, such as a laptop, can cause data loss at this voltage.

4.4.9.3 IO-Link

To inject burst pulses on the IO-Link line, the capacitive clamp is used and the cable is fed through. [Figure 4-54](#) shows the test setup

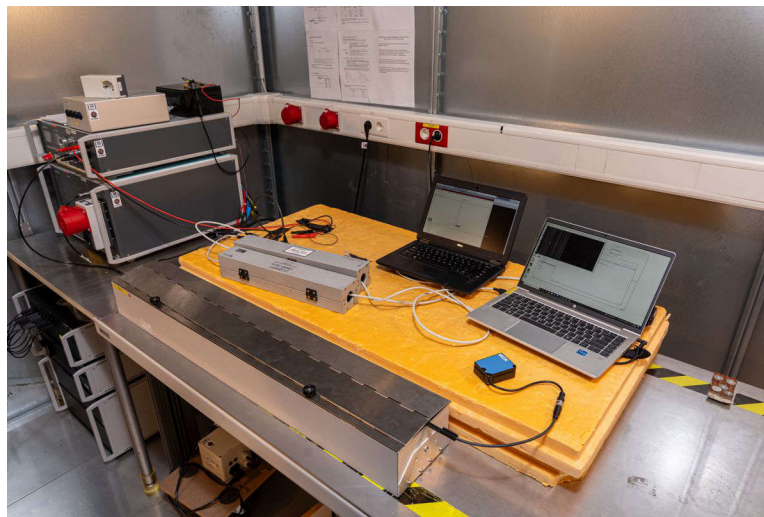


Figure 4-54. Burst Test on IO-Link Port

Without an Earth connection, class A performance can be achieved at 2kV.

With an Earth connection, class A can be achieved at 1kV. When testing on the DC port, a small capacitor of 1nF on the CQ line can improve the performance to meet class A also at 2kV.

4.4.9.4 Summary

All tests met the requirements of IO-Link and **can exceed the requirements**. The following table gives an overview of the tests. TI recommends adding a small capacitor on the CQ line of the TIOL221 because doing so will improve robustness. The number of corrupted M-sequences was not recorded, but whether the IO-Link communication needs to restart was reported.

Test	Voltage	Result	Comment
DC Port without earth connected	2kV	Class A	
DC Port with earth connected	1kV	Class A	
DC Port with earth connected	2kV	Class B	IO-Link restarts communication
DC Port with earth connected and 1nF at CQ line	2kV	Class A	
Ethernet Port	2kV	Class A	
Ethernet Port	3kV	Class B	Packet loss on Ethernet, depending on protocol class A possible
IO-Link Port without earth connected	2kV	Class A	
IO-Link Port with earth connected	1kV	Class A	
IO-Link Port with earth connected	2kV	Class B	IO-Link restarts communication
IO-Link Port with earth connected and 1nF at CQ line	2kV	Class A	

4.4.10 IEC 61000-4-5 Surge

For testing surge on the Ethernet cable, the setup is similar as before except one cable is changed by a long cable and the shield of the cable is connected to the surge generator. The earth of the reference design is connected to earth. [Figure 4-55](#) shows the setup.

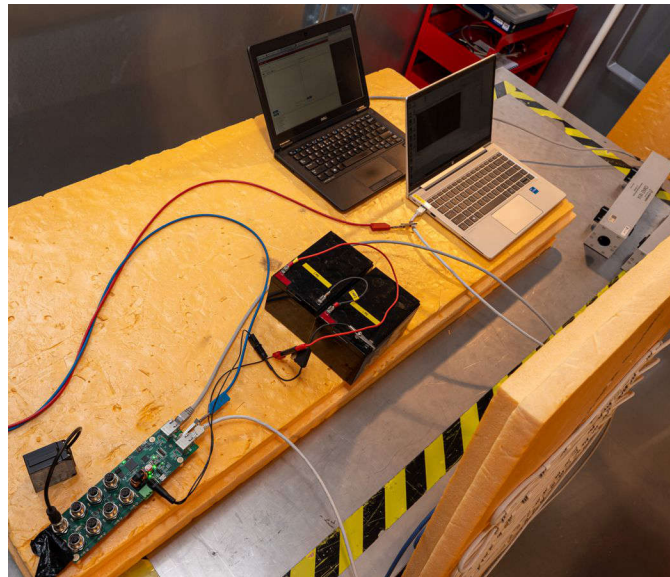


Figure 4-55. Surge Test on Ethernet Port

This test is done with 2Ω source impedance and with voltages up to 2kV. The reference design shows no interference and communication keeps running, which meets class A criteria.

Testing on the IO-Link port while communication is running is not possible in this setup. The cable is unshielded, so the surge needs to be applied through a coupling network into the lines in different configurations like line to line and line to earth. The impedance is 42Ω and leads to less current. However, no communication is possible in COM2 or COM3 through the coupling network. Therefore, surge pulses were applied and the functionality of the IO-Link were checked after. In all configurations, the IO-Link port is still functional after the test was completed.

4.4.11 IEC 61000-4-6 Conducted Immunity

For testing the conducted RF immunity, IO-Link communication and Ethernet communication is established. Iperf3 is running to load Ethernet and observe if packets are lost. RF noise is coupled into the DC port, the IO-Link and the Ethernet, which does not interfere with the communication. Figure 4-56 shows the test setup. Coupling networks (CDN) were used to couple in the RF noise. To communicate through the CDN the IO-Link needs to be configured to use COM2 instead of COM3.

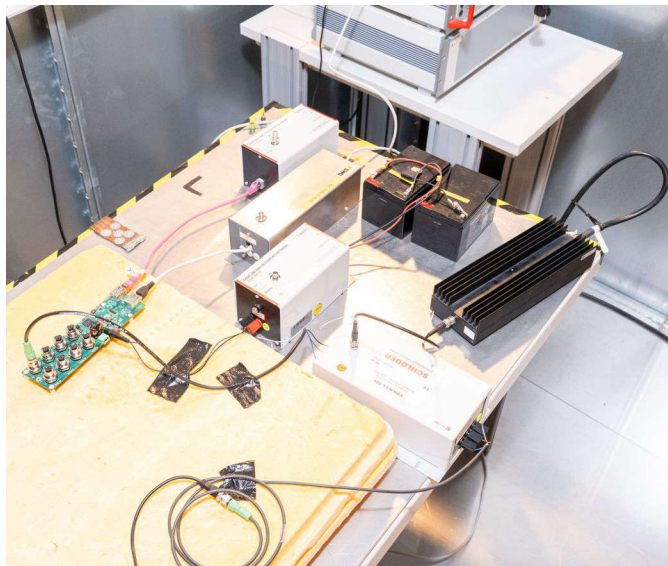


Figure 4-56. Conducted Immunity Setup

An RF voltage of 20V does not interfere with the communication on any port so that the test setup exceeds the requirements of IO-Link.

4.5 Ethernet Compliance

The two Ethernet ports are tested to be compliant to the 100 BASE-TX standard. As the ports support auto MDI-X and therefore can swap RX and TX, this alternative configuration is also tested. The results are summarized in the table below.

Test	Measurement	Value Eth 1	Value Eth 1 MDI-X	Value Eth 2	Value Eth 2 MDI-X	Result
Mask Test	Twisted Pair Active Output Interface template	pass	pass	pass	pass	pass
ANSI 9.1.9	Jitter Base to Upper	401ps	389ps	352ps	397ps	pass
ANSI 9.1.9	Jitter Base to Lower	448ps	452ps	475ps	493ps	pass
ANSI 9.1.2.2	UTP DOV Base to Upper	958.7mV	956mV	957.1mV	954mV	pass
ANSI 9.1.2.2	UTP DOV Base to Lower	968.1mV	967.8mV	967.5mV	961.9mV	pass
ANSI 9.1.4	Signal Amplitude Symmetry	0.998	0.996	0.997	0.999	pass
ANSI 9.1.3	Overshoot Positive	2.2%	2.7%	2.5%	2.7%	pass
ANSI 9.1.3	Overshoot Negative	2.6%	2.5%	2.4%	2.1%	pass
ANSI 9.1.6	Rise Base to Upper	3.189ns	3.237ns	3.003ns	3.030ns	pass
ANSI 9.1.6	Fall Upper to Base	3.421ns	3.434ns	3.330ns	3.440ns	pass
ANSI 9.1.6	Rise Lower to Base	3.492ns	3.598ns	3.383ns	3.429ns	pass

Test	Measurement	Value Eth 1	Value Eth 1 MDI-X	Value Eth 2	Value Eth 2 MDI-X	Result
ANSI 9.1.6	Fall Base to Lower	3.201ns	3.243ns	3.118ns	3.203ns	pass
ANSI 9.1.6	Rise/Fall Symmetry	303ps	361ps	379ps	410ps	pass
ANSI 9.1.8	Duty Cycle Distortion	25.1ps	27.8ps	26.9ps	27.1ps	pass

5 Design and Documentation Support

5.1 Design Files

5.1.1 Schematics

To download the schematics, see the design files at [TIDA-011002](#).

5.1.2 BOM

To download the bill of materials (BOM), see the design files at [TIDA-011002](#).

5.1.3 PCB Layout Recommendations

5.1.3.1 Layout Prints

To download the layer plots, see the design files at [TIDA-011002](#).

5.2 Software

[IND-COMMS-SDK](#) Industrial real-time communications software development kit

5.3 Documentation Support

1. Texas Instruments, [LMR436x0-Q1 36V, 1A / 2A, Automotive Buck Converters With < 2.5 \$\mu\$ A IQ at 150°C TJMAX in 4mm2 HotRod™ QFN datasheet](#)
2. Texas Instruments, [TPS62850x-Q1 2.7V to 6V, 1A, 2A, 3A, Automotive, Step-Down Converters in an SOT583 Package datasheet](#)
3. Texas Instruments, [TLIN1021A-Q1 Fault-Protected LIN Transceiver with Inhibit and Wake datasheet](#)

5.4 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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6 About the Author

STEFFEN GRAF works as a systems engineer at Texas Instruments in the EMEA headquarter in Freising, Germany. Here he is part of the systems engineering team with strong focus on industrial systems supporting customers world wide.

For more than nine years, Steffen has gained experience in different Ethernet technologies including SPE, PoDL and APL, but also other industrial communication protocols such as IO-Link with a focus on hardware level design, firmware validation and EMI/EMC testing.

Steffen holds a Master of Science degree in electrical engineering with a focus on microelectronics from Darmstadt University of Applied Sciences, where he graduated in 2017.

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (March 2026) to Revision A (May 2026)	Page
• Added sections 1 through 7.....	2

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