Design Guide: TIDA-060054

Humanoid Robotics Audio Subsystem Reference Design

Description

This reference design for the audio subsystem of a humanoid robot contains an 8-channel digital microphone interface, which is processed into a single TDM data stream by the high-performance PDM to TDM converter PCMD3180-Q1, and includes a digital input Class-D audio amplifier TAS6511-Q1 to deliver 50W output power to a 2Ω load.

Resources

TIDA-060054	Design Folder
PCMD3180-Q1	Product Folder
TAS6511-Q1	Product Folder
LMR51450-Q1	Product Folder
TLV767-Q1	Product Folder

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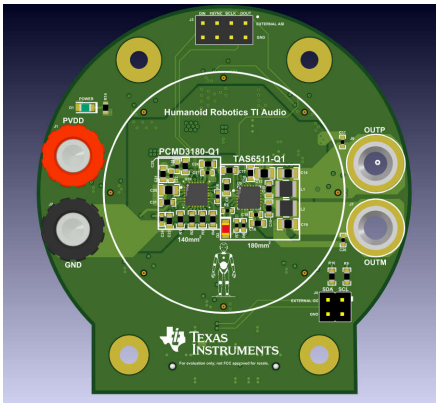
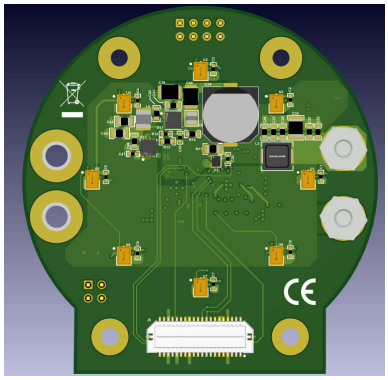
Features

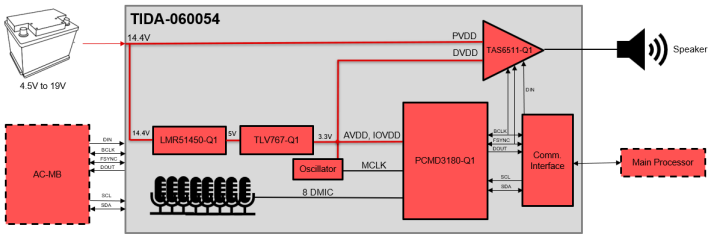
- 4.5V to 19V input voltage range
- 8-channel pulse density modulation (PDM) microphones simultaneous conversion
- 50W output power delivered through a 2Ω load
- Programmable digital volume control
- External ASI and I2C headers for connection with system processor
- Integrated with Audio Converters motherboard for PC audio and programming option
- Bill of materials (BOM) size highlighted

Applications

- Humanoid robot sensor module







1 System Description

The TIDA-060054 enables audio recording of eight on-board digital PDM microphones with the PCMD3180-Q1 PDM to TDM data converter, and audio playback with the digital input class-D audio amplifier TAS6511-Q1, which can deliver 50W output power through a 2Ω load. The TDM audio is processed externally with the audio converters motherboard (AC-MB) or another processor that interfaces with the external ASI and I2C headers.

1.1 Key System Specifications

PARAMETER	SPECIFICATIONS	MINIMUM	TYPICAL	MAXIMUM	UNIT
Input voltage	Battery	4.5	14.4	19	V
Standby current	PCMD3180-Q1, AVDD shutdown		5		µA
	PCMD3180-Q1, IOVDD shutdown		0.1		
	TAS6511-Q1, PVDD shutdown		2		
	TAS6511-Q1, DVDD shutdown		1		
Current consumption	PCMD3180-Q1, AVDD current at 3.3V, 8 PDM channels enabled		11.9		mA
	PCMD3180-Q1, IOVDD current at 3.3V, 8 PDM channels enabled		0.7		
	TAS6511-Q1, PVDD idle current, F_{SW} = 2.048MHz, no audio input		35		
	TAS6511-Q1, DVDD current, Playing -60dB Signal		8		
Speaker load		2	4		Ω
Output power	2Ω load, 10% THD+N		50		W
	2Ω load, 1% THD+N		40		
	4Ω load, 10% THD+N		30		
	4Ω load, 1% THD+N		24		
SNR	PCMD3180-Q1, 5^{th} order PDM modulator		128		dB
	TAS6511-Q1		108		
Audio input/output format		TDM8, TDM16			
Package Size	PCMD3180-Q1	4.00mm × 4.00mm			
	TAS6511-Q1	4.00mm × 4.00mm			
Solution Size	PCMD3180-Q1	140mm^2			
	TAS6511-Q1	180mm^2			

2 System Overview

The integration of an audio system in a humanoid robot is a critical step in enabling real-time communication and natural interaction with a human user, speech processing and response, and spatial awareness. The audio system acts as the ears and mouth of the humanoid robot, using the microphone array positioned around the head to listen to surroundings, and the speaker to emit a voice or sound response. The audio system is typically located in the head unit of the humanoid to be near the body parts the system is replicating.

The TIDA-060054 reference design incorporates all components necessary for the full audio subsystem of a humanoid robot and can be integrated into the larger humanoid design simply by connecting a speaker and power source and routing the audio serial interface signals (BCLK, FSYNC, DOUT and DIN) and I2C control signals (SCL and SDA) to the main system processor. The PCMD3180-Q1 converts the digital microphone data from eight PDM microphones into a single TDM audio stream that is fed directly to the main processor to handle sophisticated algorithms such as echo cancellation, beamforming, and speech recognition. To enable the humanoid to respond, audio playback from the main processor is sent directly to the TAS6511-Q1 digital input audio amplifier through the DIN pin to drive the speaker up to 50W, delivering exceptional power density in a compact design.

2.1 Block Diagram

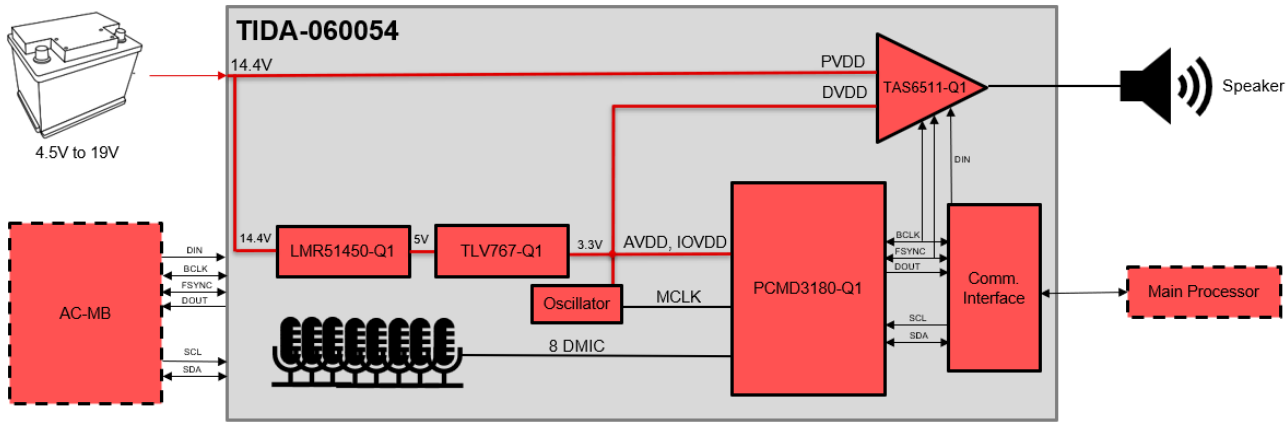


Figure 2-1. TIDA-060054 Block Diagram

2.2 Design Considerations

2.2.1 Codec Design

To more naturally reproduce human-like behaviors, the humanoid must physically turn toward the source of the detected audio and face in that direction while responding. This requires the audio system to collect data from all angles around the humanoid to estimate the location of the source of the sound. Humanoid robot systems rely on microphone design and placement to support algorithms such as beamforming, active noise cancellation, speech recognition, or spatial awareness that require full 360° coverage of audio surrounding the robot.

The TIDA-060054 reference design achieves this omnidirectional sensitivity with a circular arrangement of the eight PDM microphone array around the edge of the printed circuit board (PCB). This placement is flexible, as the microphones can be repositioned closer to or farther from the PCMD3180-Q1 audio converter depending on the system requirements.

The tradeoff of microphone placement is that a larger circular area increases the distance and frequency of sound that can be accurately collected, while a higher microphone density yields better sound localization. A microphone array positioned around a circular area approximately the size of a human head is a suitable compromise for the audio processing required by a humanoid robot.

Most applications use a maximum of eight microphones, which makes the PCMD3180-Q1 a great choice for humanoid robot audio subsystems. Digital microphones are generally preferred to analog microphones in humanoid robotics applications for their superior noise immunity, enabling robust audio processing in a variety of noisy real-world environments, such as outdoors or on a manufacturing floor. The eight PDM microphones on TIDA-060054 are powered by the MICBIAS voltage output from the PCMD3180-Q1.

Furthermore, the TIDA-060054 features an on-board oscillator to provide a 12.288MHz MCLK input to the GPIO1 pin of the PCMD3180-Q1. This provides the option to operate in controller mode, in which the BCLK and FSYNC audio clocks are generated by the PCMD3180-Q1 and sent to the TAS6511-Q1 and external processor. When operating in controller mode, do not supply external BCLK or FSYNC signals. The outputs DOUT, BCLK, and FSYNC are available at the ASI header, while input data DIN must still be supplied to the TAS6511-Q1.

The TDM data and ASI clock signals route to the main processor via the external ASI header. Alternatively, for development and testing, an optional audio converter motherboard (AC-MB) can interface the TIDA-060054 with a PC for audio processing and I2C programming support. The AC-MB is not required for operation. The board can be fully powered by the 14.4V battery input, as the on-board converters generate the 3.3V power rail for the audio devices.

2.2.2 Class-D Amplifier Design

The TAS6511-Q1 Class-D amplifier outputs a square-wave signal with a duty cycle that is proportional to the amplitude of the audio signal. An LC demodulation filter is used to recover the audio signal. The filter attenuates the high-frequency components of the output signals that are out of the audio band. The design of the demodulation filter significantly affects the audio performance of the power amplifier. Therefore, to meet the system THD+N requirements, the selection of the inductors used in the output filter must be carefully considered. The application note LC Filter Design and the Class-D LC Filter Designer calculator provide the tools necessary to design the LC filter. The TIDA-060054 uses a bridge-tied load configuration for the LC filter on the amplifier output, shown in Figure 2-2 with L_{BTL} = 3.3uH and C_g = 1uF.

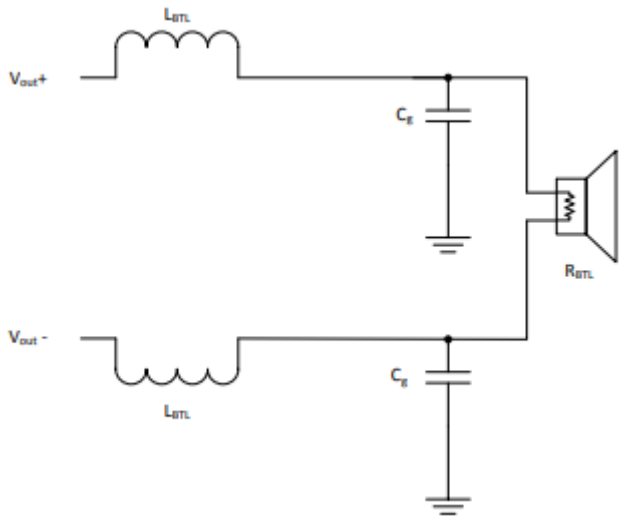


Figure 2-2. Bridge-Tied Load (BTL) Class-D Amplifier LC Filter

Figure 2-3 shows the frequency response of this LC filter for a 2Ω load.

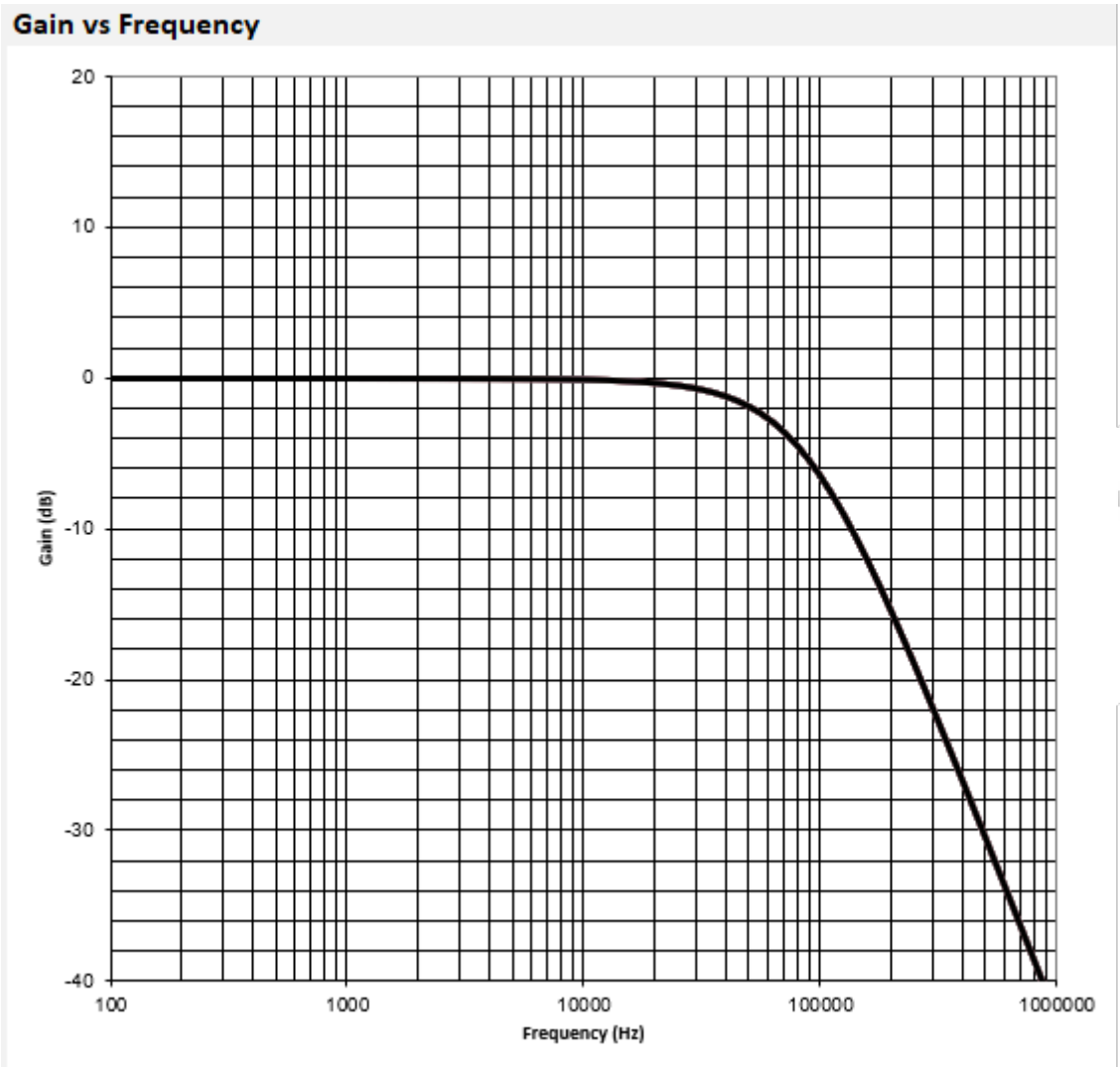


Figure 2-3. Frequency Response of TIDA-060054 Class-D Output LC Filter

The TIDA-060054 also includes a fault indicator LED D2. The red LED monitors the FAULT pin of the TAS6511-Q1, and by default turns on under any of the following conditions:

- Overtemperature shutdown (OTSD) – Latching and non-latching
- Overcurrent Limit and Shutdown events – Latching
- DC Detect – Latching

If desired, the FAULT pin can also be configured to report real-time load diagnostics events to detect shorted load, open load, short-to-power and short-to-ground conditions during audio operation of the amplifier.

2.2.3 Power Design

Battery runtime is one of the most critical considerations in humanoid robot design. High efficiency and low idle power consumption are foundational to making a humanoid viable for real-world operation.

The voltage regulators are chosen to support a current draw up to 1A from the 3.3V supply rail. The PCMD3180-Q1 is optimized to operate on a single 3.3V supply for the AVDD and IOVDD pins. The AVDD and IOVDD pins draw less than 20mA of current combined while recording with eight PDM channels enabled. Table 2-1 and Table 2-2 show the PCMD3180-Q1 power consumption for different combinations of sampling rate, channels enabled, and PDM clock frequencies. More details and information on how to configure and use the device in low-power mode when using digital microphones are discussed in TLV320ADCx140 Power Consumption Matrix Across Various Usage Scenario application note.

Table 2-1. PDM Typical Current Consumption with an External PDM 4th Order Modulator

PDM CLOCK		6.144 MHz	3.072 MHz	1.536 MHz	0.768 MHz
SAMPLING RATE (kHz)	DIGITAL MICROPHONE CHANNELS	AVDD CURRENT AT 3.3 V (mA)	AVDD CURRENT AT 3.3 V (mA)	AVDD CURRENT AT 3.3 V (mA)	AVDD CURRENT AT 3.3 V (mA)
8	8	7.85	7.93	7.89	7.87
16	8	8.97	9.23	9.19	-
24	8	8.92	8.99	8.99	-
32	8	9.71	9.92	-	-
48	8	11.26	11.69	-	-
96	4	11.87	-	-	-

Table 2-2. PDM Typical Current Consumption with an External PDM 5th Order Modulator

PDM CLOCK		6.144 MHz	3.072 MHz	1.536 MHz	0.768 MHz
SAMPLING RATE (kHz)	DIGITAL MICROPHONE CHANNELS	AVDD CURRENT AT 3.3 V (mA)	AVDD CURRENT AT 3.3 V (mA)	AVDD CURRENT AT 3.3 V (mA)	AVDD CURRENT AT 3.3 V (mA)
8	8	7.93	7.92	7.88	7.80
16	8	9.25	9.20	9.15	-
24	8	9.04	8.98	8.91	-
32	8	9.93	9.83	9.77	-
48	8	11.71	11.60	-	-
96	4	12.14	12.05	-	-
192	4	11.96	-	-	-

The TAS6511-Q1 operates with a DVDD digital logic 3.3V supply and PVDD voltage input that can be connected directly to the battery up to 19V. The DVDD pin typically draws around 10mA and the PVDD pin typically draws 35mA when idle. At full output, TAS6511-Q1 delivers best-in-class 90% efficiency at 50W output power, minimizing power draw from the battery.

The two regulators require input capacitors to improve transient performance and noise rejection, and output capacitors for voltage stability. A buck converter is chosen to step down the input voltage to 5V at a high efficiency, while the 3.3V rail is generated from an LDO to minimize noise at the supply pins of the audio devices.

The LMR514500-Q1 device has a recommendation of two 4.7µF input capacitors to reduce ripple current and isolate switching noise from surrounding circuits. The voltage rating must be at least twice the maximum input, so a 50V capacitor is used. The recommended output capacitors are two 33µF capacitors to improve transient response and add stability for a 5V output. The output inductor and resistor feedback network is designed for an output voltage of 5V and 440kHz switching frequency. The TLV767-Q1 device has a recommendation for a 1µF input capacitor to improve transient response, input ripple, and PSRR, although one is not required. Dynamic performance of the device is improved with the use of an output capacitor, with a value of 2.2µF recommended for stability.

2.3 Highlighted Products

2.3.1 PCMD3180-Q1

The PCMD3180-Q1 is a high-performance, low-power, flexible, 8-channel, pulse density modulation (PDM) input to time-division multiplexing (TDM) or I2S audio output converter with extensive feature integration. This device is intended for applications in voice-activated systems, portable computing, communication, and entertainment applications. The low power consumption makes this device appropriate for battery-powered portable audio systems. This device integrates a host of features that reduces cost, board space, and power consumption in space-constrained, battery-powered, consumer, home, and industrial applications.

The PCMD3180-Q1 consists of the following blocks:

- Eight-channel, pulse density modulation (PDM) digital microphone interface with high-performance decimation filter
- Low-noise, microphone bias output to power the digital microphones
- Programmable decimation filters with linear-phase or low-latency filter
- Programmable digital volume control, biquad filters for each channel
- Programmable phase and gain calibration with fine resolution for each channel
- Programmable high-pass filter (HPF), and digital channel mixer
- Integrated low-jitter phase-locked loop (PLL) supporting a wide range of system clocks
- Integrated digital and analog voltage regulators to support single-supply operation

Communication to the PCMD3180-Q1 to configure the control registers is supported using an I2C or SPI. The device supports a highly flexible audio serial interface (time-division multiplexing [TDM], I2S, or left-justified [LJ]) to transmit audio data seamlessly in the system across devices. The device can support multiple devices by sharing the common I2C and TDM buses across devices. Moreover, the device includes a daisy-chain feature and a secondary audio serial output data pin. However, these features require the use of a GPIO pin. With 8 PDM microphones connected, the only available GPIO pin is GPIO1, which is used as a MCLK input in TIDA-060054.

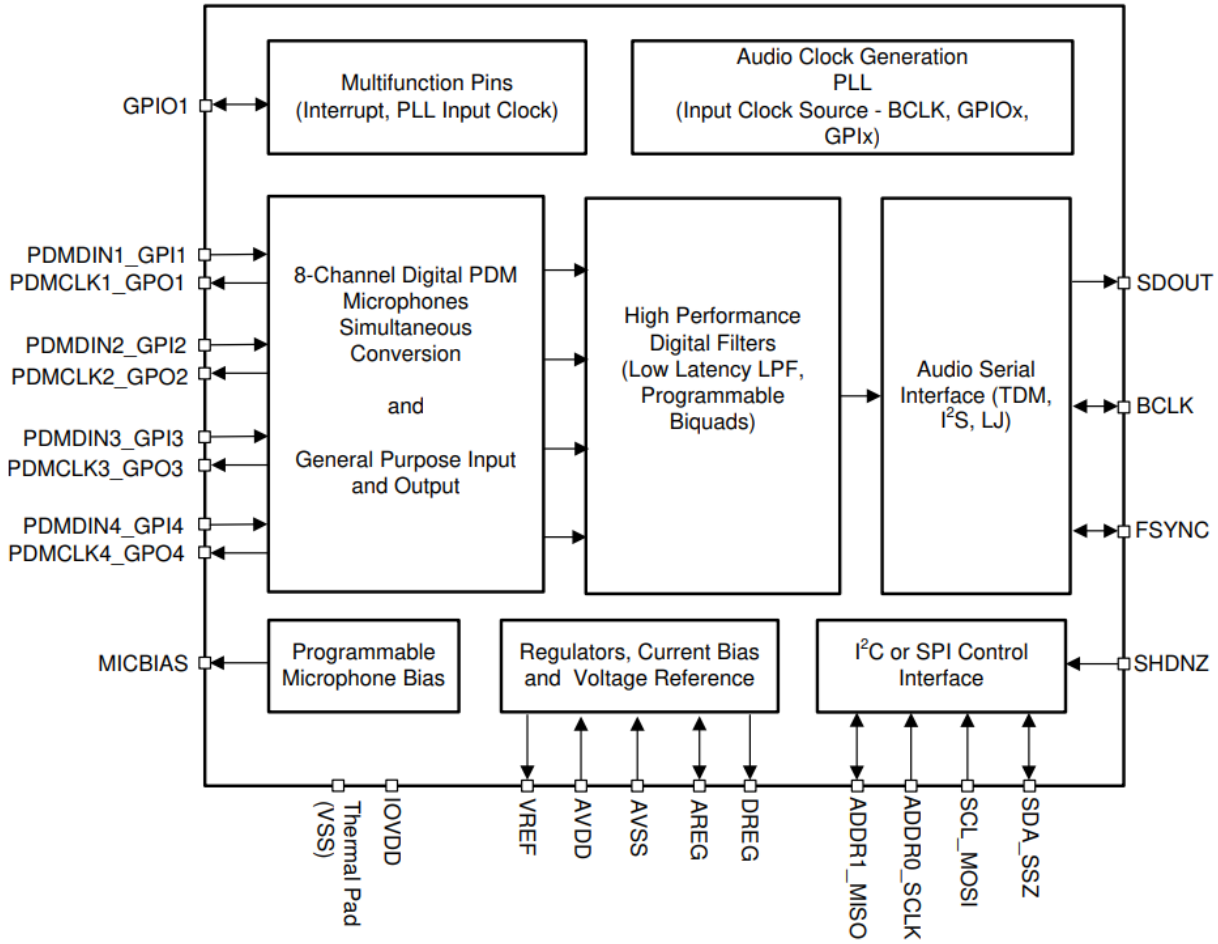


Figure 2-4. PCMD3180-Q1 Functional Block Diagram

2.3.2 TAS6511-Q1

The TAS6511-Q1 is a mono-channel, digital-input, Class-D audio amplifier that supports 2MHz switching frequency enabling a cost and size-optimized single-channel audio amplifier design. The device operates from 4.5V to 19V and delivers up to 30W (14.4V, 4Ω, 10% THD+N) and up to 50W (14.4V, 2Ω, 10% THD+N). The device integrates DC and AC load diagnostics to determine the status of the connected load before enabling the output stage. Additionally, the device can monitor the output load condition while in PLAY mode with or without

audio using real-time load diagnostics which operate independently from the host and audio input. Real-time load diagnostics (RTLDG) allow the detection of shorted load (SL), open load (OL), short-to-power (S2P) and short-to-ground (S2G) conditions during audio operation of the amplifier.

The device is available in a small pad-down TSSOP and QFN with wettable flanks packages, enabling a heatsink-free audio amplifier design.

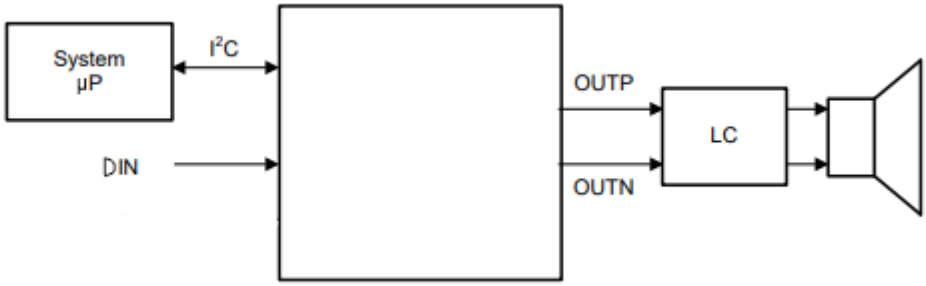


Figure 2-5. TAS6511-Q1 Simplified Block Diagram

2.3.3 LMR51450-Q1

The LMR514x0-Q1 converter is an easy-to-use, synchronous, step-down DC/DC buck converter operating from a 4V to 36V supply voltage. The device is capable of delivering up to 4A or 5A DC load current in a very small design size. The LMR514x0-Q1 features adjustable switching frequency from 200kHz to 1MHz with an external resistor, which provides the flexibility to optimize either efficiency or external component size. The family has multiple versions applicable to various applications. The LMR514x0-Q1 employs fixed-frequency peak-current mode control. The pulse frequency modulation (PFM) version enters PFM mode at light load to achieve high efficiency. A forced pulse width modulation (FPWM) version is provided to achieve low output voltage ripple, tight output voltage regulation, and constant switching frequency at light load. This reference design uses the PFM version. The device is internally compensated, which reduces design time and requires few external components. Additional features, such as precision enable and internal soft start, provide a flexible and easy-to-use design for a wide range of applications. Protection features include thermal shutdown, VIN undervoltage lockout, cycle-by-cycle current limit, and hiccup mode short-circuit protection. This family of devices requires very few external components and has a pinout designed for simple, optimum PCB layout.

2.3.4 TLV767-Q1

The TLV767-Q1 is a wide input linear voltage regulator supporting an input voltage range from 2.5V to 16V and up to 1A of load current. The output range is from 0.8V to 12V or up to 14.6V with the adjustable version. The wide input voltage range makes the device a good choice for operating from transformer secondary windings and regulated rails such as 10V or 12V. Additionally, the wide output voltage range allows the device to generate the bias voltage for silicon carbide (SiC) gate drivers and microphones as well as power microcontrollers (MCUs) and processors. The TLV767-Q1 has a 1% output accuracy that is required for powering digital loads with tight supply requirements. The internal soft-start circuit reduces inrush current during startup, thus allowing for smaller input capacitance. Wide bandwidth PSRR performance is greater than 70dB at 1kHz and 46dB at 1MHz, which helps attenuate the switching frequency of an upstream DC/DC converter and minimizes post regulator filtering. The high ripple rejection from 20Hz to 20kHz makes the device a good choice for powering audio components.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Hardware Requirements

The hardware design includes the blocks discussed previously as well as an AC-MB to send I2C commands and audio to the PCMD3180-Q1 and TAS6511-Q1. In the final system, the AC-MB controller is replaced with a compatible MCU. When evaluating this design, any I2C controller can be used by connecting at the SCL and SDA header pins.

3.2 Software

The PPC3 GUI is used to send the I2C commands. The format of the scripts is:

R/W I2C Address Register Address Data

3.2.1 Example Script

The following I2C commands show how to set up the PCMD3180-Q1 for processing the 8-channel PDM microphone array, and the TAS6511-Q1 for audio playback.

```
## PCMD3180-Q1 Device Setup ##
 ################################################################
# PDM 8-channel: PDMDIN1 - Ch1 and Ch2, PDMDIN2 - Ch3 and Ch4,
# PDMDIN3 - Ch5 and Ch6, PDMDIN4 - Ch7 and Ch8
# PDMCLKx = 2.8224MHz
# FSYNC = 48kHz (Output Data Sample Rate), BCLK = 12.288MHz (BCLK#FSYNC = 256)
 ################################################################
w 98 00 00 # Select Page 0
w 98 01 01 # Software Reset
w 98 00 00 # Select Page 0
w 98 02 81 # Exit Sleep Mode
w 98 00 00 # Select Page 0
w 98 07 30 # TDM, 32-bit
w 98 0B 00 # Channel 1 to TDM slot 0
w 98 0C 01 # Channel 2 to TDM slot 1
w 98 0D 02 # Channel 3 to TDM slot 2
w 98 0E 03 # Channel 4 to TDM slot 3
w 98 0F 04 # Channel 5 to TDM slot 4
w 98 10 05 # Channel 6 to TDM slot 5
w 98 11 06 # Channel 7 to TDM slot 6
w 98 12 07 # Channel 8 to TDM slot 7
w 98 13 81 # Controller mode with MCLK = 12.288MHz
# w 98 13 01 # Replace the command above for Target Mode
w 98 14 48 # FSYNC = 48kHz, BCLK/FSYNC = 256
w 98 1F 40 # PDMCLK is 2.8224MHz or 3.072MHz
w 98 20 00 # PDMCLK Channel 1/3/5/7 latch on negative edge, Channel 2/4/6/8 latch on positive edge
w 98 21 A0 # GPIO1 configured as MCLK input
w 98 22 41 # GPO1 = PDMCLK1
w 98 23 41 # GPO2 = PDMCLK2
w 98 24 41 # GPO3 = PDMCLK3
w 98 25 41 # GPO4 = PDMCLK4
w 98 2B 45 # GPI1 = PDMDIN1, GPI2 = PDMDIN2
w 98 2B 67 # GPI3 = PDMDIN3, GPI4 = PDMDIN4
w 98 3C 40 # Enable Channel 1 as PDM input
w 98 41 40 # Enable Channel 2 as PDM input
w 98 46 40 # Enable Channel 3 as PDM input
w 98 4B 40 # Enable Channel 4 as PDM input
w 98 50 40 # Enable Channel 5 as PDM input
w 98 55 40 # Enable Channel 6 as PDM input
w 98 5A 40 # Enable Channel 7 as PDM input
w 98 5F 40 # Enable Channel 8 as PDM input
w 98 6C 20 # 1 biquad per channel
w 98 73 FF # Enable input channels 1-8
w 98 74 FF # Enable output slots 1-8
w 98 75 E0 # Enable MICBIAS, PLL, and all PDM channels
r 98 76 02 # Read device status

## TAS6511-Q1 Device Setup ##
 ################################################################
w B0 00 00 # Page switching (1st 00) to page 0 (2nd 00)
w B0 7F 00 # Change to book 0
w B0 01 19 # Device reset
w B0 00 00 # Page switching (1st 00) to page 0 (2nd 00)
w B0 7F 00 # Change to book 0
w B0 7D 11 # Enter setup mode (1 of 2)
```

```
w B0 7E FF # Enter setup mode (2 of 2)
w B0 00 01 # Page switching (00) to page 1 (01)
w B0 28 40 # Set DIG deglitch
w B0 57 01 # Enable Isense in Hi-Z
w B0 7D 00 # Exit setup mode (1 of 2)
w B0 7E 00 # Exit setup mode (2 of 2)
w B0 00 00 # Page switching (1st 00) to page 0 (2nd 00)
w B0 21 15 # TDM mode
w B0 23 0C # 32-bit word length
w B0 25 0C # 32-bit word length
w B0 61 05 # Enable SS
w B0 62 08 # SS period from 1/FSS to 8/FSS
w B0 00 00 # Page switching (1st 00) to page 0 (2nd 00)
w B0 03 40 # Set device to play mode
```

3.3 Test Setup

Equipment:

- Audio Precision APx555 Audio Analyzer
- Audio Converters Motherboard (AC-MB)
- Power supply – 5V to 19V, 3A
- 2Ω load

Bench Test Setup:

- PVDD = 14.4V
- 2Ω load

3.4 Test Results

Total Harmonic Distortion + Noise, or THD+N, is the ratio of unwanted distortions and background noise relative to the pure original signal. This can be measured in dBFS or % relative to the input signal. Figure 3-1 shows the THD+N performance across frequency for the PCMD3180-Q1 record path, while Figure 3-2 displays the THD+N performance of the playback path through the TAS6511-Q1.

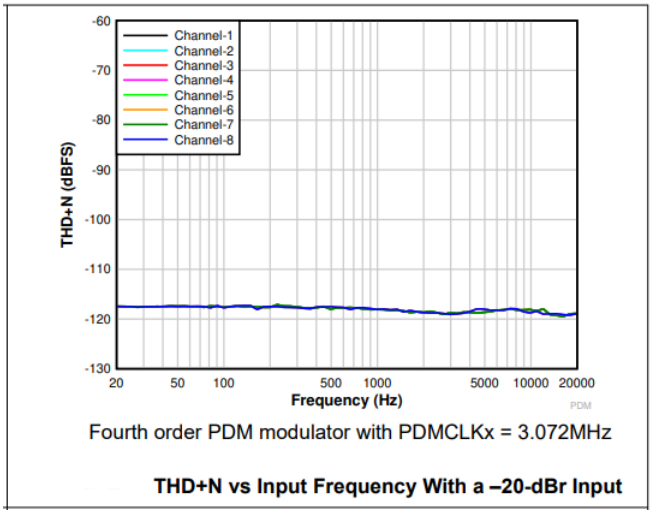


Figure 3-1. Record THD+N vs Input Frequency

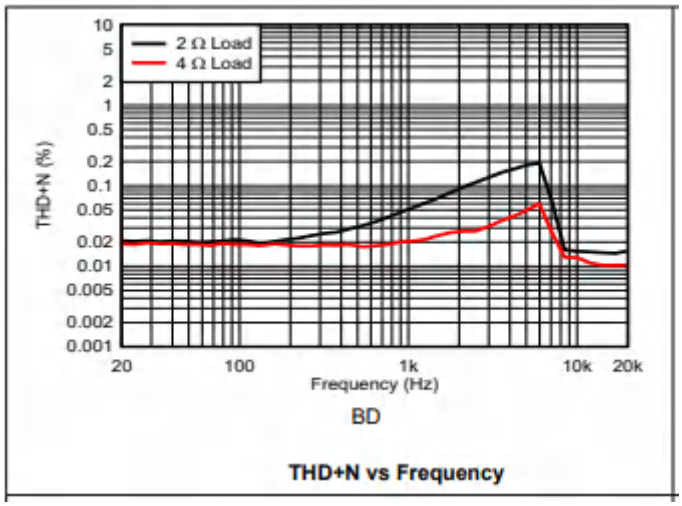


Figure 3-2. Playback THD+N vs Frequency

Figure 3-3 shows an FFT for the PDM inputs on the PCMD3180-Q1 record path. A fourth order PDM modulator is used for this measurement, as that is more common to find among typical PDM digital microphones. However, the PCMD3180-Q1 delivers 10dB better dynamic range performance with a fifth order PDM modulator.

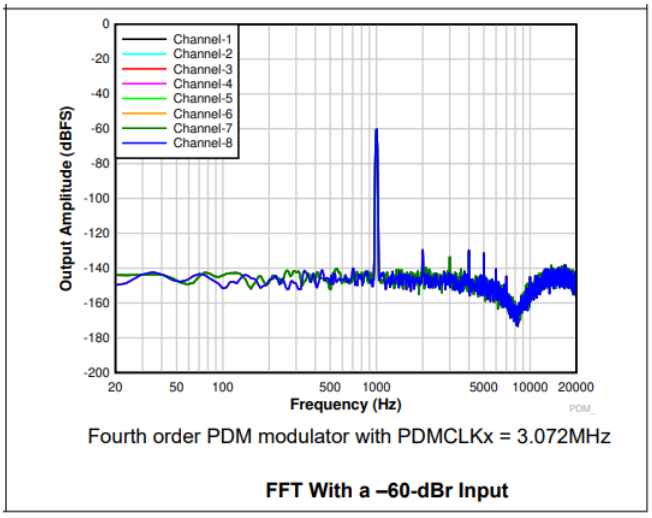


Figure 3-3. PDM FFT

This design can drive up to 50W across a 2Ω load at a 10% THD+N level for a 14.4V PVDD, represented by the dark blue line in Figure 3-4.

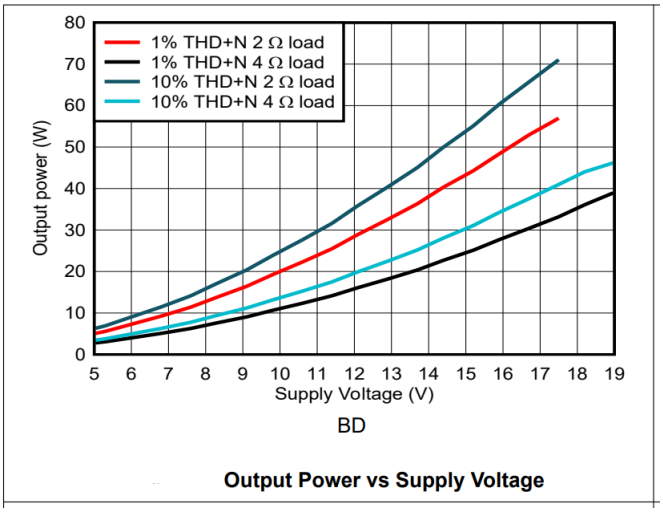


Figure 3-4. Output Power vs PVDD Voltage

Figure 3-5 displays how the playback path THD+N varies across output power.

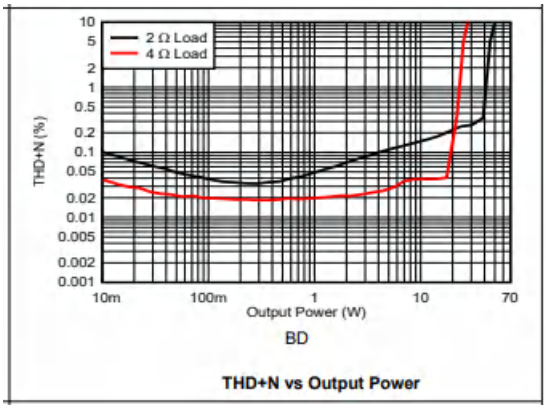


Figure 3-5. Playback THD+N vs Output Power

The Class-D amplifier is designed to increase its efficiency at higher output powers. Figure 3-6 shows the efficiency versus output power for the TIDA-060054.

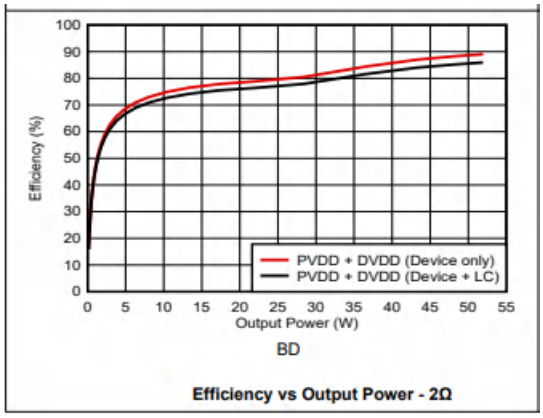


Figure 3-6. Efficiency vs Output Power, 2Ω Load

4 Design and Documentation Support

4.1 Design Files

4.1.1 Schematics

To download the schematics, see the design files at TIDA-060054.

4.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-060054.

4.1.3 PCB Layout Recommendations

The following guidelines can optimize the device performance:

- Connect the thermal pad to ground. Use a via pattern to connect the device thermal pad, which is the area directly under the device, to the ground planes to help dissipate heat from the device.
- The decoupling capacitors for the power supplies must be placed close to the device pins.
- The supply decoupling capacitors must be used ceramic type with low ESR.
- The device internal voltage references must be filtered using external capacitors. Place the filter capacitors near the VREF pin for peak performance.
- Directly short the VREF and MICBIAS external capacitors ground terminal to the AVSS pin without using any vias for this connection trace.
- Place the MICBIAS capacitor (with low equivalent series resistance) close to the device with minimal trace impedance.
- Use ground planes to provide the lowest impedance for power and signal current between the device and the decoupling capacitors. Treat the area directly under the device as a central ground area for the device, and all device grounds must be connected directly to that area.
- The ground connections for the capacitors in the LC filter have a direct path back to the device and the ground return on the same layer of the PCB as the TAS6511-Q1. This direct path allows for improved common mode EMI rejection.
- The decoupling capacitors on PVDD are very close to the device with the ground return close to the ground pins.
- A ground plane on the same side as the device pins helps reduce EMI by providing a very-low loop impedance for the high-frequency switching current. Place multiple ground vias on this plane area to enable a low impedance ground return path and improve thermal dissipation capability.
- The traces from the output pins to the inductors must have the shortest trace possible to allow for the smallest loop of switching currents.

4.2 Tools and Software

4.2.1 Tools

PCMX140Q1EVM-PDK, PCMD3180-Q1 Evaluation Board

TAS6511-Q1-DESIGN, TAS6511-Q1 Technical Documentation Request Form

TAS6511Q1EVM, TAS6511-Q1 Evaluation Board

4.2.2 Software

This reference design utilizes the I2C Master from PurePath Console 3 for I2C programming.

4.3 Documentation Support

1. Texas Instruments, *PCMD3180-Q1, Automotive, eight-channel pulse-density-modulation input to TDM or I²S output converter*, datasheet
2. Texas Instruments, *TAS6511-Q1 50W, 2MHz Digital Input 1-Channel Automotive Heatsink-Free Class-D Audio Amplifier with Current Sense and Real-time Load Diagnostics*, datasheet
3. Texas Instruments, *LMR514x0-Q1 36V, 4A / 5A, Automotive, Synchronous Buck Converter with Low IQ*, datasheet
4. Texas Instruments, *TLV767-Q1 1-A, 16-V Linear Voltage Regulator*, datasheet

4.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search for existing answers or ask your own question to get the quick design help you need.

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5 About the Author

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