Design Guide: TIDA-010990

Pack-Level Electrochemical Impedance Spectroscopy (EIS) Excitation Reference Design With Active Pack Balancing

Description

This reference design features a bidirectional isolated, multi-port dual active bridge (DAB) DC/DC converter designed for battery pack EIS excitation and active pack balancing. The design can generate a sinusoidal current from 0.04Hz to 2000Hz with up to 10A peak-to-peak amplitude. Additionally, the design supports both constant current (CC) and constant voltage (CV) modes to achieve efficient active pack balancing.

Resources

TIDA-010990	Design Folder
TMS320F28P550SG	Product Folder
UCC23525	Product Folder
UCC27834	Product Folder
AMC0311R	Product Folder

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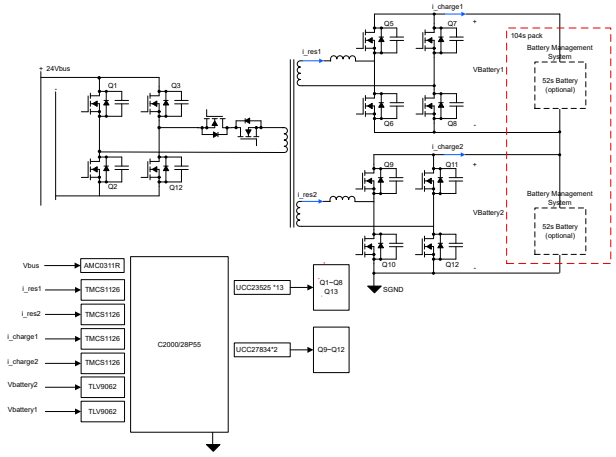
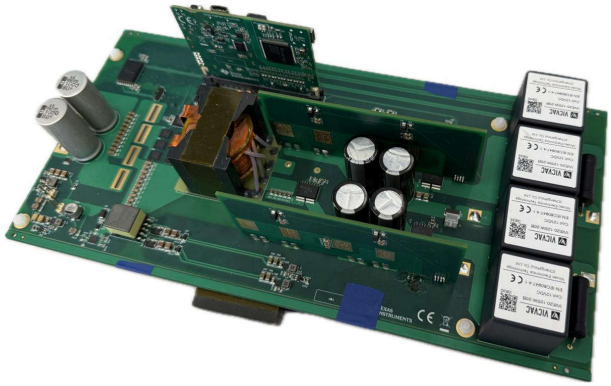
Features

- Bidirectional dual-active-bridge with simple single-phase-shift (SPS) control scheme
- PI + PR control for closed loop control for 0.04hz - 2000hz sinusoidal current
- Supports SPI and CAN communication
- Supports up to 104s battery pack
- TMS320F28P55 controller for digital control
- One rack can do APB and EIS at the same time and have no effect on the other

Applications

- ESS – Battery management system (BMS)





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1 System Description

Energy storage system (ESS) play an important role in renewable energy applications. Depending on the system voltage, capacity and usage, ESS can be divided into three different categories: residential ESS, commercial and industrial ESS, and grid ESS. Commercial and industrial, and grid ESS contain several racks that each contain packs in stack.

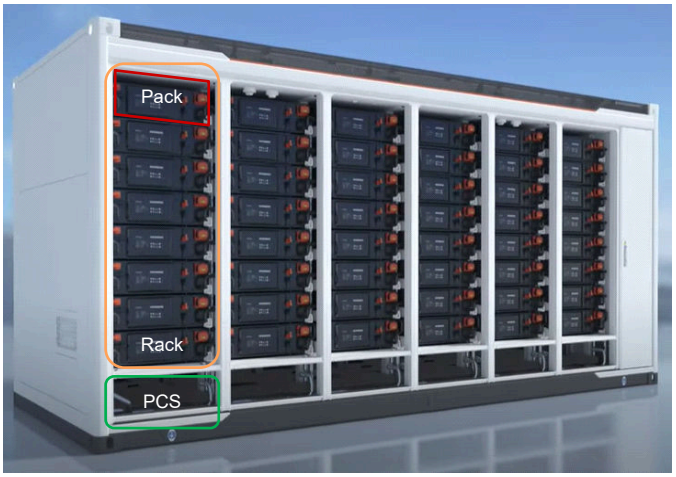

Figure 1-1. Architecture of Grid scale ESS

Figure 1-1 illustrates a typical grid-scale energy storage system (ESS) leveraging a distributed architecture. The system is structurally segmented into three core layers:

- **Battery Pack**: The fundamental energy storage unit, consisting of multiple battery cells connected in series and parallel, managed by an integrated Battery Management System (BMS).
- **Battery Rack**: A vertical cluster formed by stacking multiple battery packs. It aggregates the voltage and capacity to meet high-power grid demands and includes rack-level control and protection circuitry.
- **PCS (Power Conversion System)**: In this highly integrated, distributed topology, a dedicated cluster PCS is deployed directly at the bottom of the rack. This distributed configuration allows for independent charge and discharge management per rack, significantly mitigating the negative impacts of cell capacity mismatch (barrel effect) and maximizing total system energy yield.

The grid-scale high-voltage energy storage system (HV ESS) market faces a critical safety inflection point. As battery cell capacities rapidly escalate from 280Ah to 684Ah, the risk and propagation velocity of thermal runaway have increased exponentially. Legacy management methods rely primarily on temperature-only monitoring. However, due to the massive physical volume of modern large-format cells, internal thermal anomalies suffer from severe thermal lag, making surface-temperature tracking inadequate for early warning.

To overcome this limitation, Electrochemical Impedance Spectroscopy (EIS) has emerged as the definitive technical solution for ultra-fast anomaly detection. By shifting the diagnostic focus from external thermal effects to internal chemical states, EIS measures real-time cell impedance variations across a broad frequency spectrum. This technique bypasses traditional thermal propagation delays entirely, capturing cell degradation and internal short circuits at the absolute earliest microstructural stage to guarantee grid-scale system integrity.

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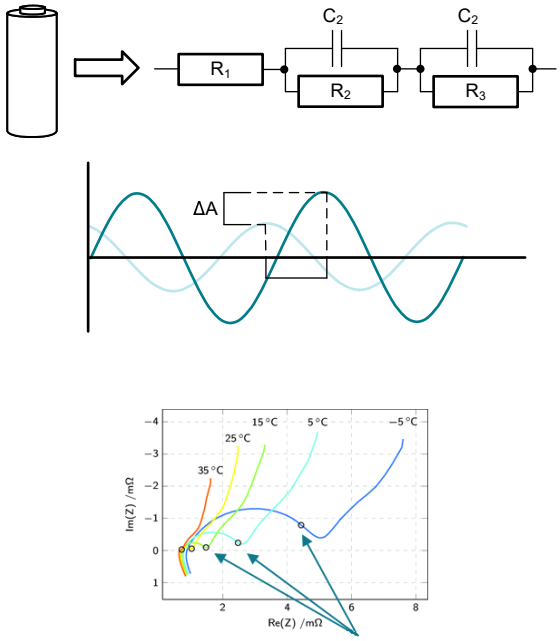

Figure 1-2. Principle of EIS

Figure 1-2 shows the principle of EIS. Mechanically, EIS operates by injecting a controlled, low-amplitude sinusoidal current (or voltage) perturbation into the battery cell across a specific frequency range—typically from tens of millihertz to several kilohertz. The system then synchronously measures the resulting sinusoidal voltage (or current) response. By analyzing the phase shift and amplitude ratio between the excitation signal and the response signal, the complex electrochemical impedance (Z) is calculated at each frequency point.

From an electrochemical standpoint, a battery cell is not a pure resistor, but a complex network of resistances, capacitances, and inductances representing internal physical phenomena (such as ohmic resistance, charge transfer at the electrode interfaces, and ion diffusion). When an internal short circuit or localized overheating begins to develop in a large-format cell, these microstructural properties change instantly. Because these electrical and chemical impedance shifts occur long before the heat can conduct through the thick jelly-roll to cause a surface temperature spike, EIS can detect thermal runaway precursors near-instantaneously.

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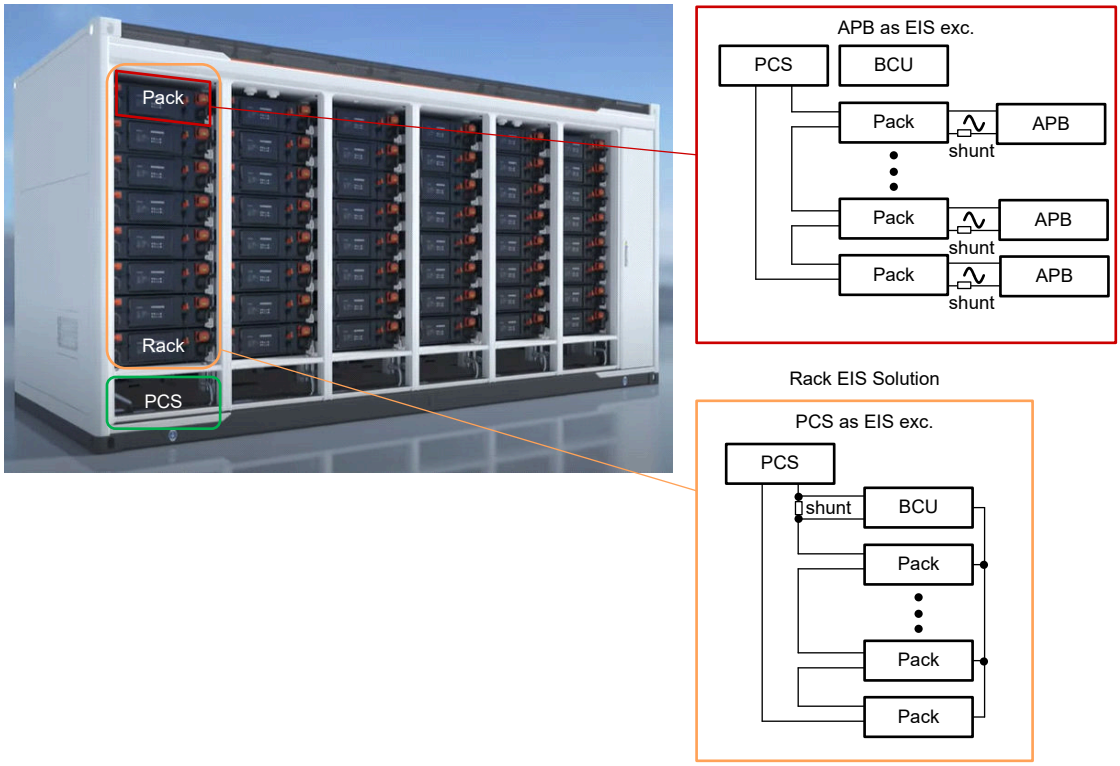

Figure 1-3. Excitation in Grid Scale ESS

To practically deploy EIS in a grid-scale ESS, selecting the appropriate hardware topology to inject the sinusoidal perturbation is critical. As illustrated in Figure 1-3, two primary architecture-level deployment methods exist:

- *Rack-Level EIS Solution (PCS as Excitation Source)*: In this centralized approach, the rack-level Power Conversion System (PCS) directly modulates the entire string current to inject the EIS excitation signal. While this method requires minimal additional hardware per pack, it faces design challenges in resolving fine-grained impedance variations for individual large-format cells due to high common-mode voltage and systemic signal attenuation along the high-voltage bus.
- *Pack-Level EIS Solution (Local Converter as Excitation Source)*: This decentralized approach deploys an independent, localized excitation board—such as the Active Pack Balancing (APB) module—for each individual battery pack. By isolating the excitation source locally, the signal-to-noise ratio (SNR) is significantly improved, enabling precise impedance spectroscopy tailored to the unique aging characteristics of that specific pack.

This reference design focuses exclusively on the Pack-Level EIS design, leveraging a dedicated, highly integrated hardware framework. The standout technical advantage of this localized approach is its ability to repurpose the EIS excitation source as an Active Pack Balancing (APB) converter.

During normal grid operations, this bi-directional, multi-port topology operates in constant-current (CC) or constant-voltage (CV) mode to redistribute energy between mismatched packs, eliminating the classic barrel effect of large-format cells. When safety diagnostics are triggered, the same hardware dynamically transitions to generate the precise 0.04Hz to 2000Hz sinusoidal perturbation required for EIS analysis. This dual-purpose convergence eliminates the need for redundant power electronics, substantially reducing the total bill-of-materials (BOM) cost and physical footprint, while simultaneously maximizing system-level safety and energy efficiency.

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2 System Overview

2.1 Block Diagram

Figure 2-1 shows the block diagram of this multi-port DAB bidirectional isolated DC/DC design. The primary and secondary side needs voltage and current sensing. The TLV9062 device senses the output voltage and the TMCS1126 is used to sense the output current to perform the current loop. The AMC03111R is used to sense the primary voltage to perform voltage loop.

A TMDSCNCD28P55X control card supports the digital control and the UCC23525 and UCC27834 devices are used as gate drivers on both sides. The architecture has three full bridges with SiC in secondary side, Si mos in primary side, DC blocking capacitors, resonant inductors, and one transformer.

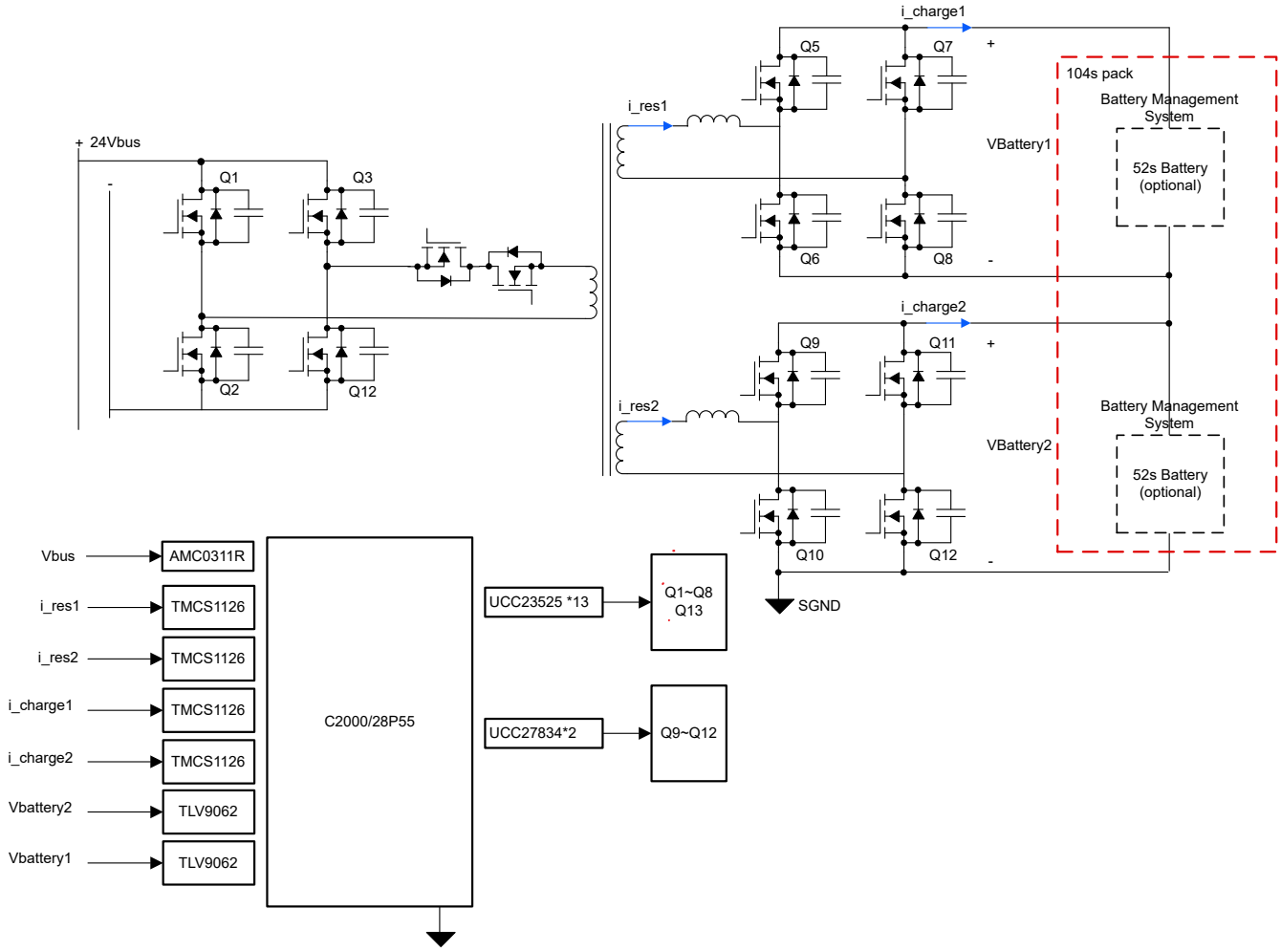

Figure 2-1. TIDA-010990 Block Diagram

2.2 Design Considerations

2.2.1 Design Considerations Introduction

To achieve highly efficient, bidirectional power flow and galvanic isolation for battery diagnostics and balancing, selecting an optimal power electronics topology is critical. Among various isolated bi-directional converters, the Dual Active Bridge (DAB) topology as shown in Figure 2-2 has become the industry standard for high-power energy storage applications. A conventional DAB converter consists of a full-bridge inverter on the primary side, an isolation transformer, and a full-bridge rectifier on the secondary side. By controlling the phase-shift angle between the primary and secondary bridges, the converter can precisely regulate both the direction and the magnitude of power flow. The primary advantages of the conventional DAB include:

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- *Soft-Switching Capability:* It naturally facilitates Zero Voltage Switching (ZVS) across a wide operating range, significantly reducing switching losses and enabling high-frequency operation for a minimized physical footprint.
- *Bi-directional Power Flow:* It seamlessly handles energy transfer in both directions, making it ideal for applications requiring continuous charge and discharge cycles.
- *High Power Density and Isolation:* The high-frequency transformer provides safety-critical galvanic isolation while maintaining an exceptionally high power-to-volume ratio.

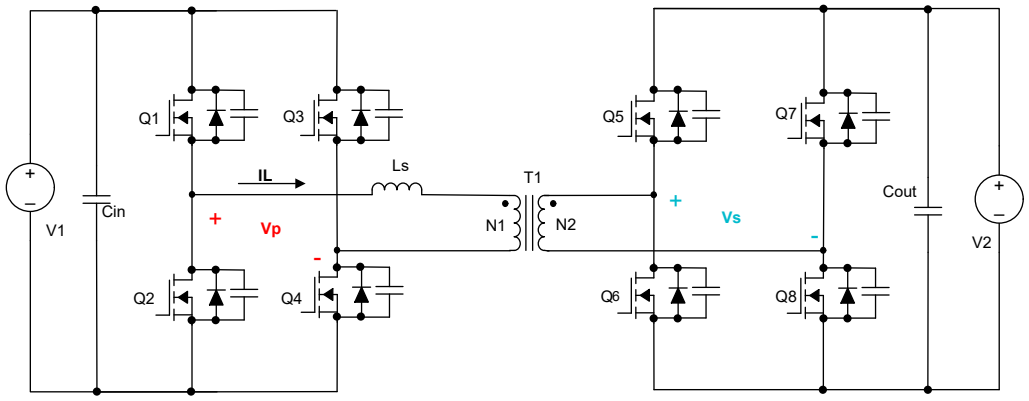

Figure 2-2. Topology of DAB

The Multi-Port DAB topology expands the conventional design by incorporating three or more active bridges linked through a single multi-winding high-frequency transformer, as shown in Figure 2-3. This integration allows a single converter to manage power distribution among multiple independent voltage ports simultaneously. In this design, the multi-port DAB topology serves as the architectural core, connecting the two battery modules, and the auxiliary bus. By controlling the relative phase shifts among all active ports, energy can be dynamically routed between any ports with minimal conversion stages. This advanced topology not only inherits all the soft-switching and high-efficiency benefits of a standard DAB, but also provides the multi-channel flexibility required to generate precise multi-frequency EIS excitation currents while executing active pack-to-pack energy balancing.

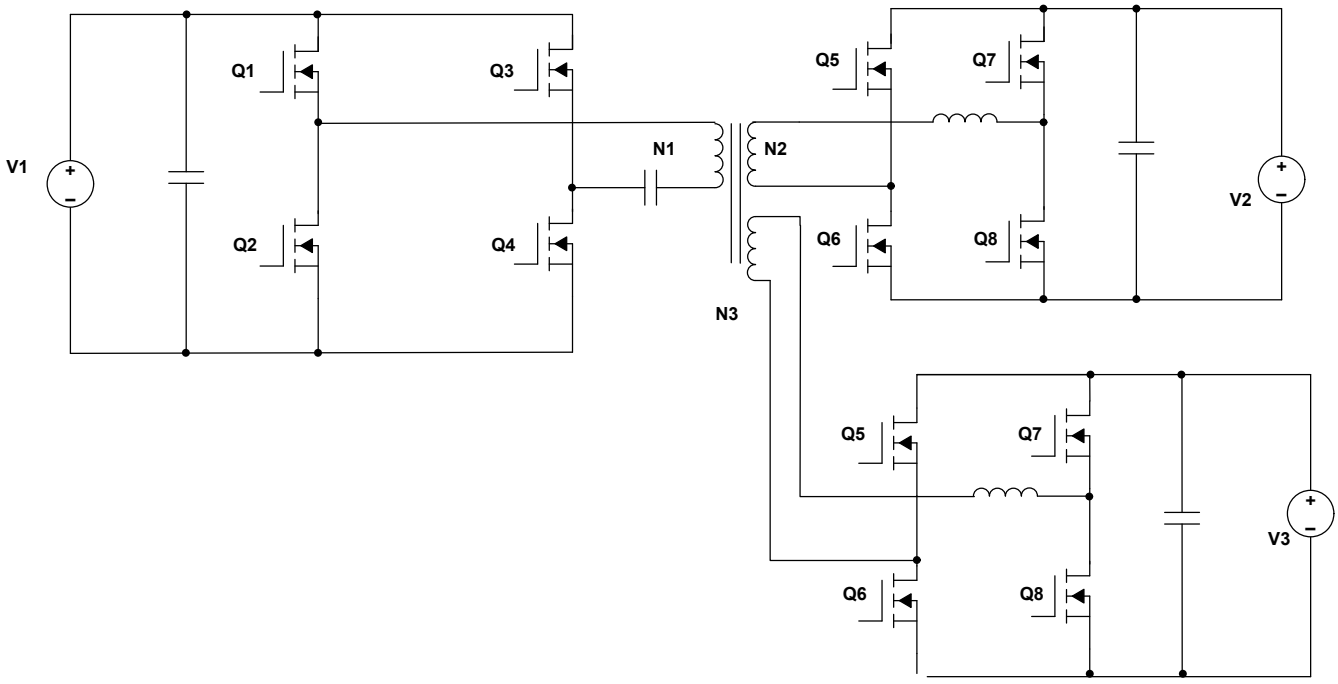

Figure 2-3. Topology of Multi-port DAB

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2.2.2 Basic Operation Principles for DAB

The Single-Phase-Shift (SPS) modulation is the most fundamental and widely adopted control method for the Dual Active Bridge (DAB) converter. Under SPS control, both the primary-side full bridge (Bridge 1) and the secondary-side full bridge (Bridge 2) operate at a fixed 50% duty cycle. The diagonal switch pairs of each bridge (such as Q1/Q4 and Q5/Q8) are turned on and off synchronously .

The core control variable in this scheme is the external phase-shift angle ϕ introduced between the primary-side square-wave voltage (V_p) and the secondary-side square-wave voltage (V_s). This phase shift angle directly regulates the direction and magnitude of the power flow across the high-frequency isolation transformer T1, as shown in Figure 2-4.

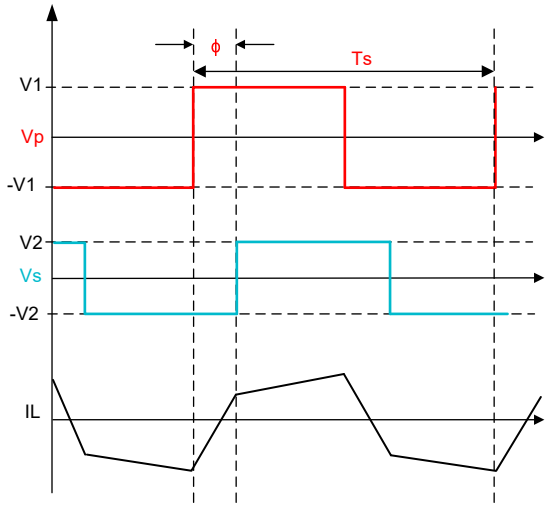

Figure 2-4. Waveforms under SPS control

The average power P_{12} transferred between the two bridges is governed by the energy stored and released in the series leakage inductor L_s, which can be mathematically expressed as :

$$P_{12} = \frac{N \cdot V_1 \cdot V_2 \cdot \phi \cdot (\pi - |\phi|)}{2 \cdot \pi^2 \cdot L_s \cdot f_s} \quad \left(-\pi \le \phi \le \pi\right) \tag{1}$$

Where V_1 is the input DC voltage, V_2 is the output DC voltage, f_s is the switching frequency, and N is the transformer turns ratio ($N = N1/N2$) .

- **Forward Power Mode ($0 \le \phi \le \pi$)**: V_p leads V_s, causing energy to flow from the primary side to the secondary side .
- **Reverse Power Mode ($-\pi \le \phi \le 0$)**: V_p lags V_s, causing energy to seamlessly flow back from the secondary side to the primary side.

The maximum power capability (P_{max}) is strictly limited by the hardware parameters L_s and f_s, and is achieved when the phase-shift angle ϕ equals $\pi/2$:

$$P_{max} = \frac{N \cdot V_1 \cdot V_2}{8 \cdot L_s \cdot f_s} \tag{2}$$

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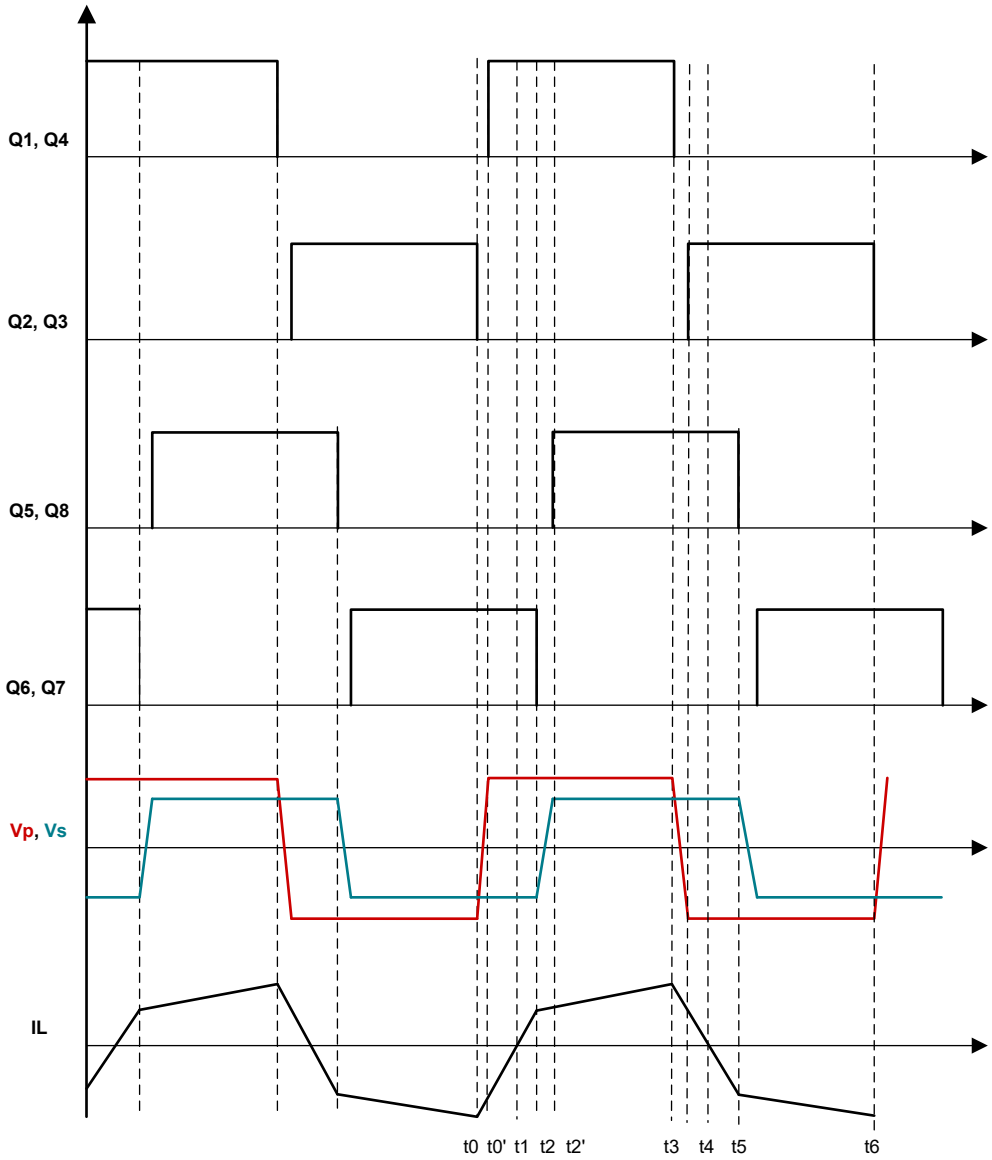

Figure 2-5. Complete Waveforms of PWM and Current Under SPS Control

To minimize switching losses and achieve high total system efficiency, the SPS-DAB relies entirely on the reactive energy stored in the leakage inductor L_s to discharge and charge the MOSFET parasitic output capacitances C_{oss}, thereby facilitating Zero Voltage Switching (ZVS). Figure 2-5 shows complete waveforms of PWM and current . Taking the forward operation mode as a reference, a typical switching cycle progresses through the following key intervals:

- **Interval 1 (t_0 to t_0' - Dead Time Realization,** as shown in Figure 2-6**)**: Prior to t_0 , the switches Q1 and Q4 are turned off . During this dead-time interval, the inductor current I_L must remain negative ($I_L(t_0) < 0$). This negative current forces the energy stored in L_s to discharge the output capacitances of Q1 and Q4 while charging those of Q2 and Q3, creating the necessary zero-voltage condition across Q1 and Q4 prior to their turn-on .

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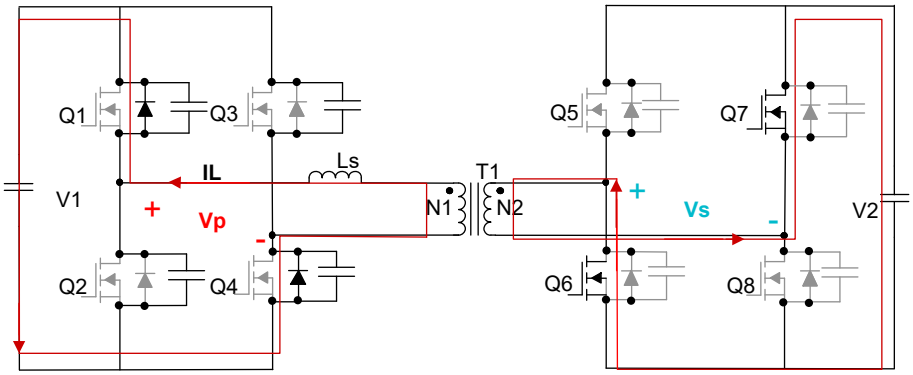

Figure 2-6. DAB converter operating stage during Interval 1

- **Interval 2 (t_0' to t_1 - Primary Channel Conduction,** as shown in Figure 2-7**)**: At t_0' , switches Q1 and Q4 are turned on under a strict zero-voltage condition(Ideal situation). The inductor current passes through the channels of Q1 and Q4, and begins to rise linearly .

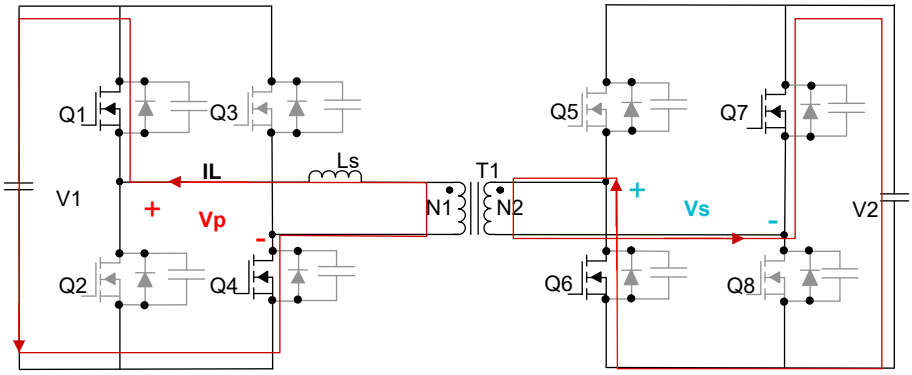

Figure 2-7. DAB converter operating stage during Interval 2

- **Interval 3 (t_1 to t_2 - Current Reversal,** as shown in Figure 2-8**)**: At t_1 , the inductor current crosses zero and switches its direction to positive, continuing its linear progression driven by the voltage difference across the transformer.

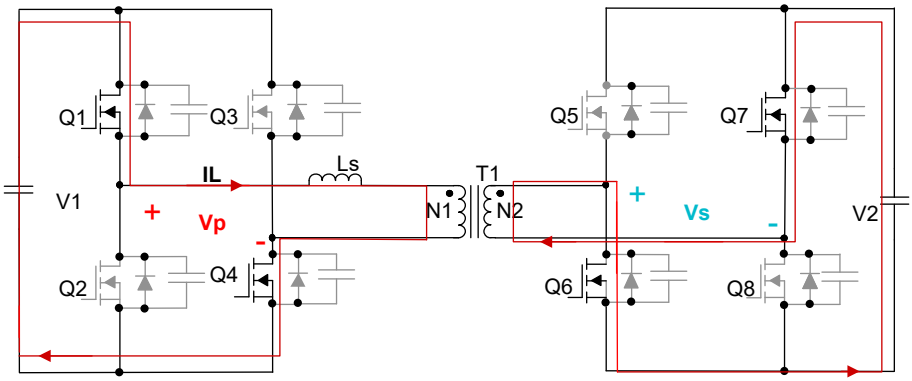

Figure 2-8. DAB Converter Operating Stage During Interval 3

- **Interval 4 (t_2 to t_2' - Secondary Side ZVS Realization,** as shown in Figure 2-9**)**: At t_2 , the secondary side switches Q5 and Q8 are turned off . To enable ZVS for the secondary bridge, the inductor current at this moment must be positive ($I_L(t_2) > 0$). This positive transformer current successfully discharges the output capacitances of Q5 and Q8 while charging Q6 and Q7 during the secondary side dead time.

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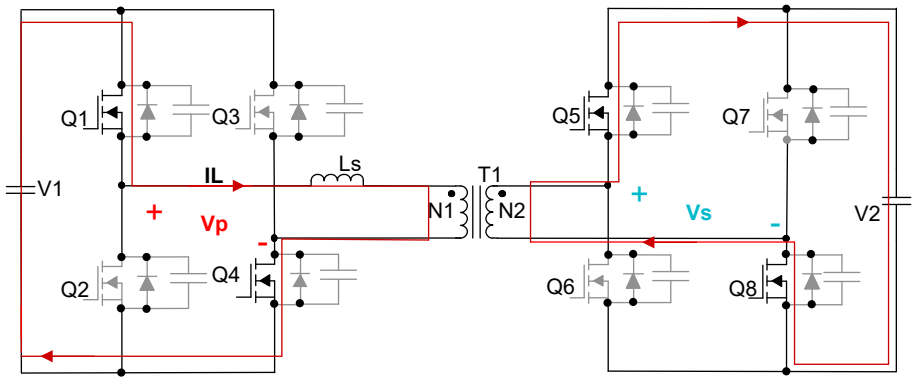

Figure 2-9. DAB Converter Operating Stage During Interval 4

- **Interval 5 (t_2' to t_3) - Full Commutation,** as shown in Figure 2-9**)**: At t_2' , Q5 and Q8 achieve soft turn-on. The current flows naturally through the secondary bridge channels, completing the primary-to-secondary power commutation phase until the next half-cycle repeats the identical process for the remaining FETs from t_3 to t_6 .

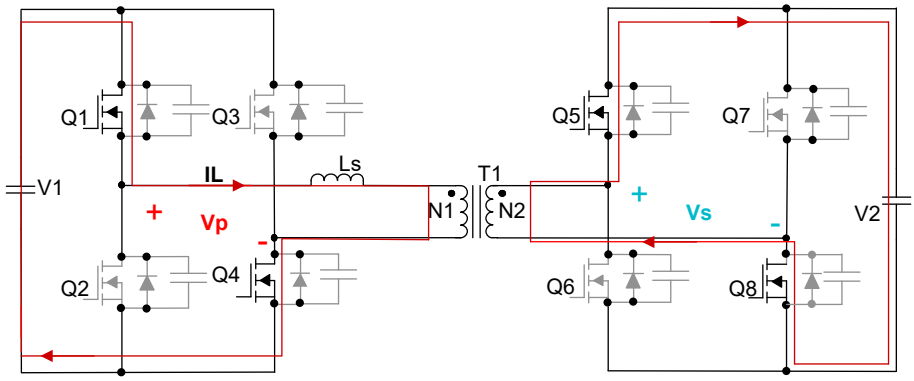

Figure 2-10. DAB Converter Operating Stage During Interval 5

2.3 Highlighted Products

2.3.1 TMS320F28P550SG

The TMS320F28P55x (F28P55x) is a member of the C2000™ real-time microcontroller family of scalable, ultra-low latency devices designed for efficiency in power electronics, including but not limited to: high power density, high switching frequencies, and supporting the use of GaN and SiC technologies.

The real-time control subsystem is based on TI's 32-bit C28x DSP core, which provides 150MHz of signalprocessing performance for floating- or fixed-point code running from either on-chip flash or SRAM. The C28x CPU is further boosted by the Floating-Point Unit (FPU), Trigonometric Math Unit (TMU), and VCRC (Cyclical Redundancy Check) extended instruction sets, speeding up common algorithms key to real-time control systems.

The CLA allows significant offloading of common tasks from the main C28x CPU. The CLA is an independent 32-bit floating-point math accelerator that executes in parallel with the CPU. Additionally, the CLA has its own dedicated memory resources and it can directly access the key peripherals that are required in a typical control system. Support of a subset of ANSI C is standard, as are key features like hardware breakpoints and hardware task-switching.

The TinyEngine™ NPU (Neural-network Processing Unit) can support machine-learning inferencing using pretrained models. Capable of 600–1200MOPS (Mega Operations Per Second) with model support for ARC fault detection or Motor Fault detection, the TinyEngine NPU provides up to 10x NN inferencing cycle improvement versus a SW-only-based implementation. Load and train models with the Edge AI Studio - Model Composer from TI or with the Tiny ML Modelmaker for an advanced set of capabilities. Source code for the C28x is generated by these tools, no manual coding is necessary. For customers who rely on their own AI training framework, TI's

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Neural Network Compiler can help port your AI model to be compatible with many C28x-based MCUs. For those interested in reference solutions, request access to TI's Arc Fault Detection Project or the Motor Bearing Fault Detection Project.

The F28P55x supports up to 1088KB of flash memory divided into four 256KB banks plus one 64KB bank, which enable programming one bank and execution in another bank in parallel. Up to 133KB of on-chip SRAM is also available to supplement the flash memory.

The Live Firmware Update hardware enhancements on F28P55x allow fast context switching from the old firmware to the new firmware to minimize application downtime when updating the device firmware.

High-performance analog blocks are integrated on the F28P55x real-time microcontroller (MCU) and are closely coupled with the processing and PWM units to provide optimal real-time signal chain performance. Twenty-four PWM channels, all supporting frequency-independent resolution modes, enable control of various power stages from a 3-phase inverter to power factor correction and advanced multilevel power topologies.

The inclusion of the Configurable Logic Block (CLB) allows the user to add custom logic and potentially integrate FPGA-like functions into the C2000 real-time MCU.

Interfacing is supported through various industry-standard communication ports (such as SPI, SCI, I2C, PMBus, LIN, and CAN FD) and offers multiple pin-muxing options for optimal signal placement.

2.3.2 TMCS1126

The TMCS1126 is a galvanically isolated Hall-effect current sensor with industry leading isolation and accuracy. An output voltage proportional to the input current is provided with excellent linearity and low drift at all sensitivity options. Precision signal conditioning circuitry with built-in drift compensation is capable of less than 1.4% maximum sensitivity error over temperature 1.4% and lifetime with no system level calibration, or less than 0.9% maximum sensitivity error including both lifetime and temperature drift with a one-time calibration at room temperature.

AC or DC input current flows through an internal conductor generating a magnetic field measured by integrated, on-chip, Hall-effect sensors. Coreless construction eliminates the need for magnetic concentrators. Differential Hall sensors reject interference from stray external magnetic fields. Low conductor resistance increases measurable current ranges up to ±120A while minimizing power loss and easing thermal dissipation requirements. Insulation capable of withstanding 5kVRMS, coupled with a minimum of 8mm creepage and clearance, provides high levels of reliable lifetime reinforced working voltage.

Integrated shielding enables excellent common-mode rejection and transient immunity. Fixed sensitivity allows the device to operate from a single 3V to 5.5V power supply, eliminating ratiometry errors and improving supply noise rejection. TI provides Grade B options at lower-cost.

2.3.3 UCC23525

The UCC23525 driver is an opto-compatible, singlechannel, isolated gate driver for IGBTs, MOSFETs and SiC MOSFETs, with 5A source and 5A sink peak output current and 5kVRMS reinforced isolation rating. The high supply voltage range of 30V allows the use of bipolar supplies to effectively drive IGBTs and SiC power FETs. The UCC23525 can drive both low-side and high-side power FETs. Key features and characteristics bring significant performance and reliability upgrades over standard opto-coupler based gate drivers while maintaining pin-to-pin compatibility in both schematic and layout design.

Performance highlights include high common-mode transient immunity (CMTI), low propagation delay, and small pulse width distortion. Tight process control results in small part-to-part skew. The input stage is an emulated diode (e-diode) which means long term reliability and excellent aging characteristics compared to traditional LEDs found in optocoupler gate drivers. The UCC23525 is offered in a stretched SO-6 package, supporting 5KVRMS reinforced isolation rating. The stretched SO-6 package has >8.5mm creepage and clearance, and a mold compound from material group I which has a comparative tracking index (CTI) >600V.

The high performance and reliability of the UCC23525 makes the device ideal for use in all types of motor drives, solar inverters, industrial power supplies, and appliances. The higher operating temperature opens up opportunities for applications not previously able to be supported by traditional optocouplers.

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2.3.4 UCC27834

The UCC278X4 is a 230V half-bridge gate driver with 3.5A source, 4A sink current, targeted to drive power MOSFETs. The device consists of one ground referenced channel (LO) and one floating channel (HO) which is designed to drive half-bridge configured MOSFETs operating with bootstrap power supplies. The device features fast propagation delays and excellent delay matching between both channels. The UCC278X4 allows a wide VDD operating voltage of 8.5V to 20V to support a wider range of gate voltage drive, as well as UVLO protection for both the lowside (VDD) and the high-side (HB) bias supplies. The UCC27834 includes an interlock function option to prevent both outputs from being turned on simultaneously.

The device features robust drive with excellent noise and transient immunity including high dV/dt tolerance (100V/ns), and wide negative transient safe operating area (NTSOA) on the switch node (HS). The UCC278X4 is available in the SOIC-8 pin package and is rated to operate from –40°C to 150°C.

2.3.5 AMC03111R

The AMC0x11R is a precision, galvanically isolated amplifier with a 2.25V, high impedance input and single-ended ratiometric output. The high-impedance input is optimized for connection to a high-impedance resistive divider or other voltage signal source with high output resistance.

The isolation barrier separates parts of the system that operate on different common-mode voltage levels. The isolation barrier is highly resistant to magnetic interference. This barrier is certified to provide reinforced isolation up to 5kVRMS (DWV package) and basic isolation up to 3kVRMS (D package) (60s).

The AMC0x11R outputs a single-ended signal proportional to the input voltage. The full-scale output is set by the voltage applied to the REFIN pin. The output of the AMC0x11R is designed to connect directly to the input of an ADC. Connect REFIN to the same reference voltage as the ADC to match the dynamic input voltage range of the ADC.

The AMC0x11R devices come in 8-pin, wide- and narrow-body SOIC packages, and are fully specified over the temperature range from –40°C to +125°C.

2.4 System Design Theory

2.4.1 Switching Frequency and Transformer Ratio Design

Figure 2-11 shows the schematic of TIDA-010990.

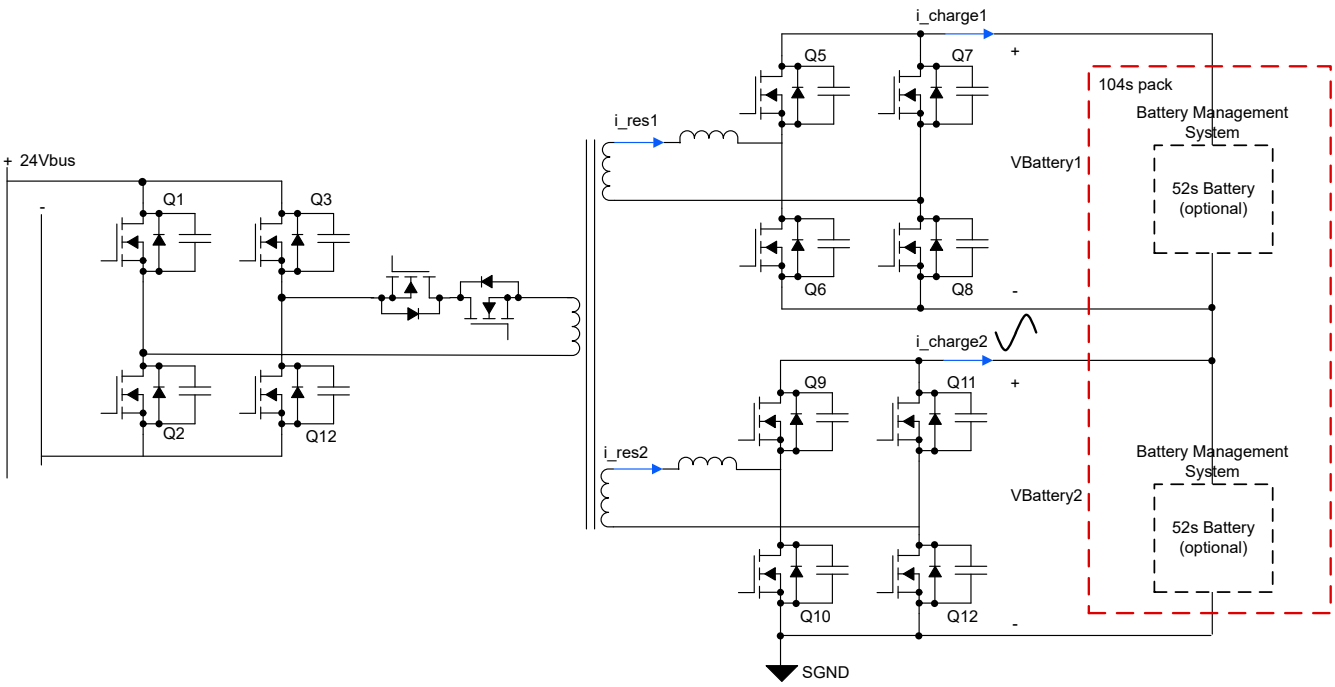

Figure 2-11. The Schematic of TIDA-010990

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The switching frequency (f_s) represents a critical trade-off between the target EIS excitation bandwidth and the converter's thermal efficiency. To support the maximum required EIS excitation frequency of 2kHz with sufficient control resolution and low signal distortion, the switching frequency must be significantly higher than the excitation spectrum.

Simultaneously, to minimize switching losses and magnetic core losses within the localized pack-level enclosure, 25kHz is selected as the optimal switching frequency.

To minimize reactive power and achieve optimized soft-switching (ZVS) performance under standard active balancing conditions, the transformer turns ratio should align with the nominal voltage conversion ratio among the ports. As illustrated in the schematic (Figure 2-11), the primary-side DC bus voltage V_{bus} is stabilized at 24V, while each secondary-side port connects to a 52s battery pack. Assuming a nominal lithium-ion cell voltage of 3.3V, the nominal port voltage for both $V_{battery1}$ and $V_{battery2}$ is approximately 171.6V (3.3V x 52). Therefore, the transformer turns ratio among the primary winding (N1) and the two identical secondary windings (N2, N3) is designated as:

$$N_1 : N_2 : N_3 = 1 : 7.15 : 7.15 \tag{3}$$

2.4.2 Resonant Inductance Design

The series leakage inductance serves as the core energy-buffering element that governs the maximum power transfer capability under SPS modulation. This component is optimized based on the extreme operating conditions required during EIS diagnostic mode.

When the primary switch Q13 is disabled, the primary port is completely isolated. The topology functions as a symmetrical secondary-to-secondary DAB converter, dynamically shuffling energy between winding N2 and winding N3 to inject a sinusoidal current with a 5A peak amplitude. According to the ideal SPS power equation, the target total loop inductance required at nominal voltage (171.6V) and an optimized phase-shift angle ($\phi = \pi/4$) is approximately 128 μH :

$$L_{total\_theoretical} = \frac{V_1 \cdot V_2 \cdot \phi(\pi - \phi)}{2\pi^2 \cdot f_s \cdot P_{max}} \tag{4}$$

To mathematically satisfy this condition while ensuring a symmetrical, modular hardware layout, this design split-allocates the loop inductance across both secondary ports. Two identical external resonant inductors *i*_res1 and *i*_res2 are deployed, each selected with a nominal value of **50** μH . This provides a total initial loop inductance of approximately 100 μH (excluding transformer parasitic leakage), perfectly positioning the nominal control trajectory around the highly efficient $45°$ phase-shift window.

2.4.3 DC-Blocking Capacitor Design

In a DAB converter, any minor volt-second asymmetry caused by gate-driver propagation delays or component mismatches can inject a DC bias current into the high-frequency transformer, leading to catastrophic core saturation. Therefore, a DC-blocking capacitor C_b must be placed in series with the transformer windings and resonant inductors on the high-frequency AC side.

The selection of C_b is strictly dictated by the 25 kHz switching frequency and must satisfy the following two hardware constraints:

1. **Impedance Dominance Prevention**: To ensure that the power transfer capability remains strictly controlled by the resonant inductors ($L_{total} = 100 \ \ \mu\text{H}$), the impedance of the blocking capacitor at the switching frequency ($f_s = 25\ \text{kHz}$) must be significantly smaller than that of the inductors (typically less than 10%). This ensures that C_b does not interfere with the standard SPS power equations:

$$X_{Cb} = \frac{1}{2\pi \cdot f_s \cdot C_b} \leq 10\,\% \cdot \left(2\pi \cdot f_s \cdot L_{total}\right) \tag{5}$$

2. **Resonant Frequency Placement**: The unintended series resonant frequency (f_r) formed by C_b and L_{total} must be placed safely below the switching frequency to avoid severe voltage overshoots and control instability:

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$$f_r = \frac{1}{2\pi\sqrt{L_{total} \cdot C_b}} \ll f_s \quad (6)$$

Based on these criteria for a 25kHz operational frequency and 100 μH loop inductance, the optimal capacitance for C_b is calculated to be in the **range of 2 μF to 5 μF ,** choose 10 μF . High-frequency, low-ESR **polypropylene film capacitors** or multi-layer ceramic capacitors (MLCCs) with a high AC RMS current rating must be selected to withstand the continuous high-frequency switching stress without thermal degradation.

2.4.4 Hardware Design Theory

This section discuss hardware-related selection, and schematic PCB design for example.

2.4.4.1 Power Stage

Figure 2-12 shows the power stage of the bidirectional isolated multi-port DAB converter. The primary side consists of 60V, 2.2mΩ, N-channel, power MOSFET CSD18540Q5B to block a DC voltage of 24V, and the secondary side consists of 400V, 25.4mΩ, SiC IMBG40R025M2H to block DC voltage of 200V.

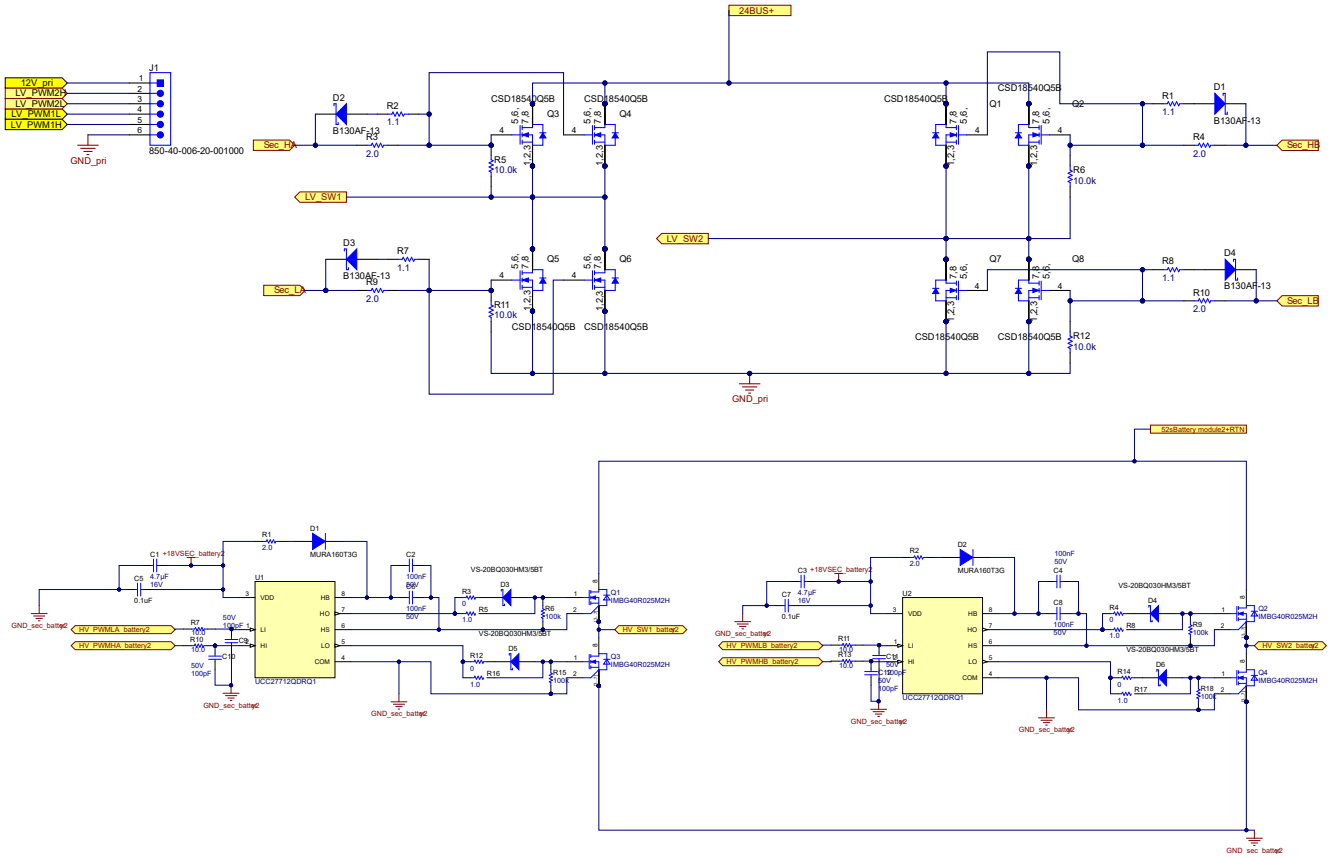

Figure 2-12. Power Stage

2.4.4.2 Sensing

This design needs to sense input voltage to perform a constant voltage loop when in reverse mode. The primary DC voltage needs to be sensed.

Figure 2-13 shows the primary voltage sensing circuit. The maximum primary bus voltage to be sensed is 30V, and MCU is put on secondary side. Therefore, choose AMC0311R to sense the primary side DC voltage.

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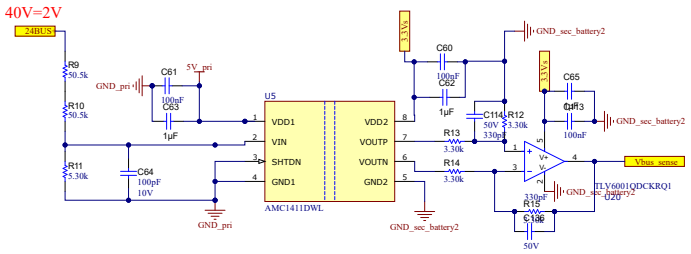

Figure 2-13. Primary Voltage Sensing Circuit

Figure 2-13 shows the secondary voltage sensing circuit. The maximum secondary battery voltage to be sensed is 200V.

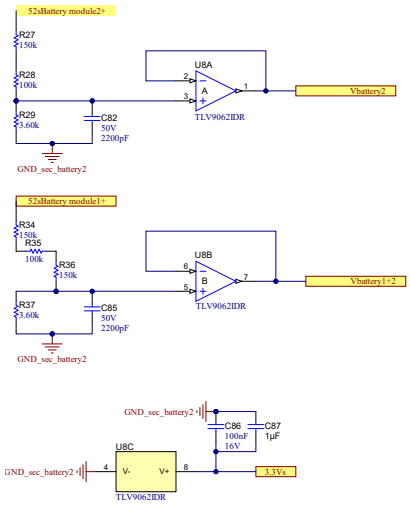

Figure 2-14. Secondary Voltage Sensing Circuit

This design needs to sense onput voltage to perform current loop when in EIS mode. The secondary current needs to be sensed. Figure 2-14 shows the secondary current sensing. Choose TMCS1126B4 to sense upto 10A output current. Also Figure 2-15 shows the resonant tank current, it is used for protection, also choose TMCS1126B4.

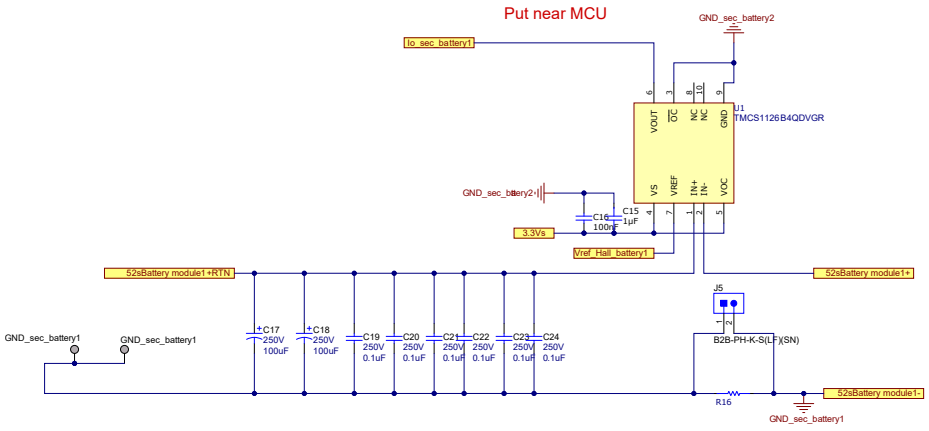

Figure 2-15. Secondary Current Sensing Circuit

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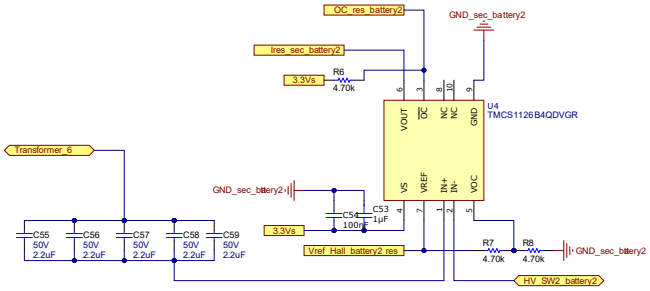

Figure 2-16. Resonant Tank Current Sensing Circuit

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3 Hardware, Software, Testing Requirements, and Test Results

3.1 Hardware Requirements

The following hardware is required for this reference design:

- One TIDA-010990 power board
- One TMDSCNCD28P55 control card
- USB Type-C® cable
- Laptop

The following test equipment is needed to power and evaluate the DUT:

- Bidirectional DC source capable of delivering voltage between 0V–200V at required current
- Power analyzer
- Auxiliary power supply
- Oscilloscope
- Isolated voltage probes and current probes

3.2 Test Setup

To test the efficiency of this reference design, use the setup shown in Figure 3-1.

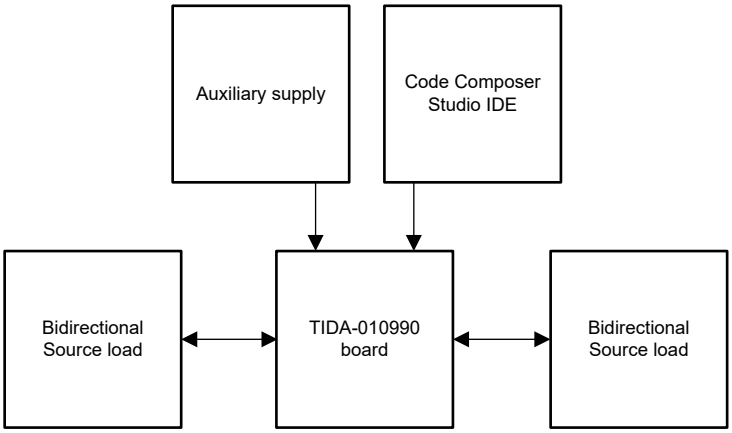

Figure 3-1. Test Setup

- As a bidirectional converter, both the input and output need to connect to bidirectional source load, where the bidirectional source and load need to support 200V 5A.
- Auxiliary power supply to provide one channel for 18V, 1A.
- One TMDSCNCD28P55 control card
- Power analyzer
- Oscilloscope with isolated probes for voltage and current

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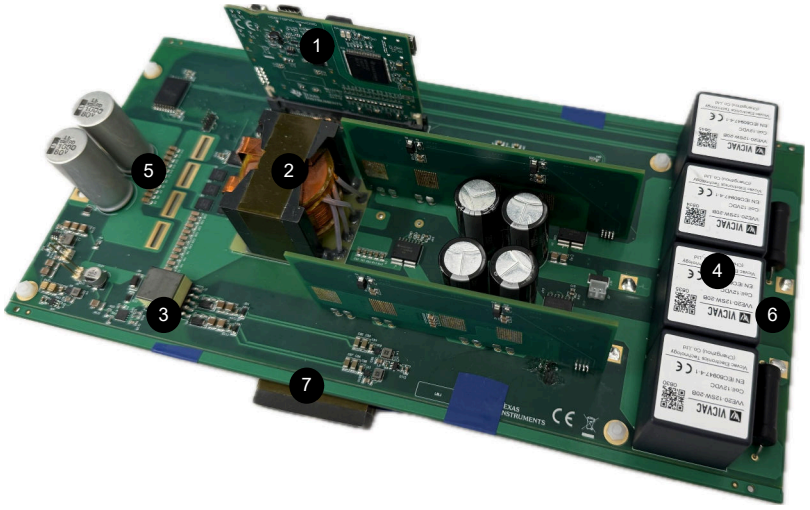

1. Control card
2. Transformer
3. Auxiliary supply
4. Relay
5. Input stage
6. Output stage
7. Resonant inductance

Figure 3-2. TIDA-010990 Board

3.3 Test Results

Below shows test results for 1hz, 50hz, 500hz, 1000hz, 1600hz, 2000hz EIS excitation current. The red is EIS excitation current, and the green is the resonant current.

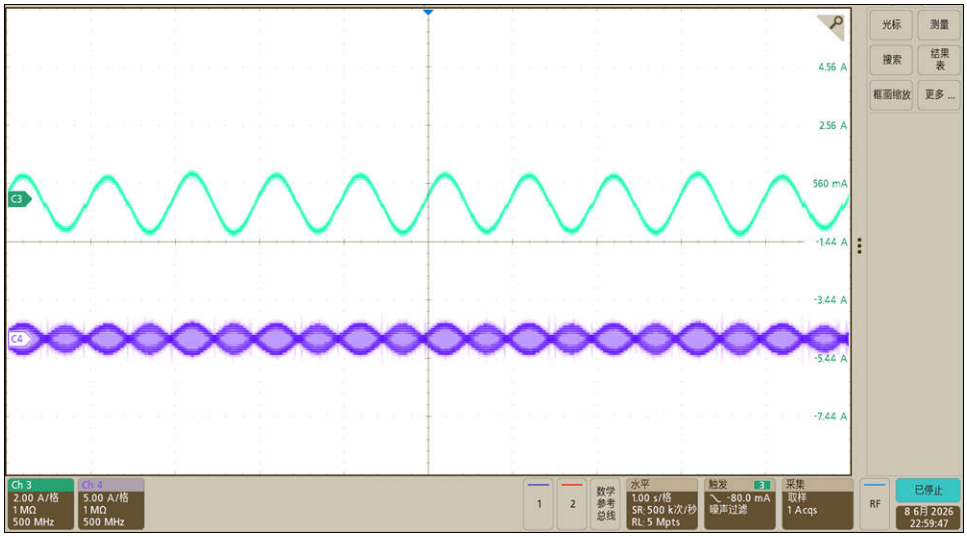

Figure 3-3. 1HZ test waveforms

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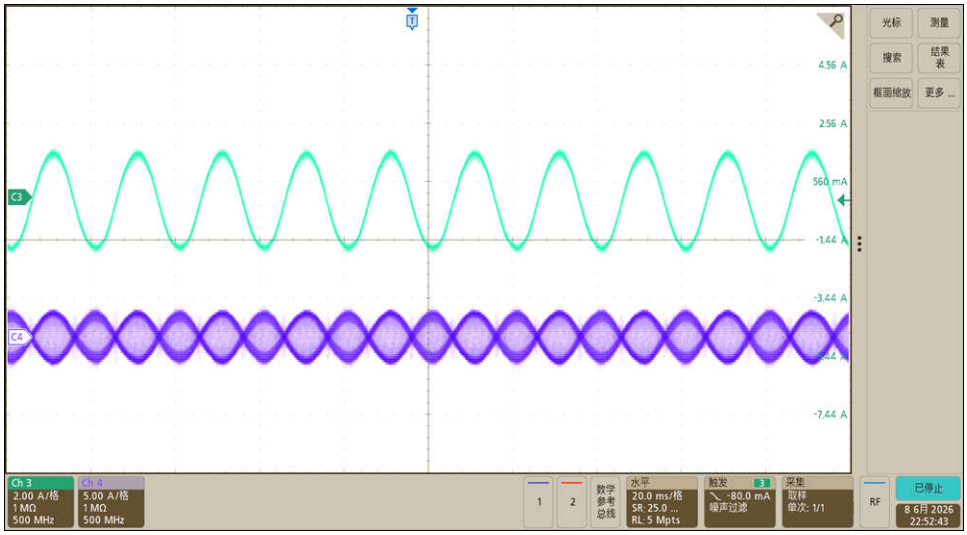

Figure 3-4. 50HZ test waveforms

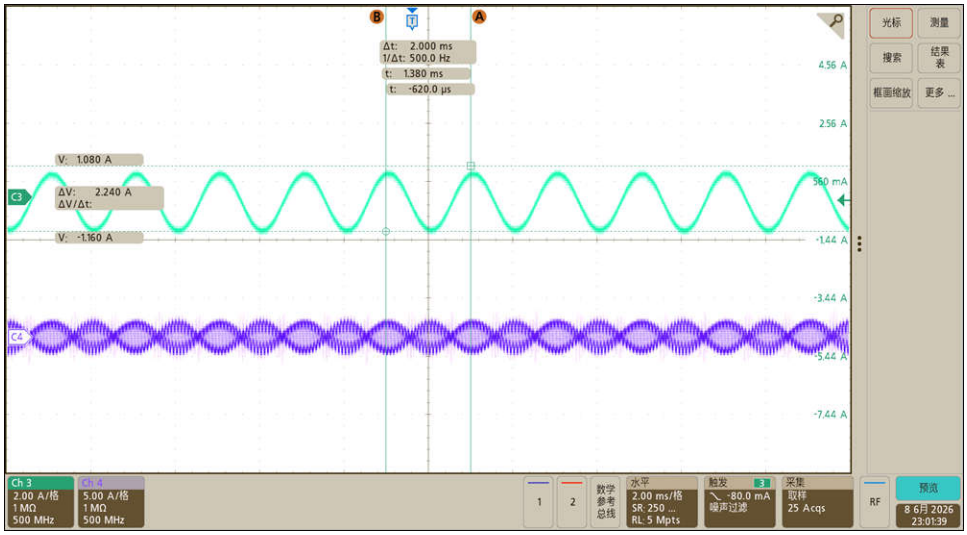

Figure 3-5. 500HZ test waveforms

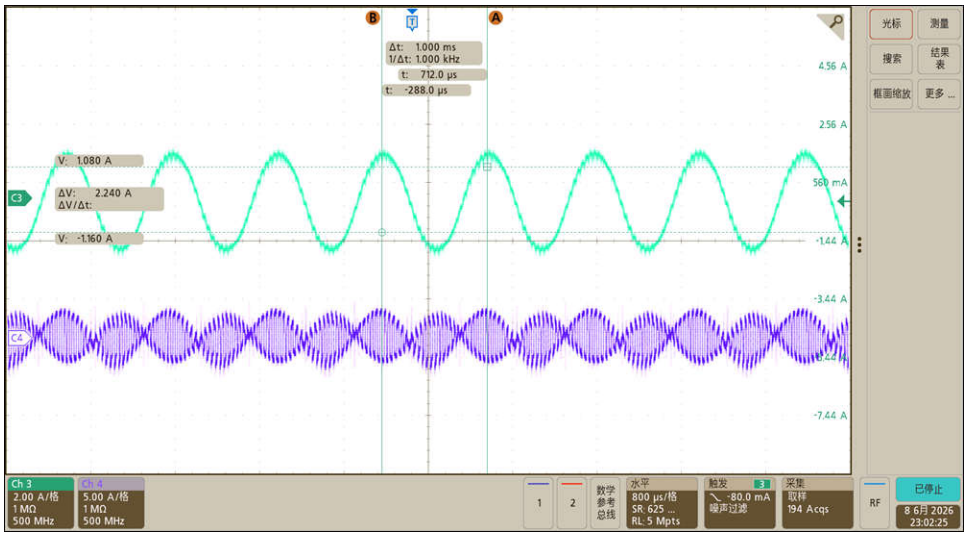

Figure 3-6. 1000HZ test waveforms

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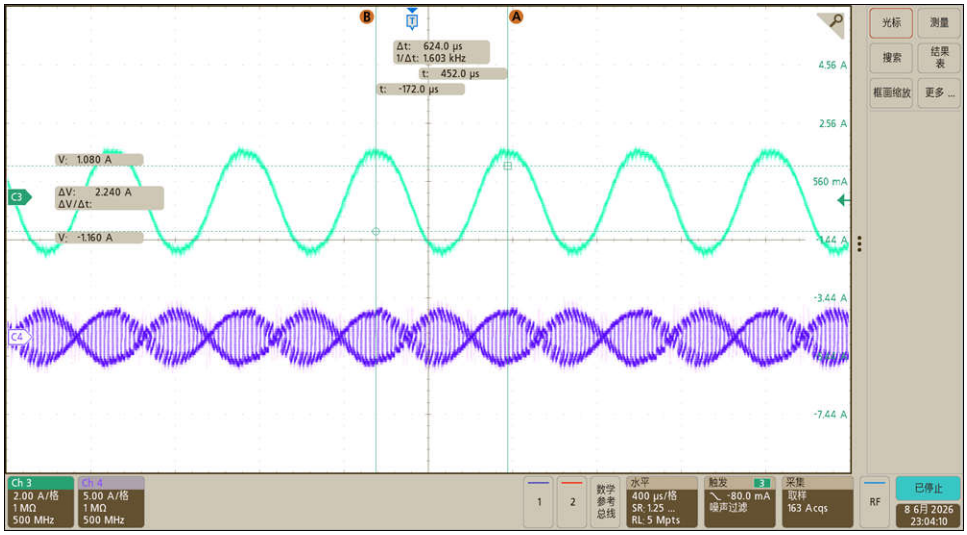

Figure 3-7. 1600HZ Test Waveforms

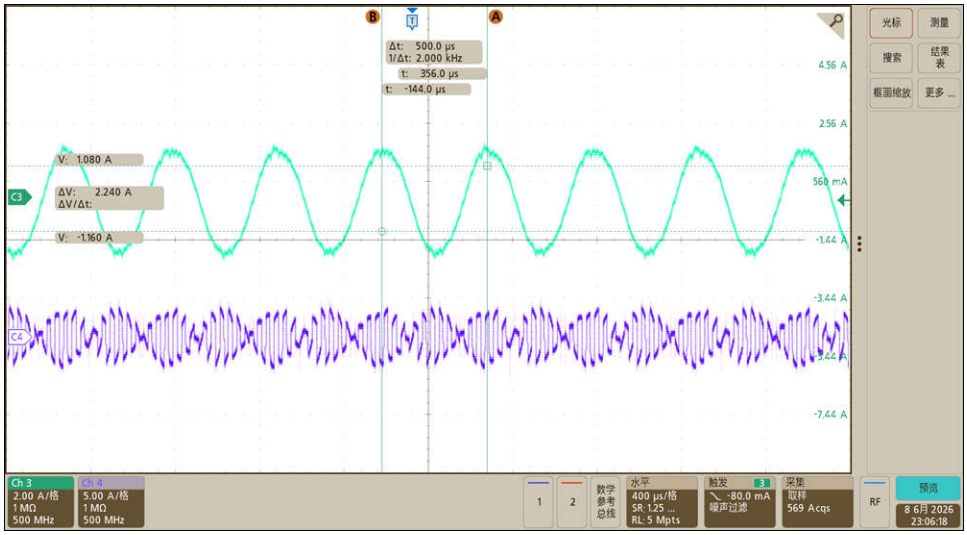

Figure 3-8. 2000HZ Test Waveforms

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4 Design and Documentation Support

4.1 Design Files

4.1.1 Schematics

To download the schematics, see the design files at TIDA-010990.

4.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-010990.

4.2 Tools and Software

Tools

C2000Ware	C2000Ware is a cohesive set of software and documentation created to minimize development time. C2000Ware includes device-specific drivers, libraries, and peripheral examples.

Software

Concise Description	Description

4.3 Documentation Support

1. Texas Instruments, *TMS320F28P55x Real-Time Microcontrollers* data sheet
2. Texas Instruments, *UCC23525 5A Source, 5A Sink, 5kVRMS Reinforced, Opto-Compatible, Single-Channel Isolated Gate Drive* data sheet
3. Texas Instruments, *UCC278X4 High-Speed, 230V Half-Bridge Driver with 3.5A, 4A Drive Strength and up to 100V/ns Noise Immunity* data sheet
4. Texas Instruments, *Dual Active Bridge Topology Overview* power supply design seminar

4.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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5 About the Author

WILL TAI is working as systems engineer focusing on Energy Storage System in Grid Infrastructure, where he is responsible for power conversion system and cell balance and pack balance designs. Before joining TI, he received his master's degree in electrical engineering at the University for Nanjing University of Aeronautics and Astronautics.

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