

DCA2000EVM

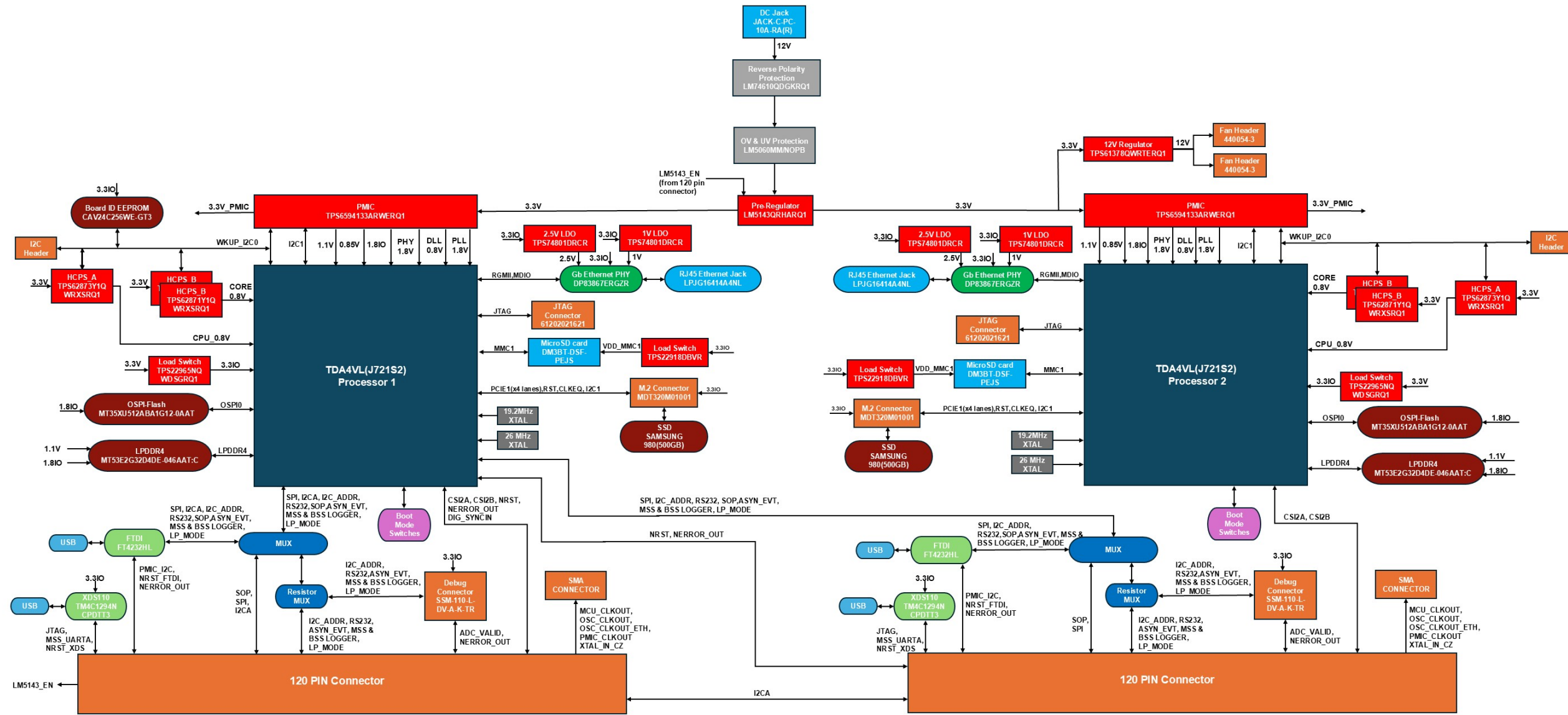
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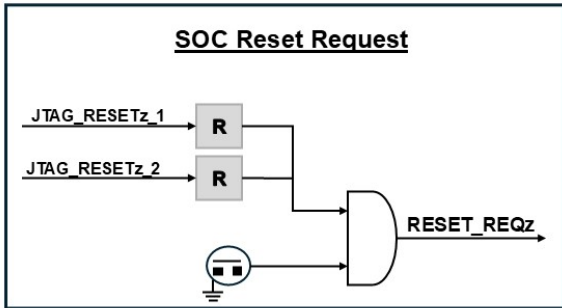
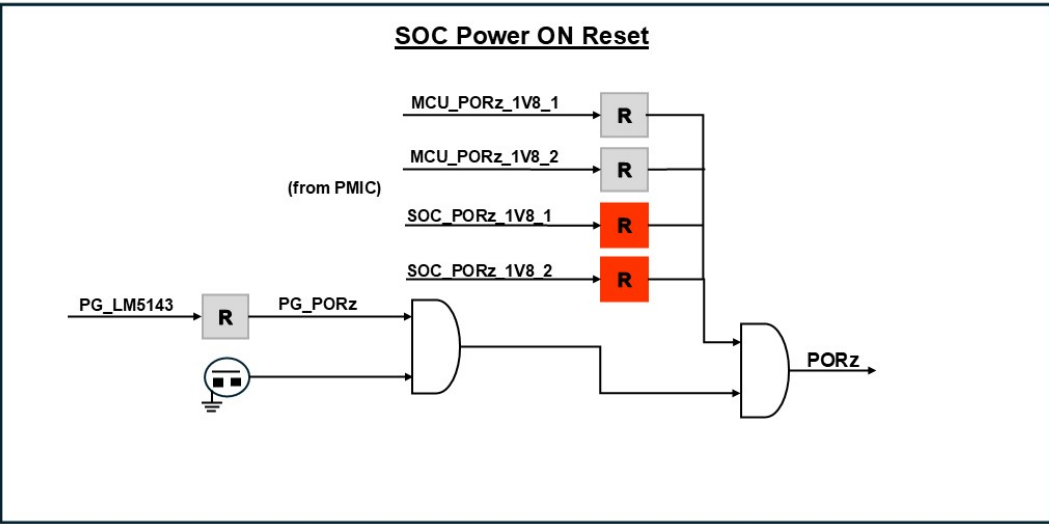
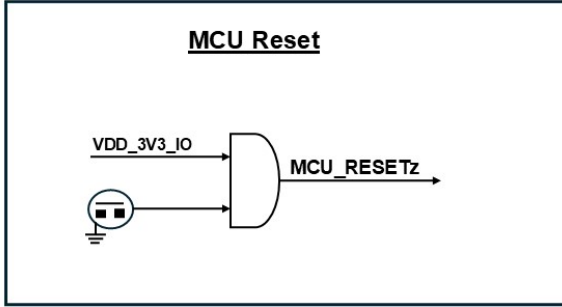
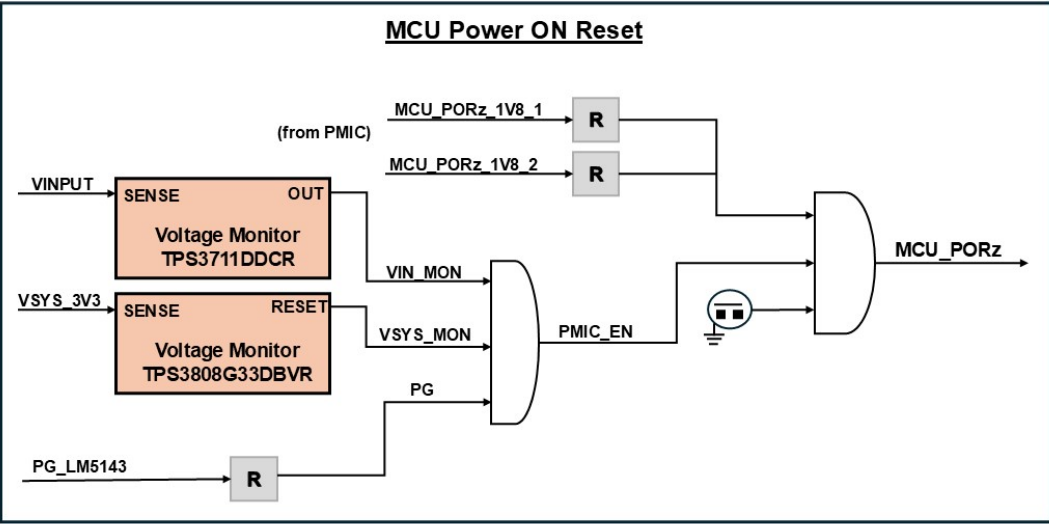
REVISION HISTORY

Rev	ECN#	Approved Date	Approved By	Notes
Rev A	01	13-09-2024		Initial Draft

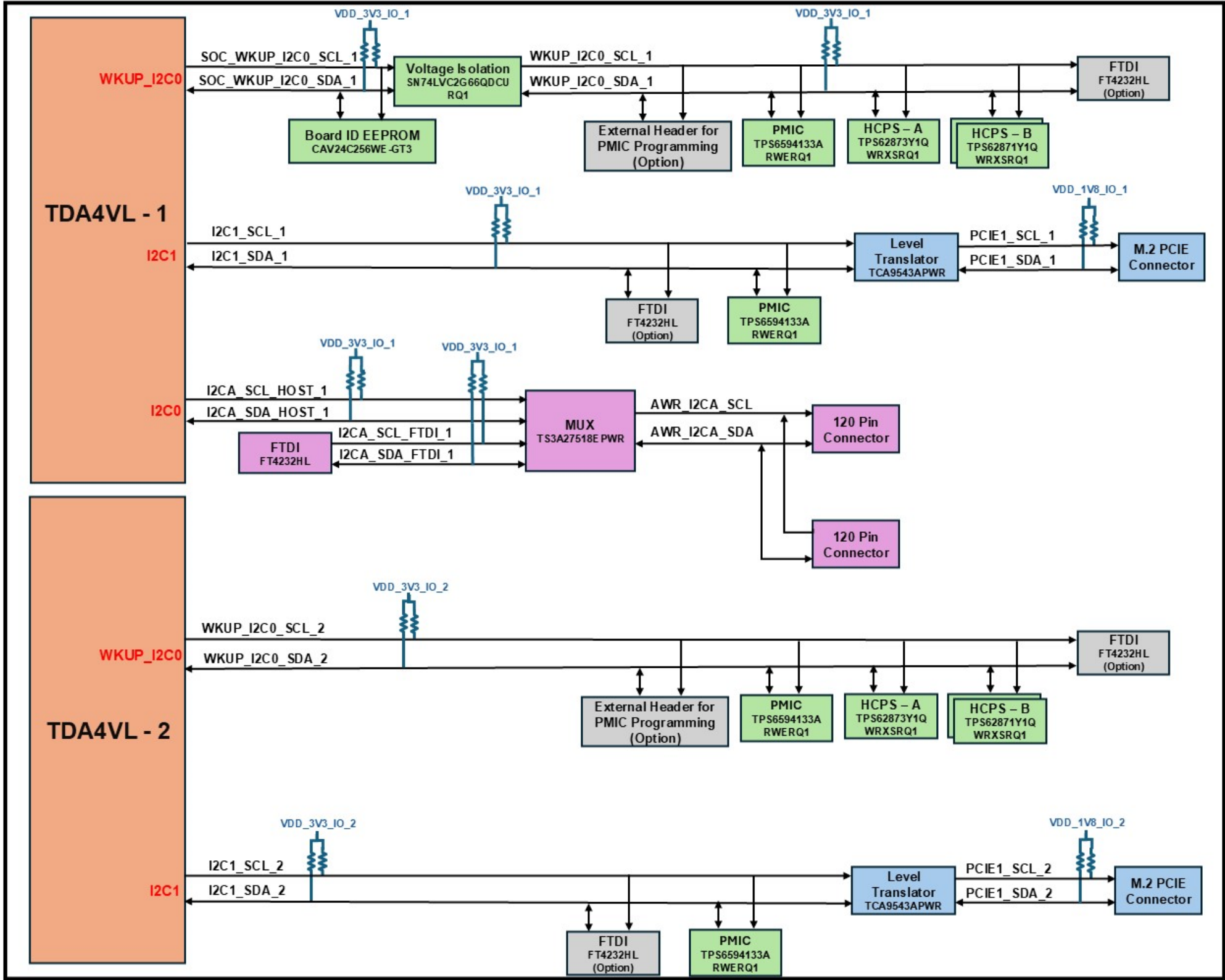
BLOCK DIAGRAM



# RESET ARCHITECTURE



I2C TREE



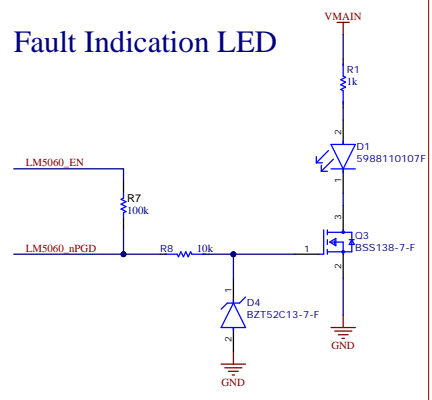


I2C TABLE

TDA4VL port Mapping	Reference Designator	Interface Name	Part#	Address
Processor - 1				
SOC_WKUP_I2C0	U18	Board ID EEPROM	CAV24C256WE-GT3	0X50
WKUP_I2C0	U5	PMIC	TPS6594133ARWERQ1	0X48, 0X49, 0X4A, 0X4B
	J4	External I2C Header	M22-2510305	
	U9	HCPS-A	TPS62873Y1QWRXSRQ1	0x40
	U10,U11	HCPS-B	TPS62871Y1QWRXSRQ1	0x43
I2C1	U5	PMIC	TPS6594133ARWERQ1	0X12
	U66	Level Translator	TCA9543APWR	0X71
	J10	M.2 PCIe Connector	MDT320M01001	
Processor - 2				
WKUP_I2C0	U7	PMIC	TPS6594133ARWERQ1	0X48, 0X49, 0X4A, 0X4B
	J5	External I2C Header	M22-2510305	
	U12	HCPS-A	TPS62873Y1QWRXSRQ1	0x40
	U13,U14	HCPS-B	TPS62871Y1QWRXSRQ1	0x43
I2C1	U7	PMIC	TPS6594133ARWERQ1	0X12
	U67	Level Translator	TCA9543APWR	0X71
	J11	M.2 PCIe Connector	MDT320M01001	

[illegible]

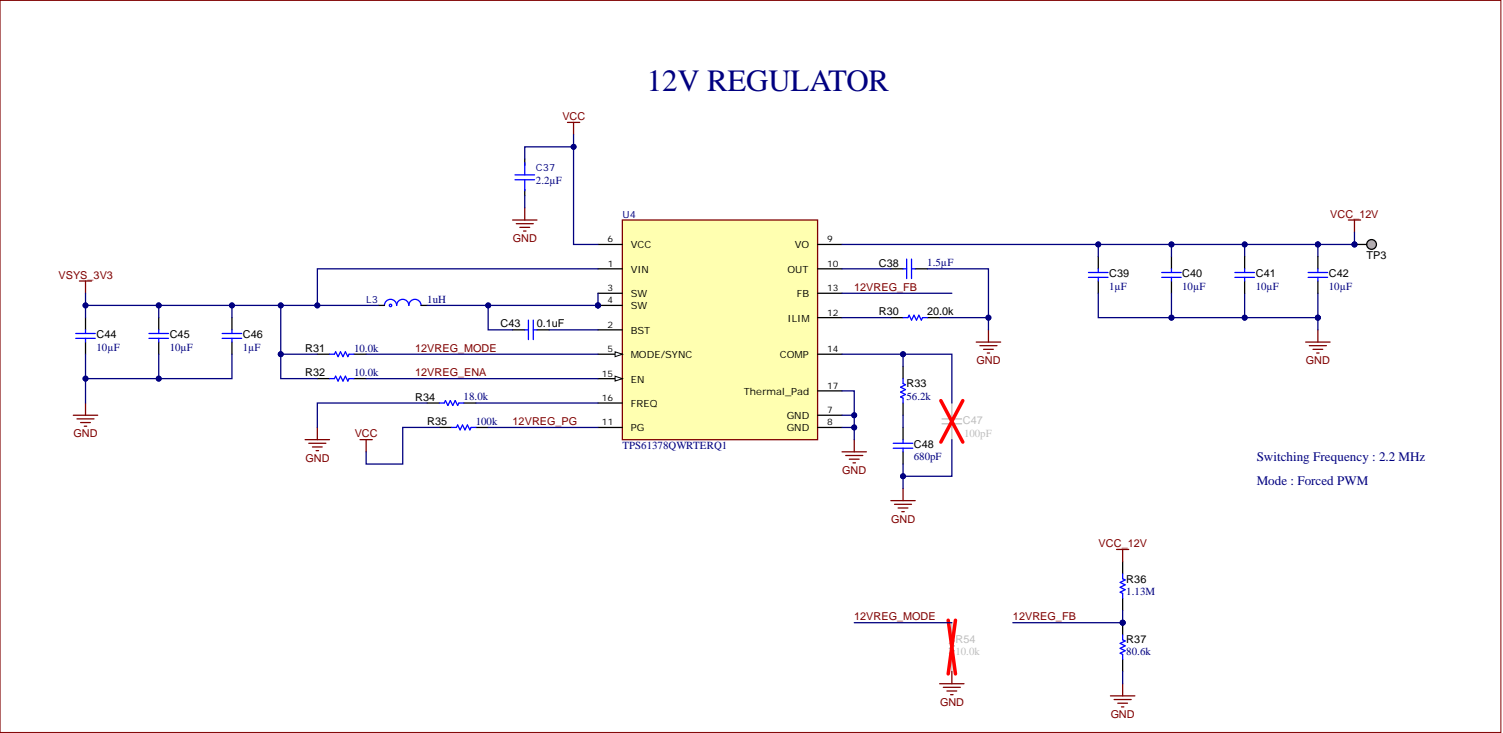
## Fault Indication LED



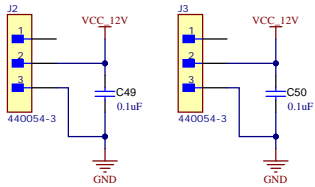
$V_{in}(\min) = 6V$ ,  $V_{in}(\max) = 28V$   
 $V_{out} = 3.3V@24A$   
 $T_a = 25\text{ deg}$

[illegible]

12V0 FAN REGULATOR

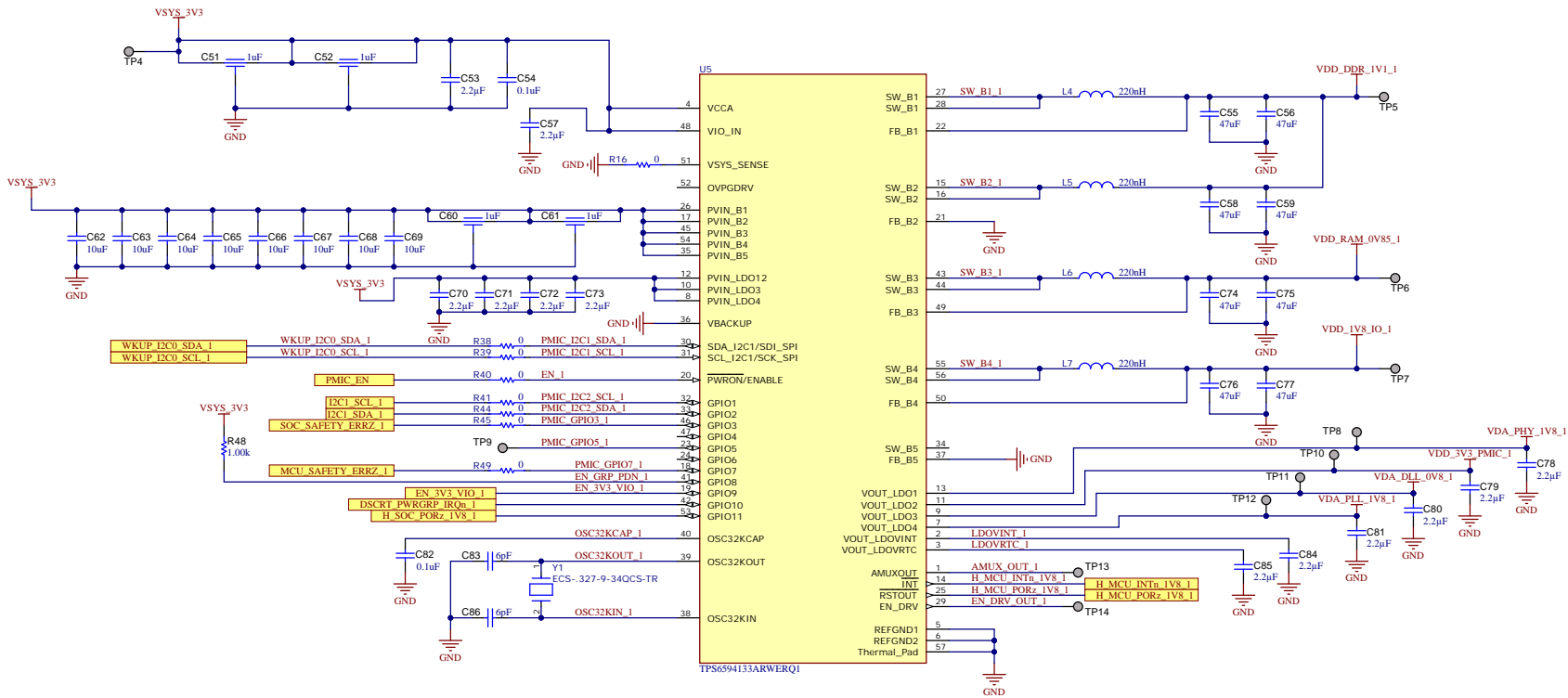


FAN HEADER

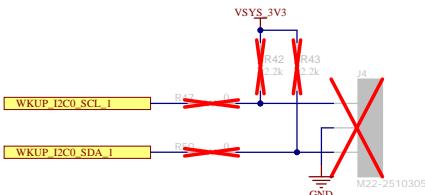


PMIC & LOAD SWITCH SECTION 1

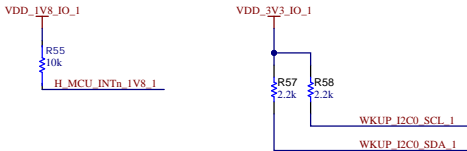
PMIC 1



External I2C HEADER

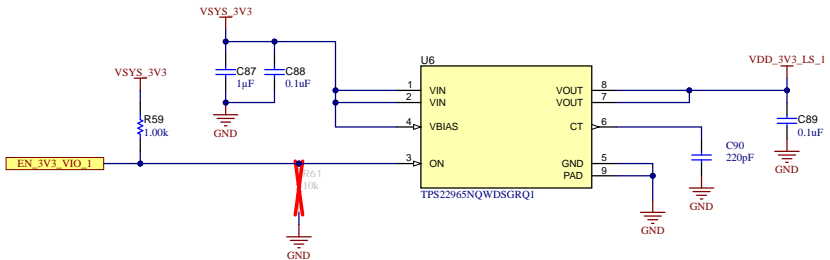


PULL UP



Switching Frequency - 2.2/4.4 MHz  
I2C1 Address - 0X48, 0X49, 0X4A, 0X4B  
I2C2 Address - 0X12

3V3 LOAD SWITCH



3V3 OPTION



"PCB Notes":

For multi-phase Buck converter configs, route remote sense feedback as follows:

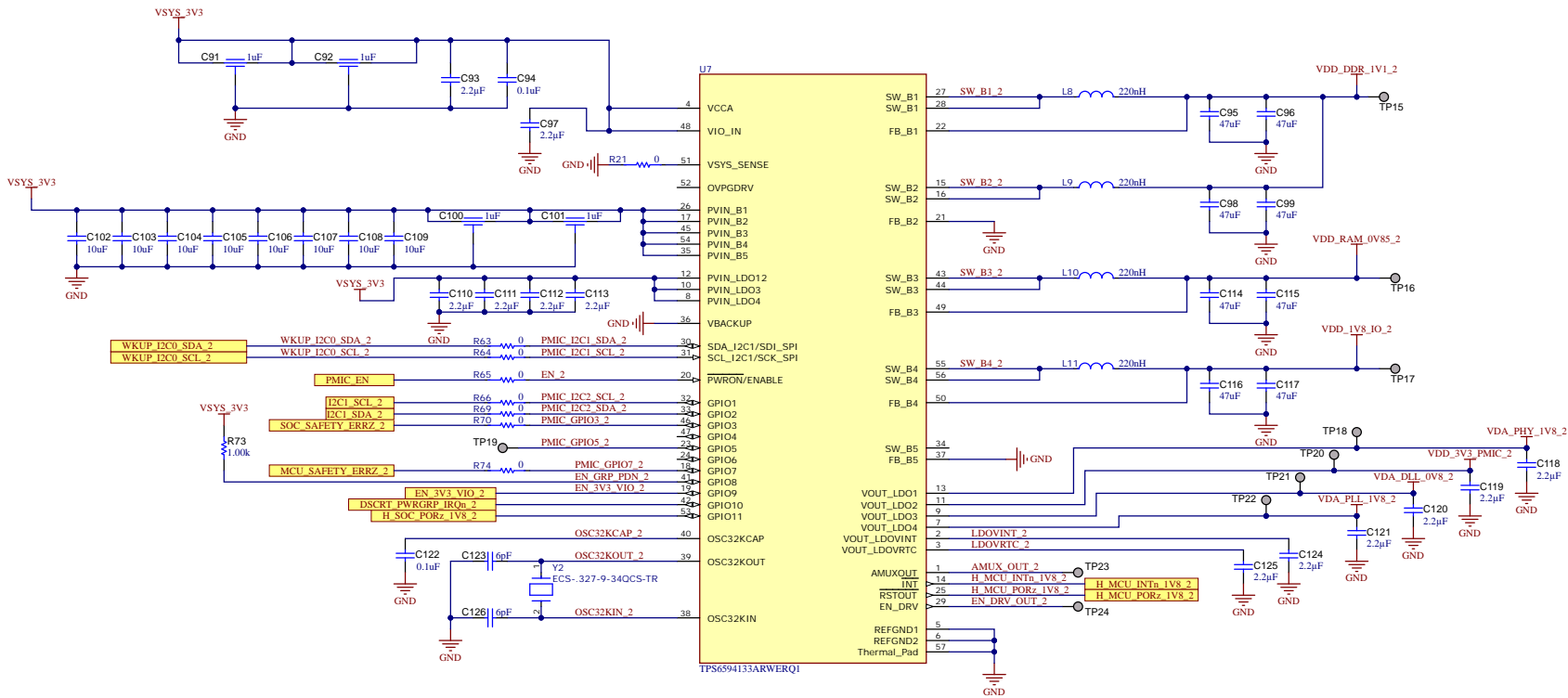
1. Use pseudo differential pair traces on same layer & next to primarily power plane segment. Avoid routing near to any noisy/switching signals.
2. Ensure only 2x Point of Load (PoL) vias connect sense trace to Pwr & Gnd planes near the middle of SOC's power ball group.
3. Ensure only PoL vias connect sense traces to Pwr or Gnd planes. All other vias (at buck component) must have Pwr & Gnd planes isolated
4. Trace widths = 4-8mil & separation distance = 8-50mil, try to keep traces near each other as best as possible.

For single-phase Buck converter configs, route remote sense feedback as follows:

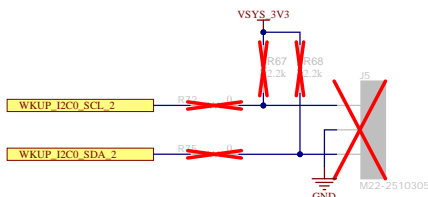
1. Use single-ended traces on same layer & next to primarily power plane segment as best as possible. Avoid routing near to any noisy/switching signals.
2. Ensure only 1x PoL via connects sense trace to Pwr plane near the middle of SOC's power ball group.
3. Ensure only PoL vias connect sense traces to Pwr or Gnd planes. All other vias (at buck component) must have Pwr & Gnd planes isolated.
4. Trace widths = 4-8mil.

PMIC & LOAD SWITCH SECTION 2

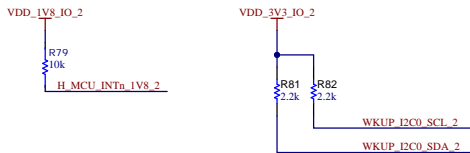
PMIC 2



External I2C HEADER

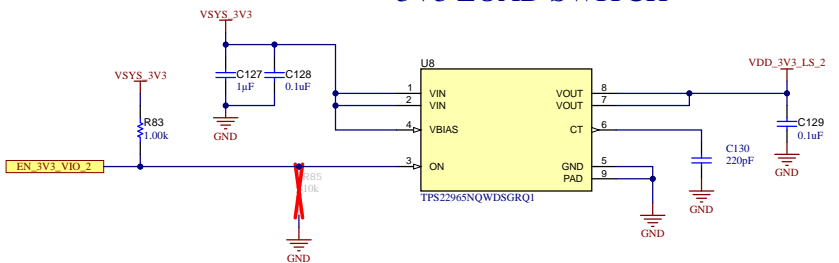


PULL UP

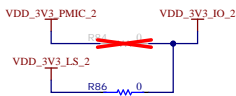


Switching Frequency - 2.2/4.4 MHz  
I2C1 Address - 0X48, 0X49, 0X4A, 0X4B  
I2C2 Address - 0X12

3V3 LOAD SWITCH



3V3 OPTION



"PCB Notes":

For multi-phase Buck converter configs, route remote sense feedback as follows:

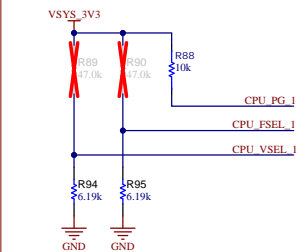
1. Use pseudo differential pair traces on same layer & next to primarily power plane segment. Avoid routing near to any noisy/switching signals.
2. Ensure only 2x Point of Load (PoL) vias connect sense trace to Pwr & Gnd planes near the middle of SOC's power ball group.
3. Ensure only PoL vias connect sense traces to Pwr or Gnd planes. All other vias (at buck component) must have Pwr & Gnd planes isolated
4. Trace widths = 4-8mil & separation distance = 8-50mil, try to keep traces near each other as best as possible.

For single-phase Buck converter configs, route remote sense feedback as follows:

1. Use single-ended traces on same layer & next to primarily power plane segment as best as possible. Avoid routing near to any noisy/switching signals.
2. Ensure only 1x PoL via connects sense trace to Pwr plane near the middle of SOC's power ball group.
3. Ensure only PoL vias connect sense traces to Pwr or Gnd planes. All other vias (at buck component) must have Pwr & Gnd planes isolated.
4. Trace widths = 4-8mil.

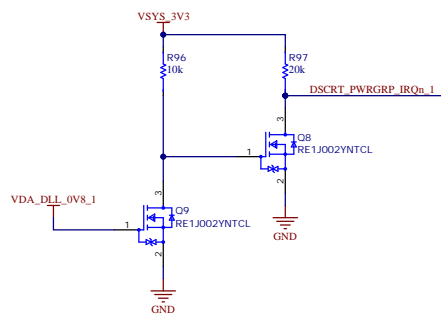


## CONTROL\_SIGNALS

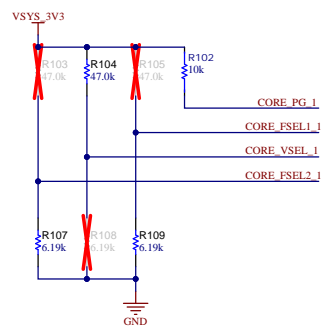


Buck EN control aligned to VDA\_DLL\_0V8 for power sequencing  
EN pin is bi-directional that both enables and report status

## ENABLE\_SIGNAL

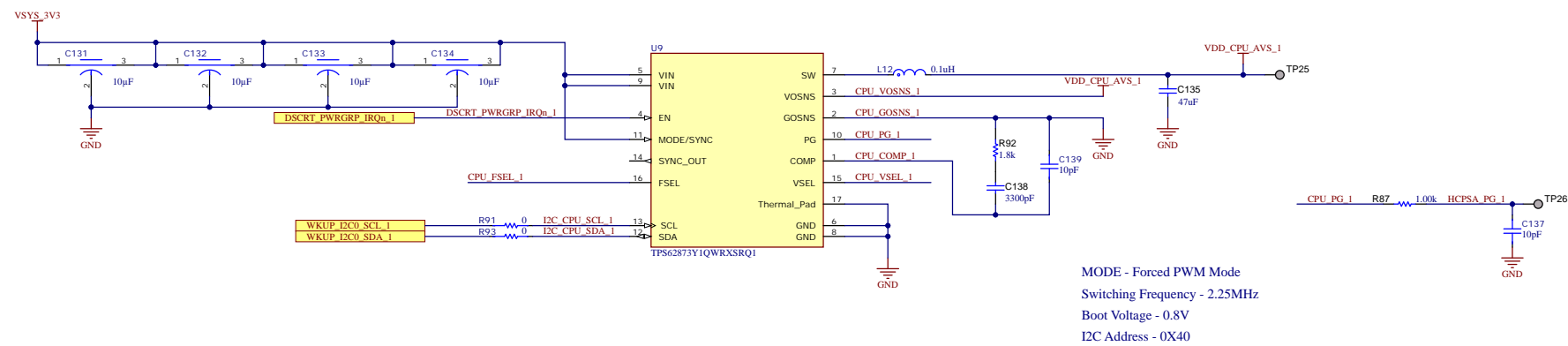


## CONTROL\_SIGNALS



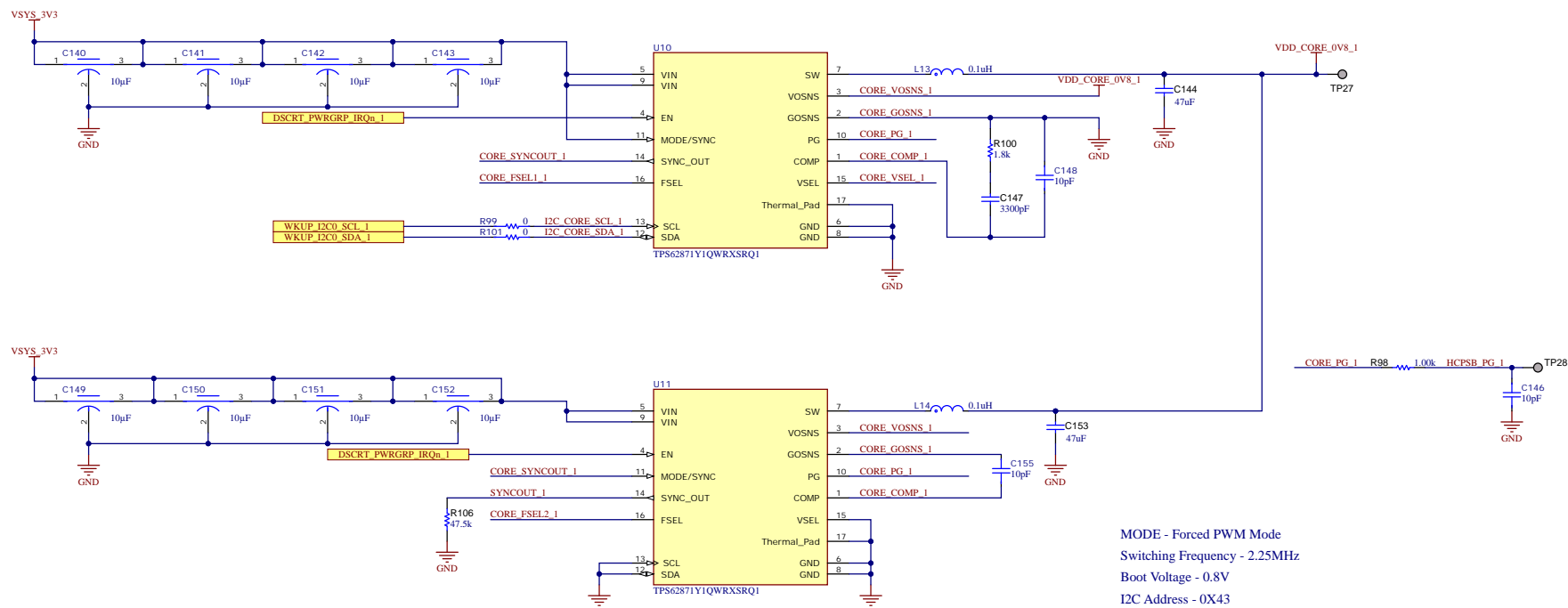
## HCPS-A REGULATOR 1

### VDD\_CPU\_AVS\_REGULATOR 1



## HCPS-B REGULATOR 1

### VDD\_CORE\_0V8\_REGULATOR 1



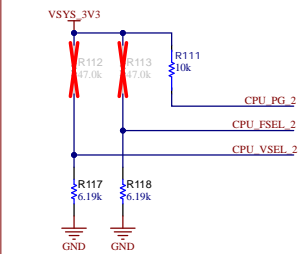
"PCB Notes":

Route remote sense as "VOSNS & GOSNS" as pseudo differential pair trace.

Line to Shape keepout needs to be given in layout for VDD\_CPU\_AVS\_x & VDD\_CORE\_0V8\_x and DGND feedback traces

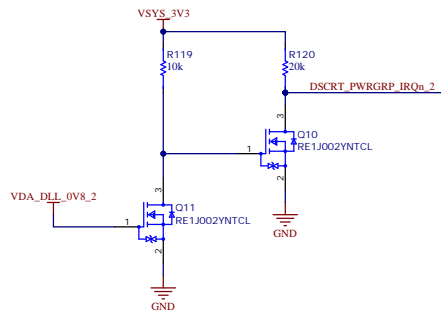
Note: Via keepout areas need to be applied to positive & negative remote sense traces/hets (i.e. "VOSNS/\_GOSNS") both at the buck & along diff trace routing path between buck"xOSNS" pins to ensure no unwanted power or Gnd connections are made before reaching the desired remote sense location where only 1x power & Gnd connection should be made

## CONTROL\_SIGNALS

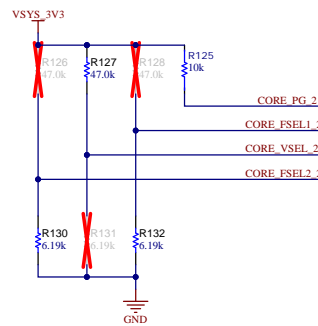


Buck EN control aligned to VDA\_DLL\_0V8 for power sequencing  
EN pin is bi-directional that both enables and report status

## ENABLE\_SIGNAL

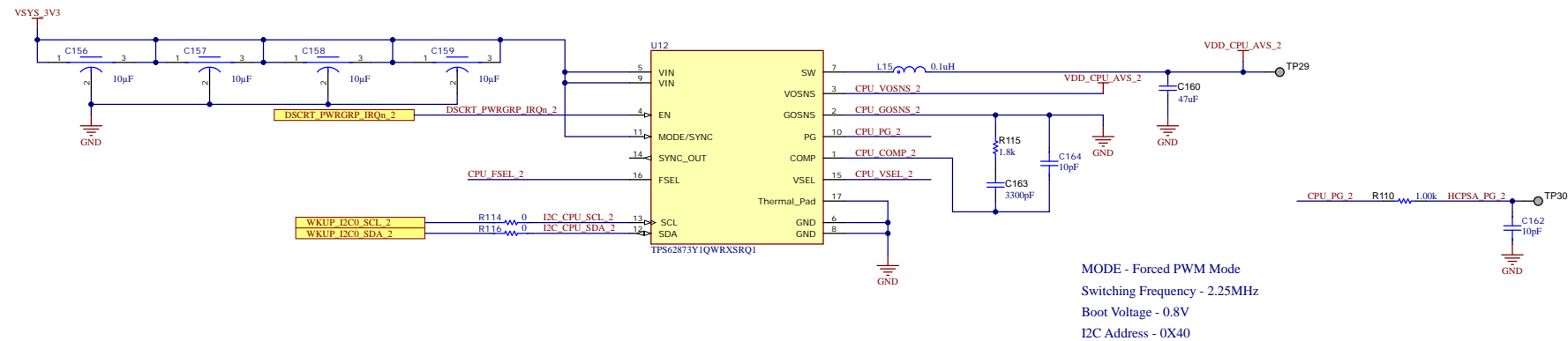


## CONTROL\_SIGNALS



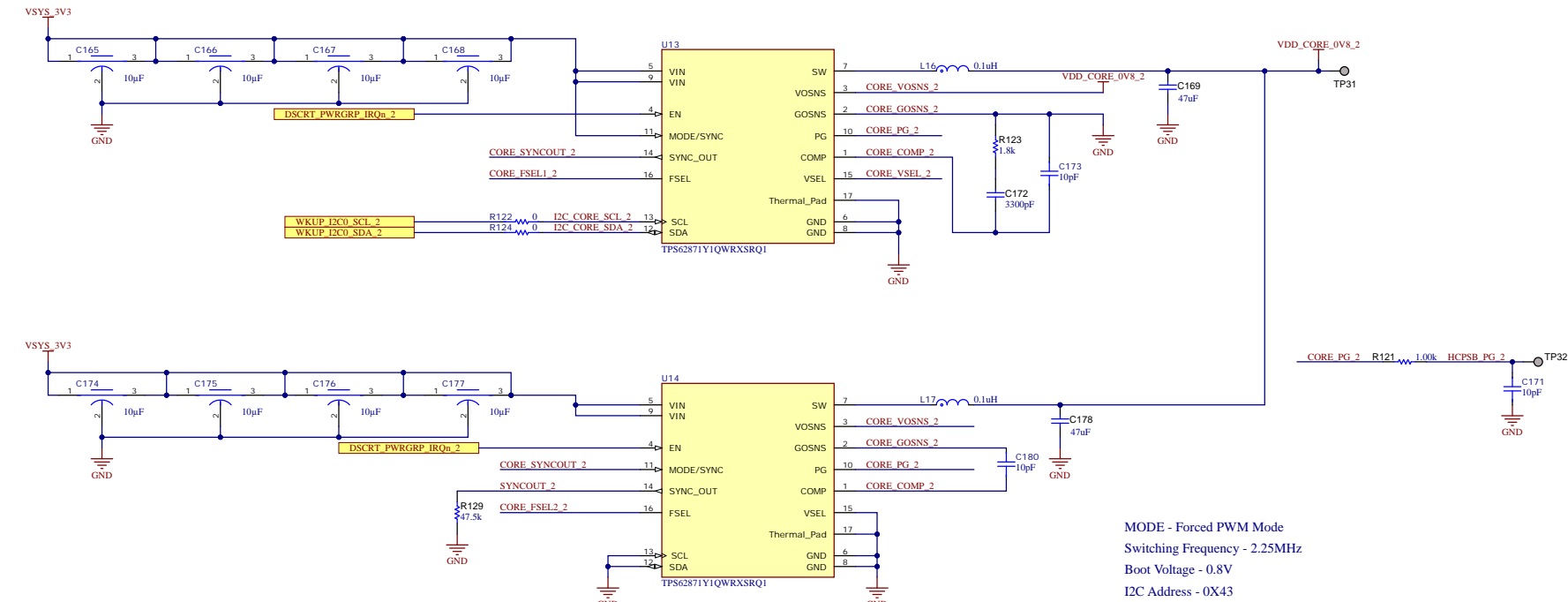
## HCPS-A REGULATOR 2

### VDD\_CPU\_AVS\_REGULATOR 2



## HCPS-B REGULATOR 2

### VDD\_CORE\_0V8\_REGULATOR 2



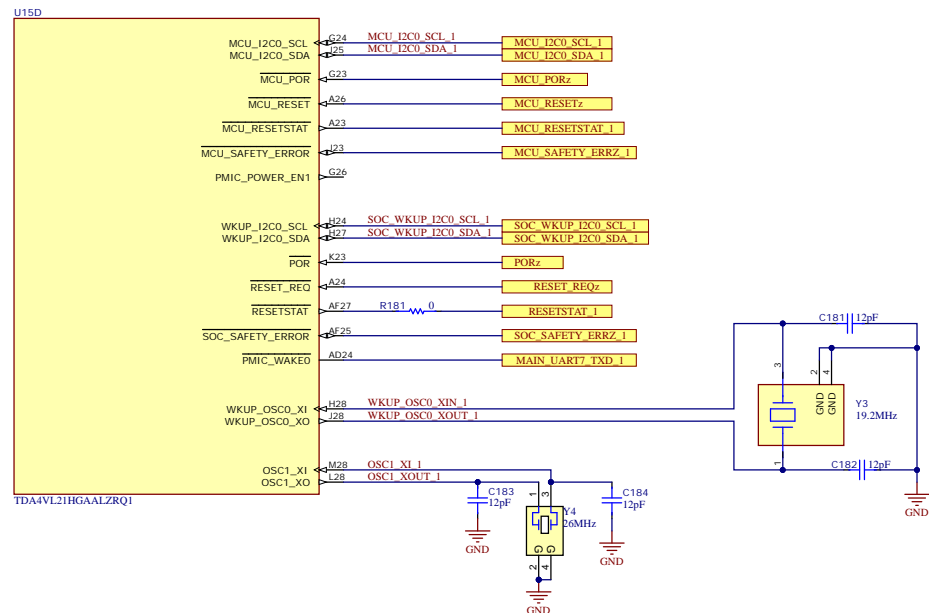
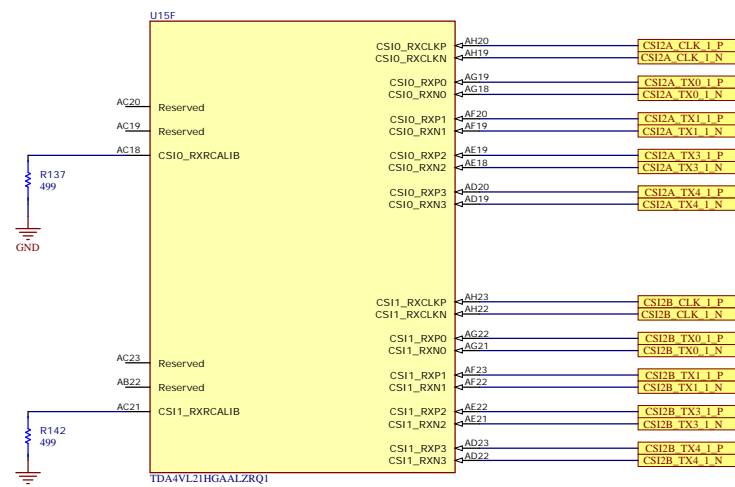
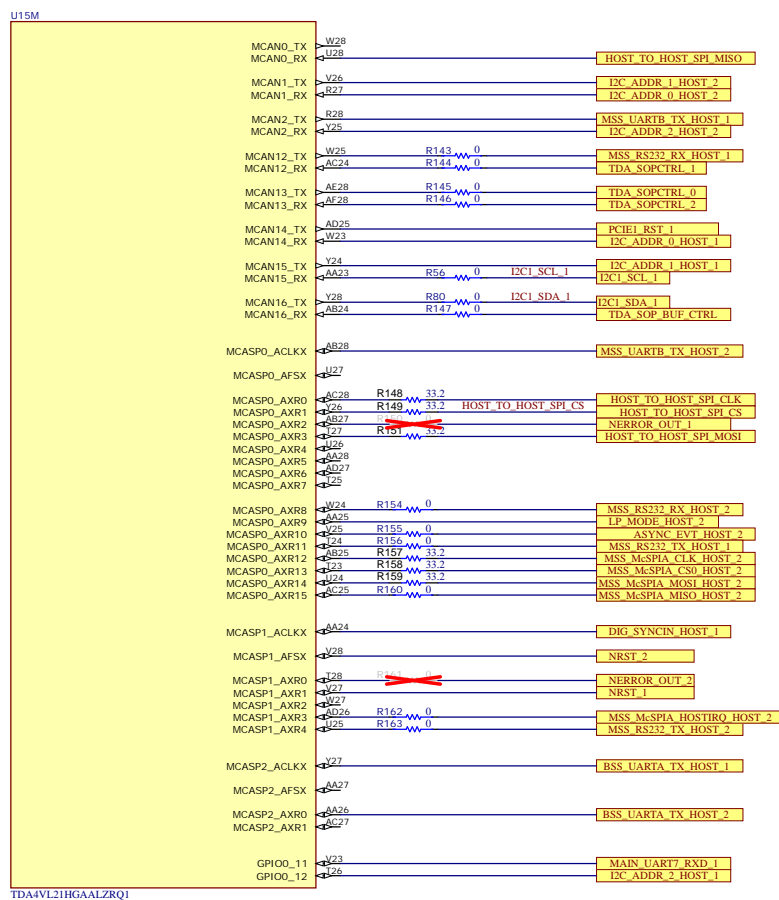
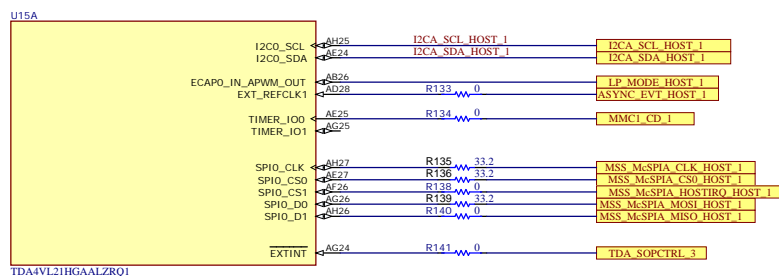
"PCB Notes":

Route remote sense as "VOSNS & GOSNS" as pseudo differential pair trace.

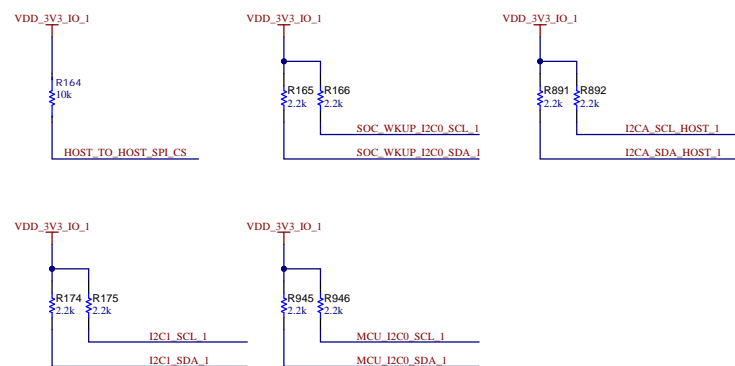
Line to Shape keepout needs to be given in layout for VDD\_CPU\_AVS\_x & VDD\_CORE\_0V8\_x and DGND feedback traces

Note: Via keepout areas need to be applied to positive & negative remote sense traces/hets (i.e. "VOSNS/\_GOSNS") both at the buck & along diff trace routing path between buck"xOSNS" pins to ensure no unwanted power or Gnd connections are made before reaching the desired remote sense location where only 1x power & Gnd connection should be made

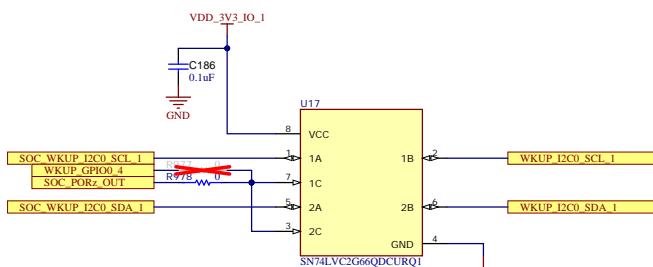
## PROCESSOR IO SECTION 1



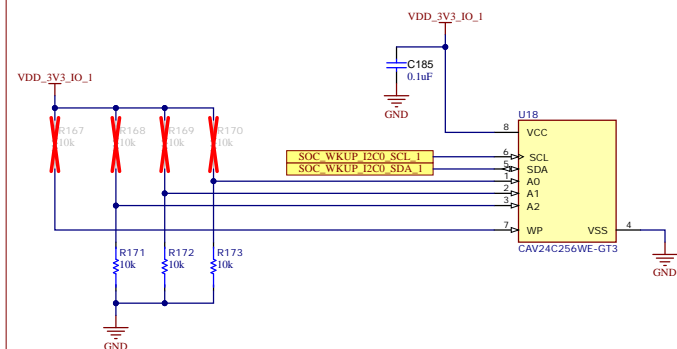
## PULL UPs



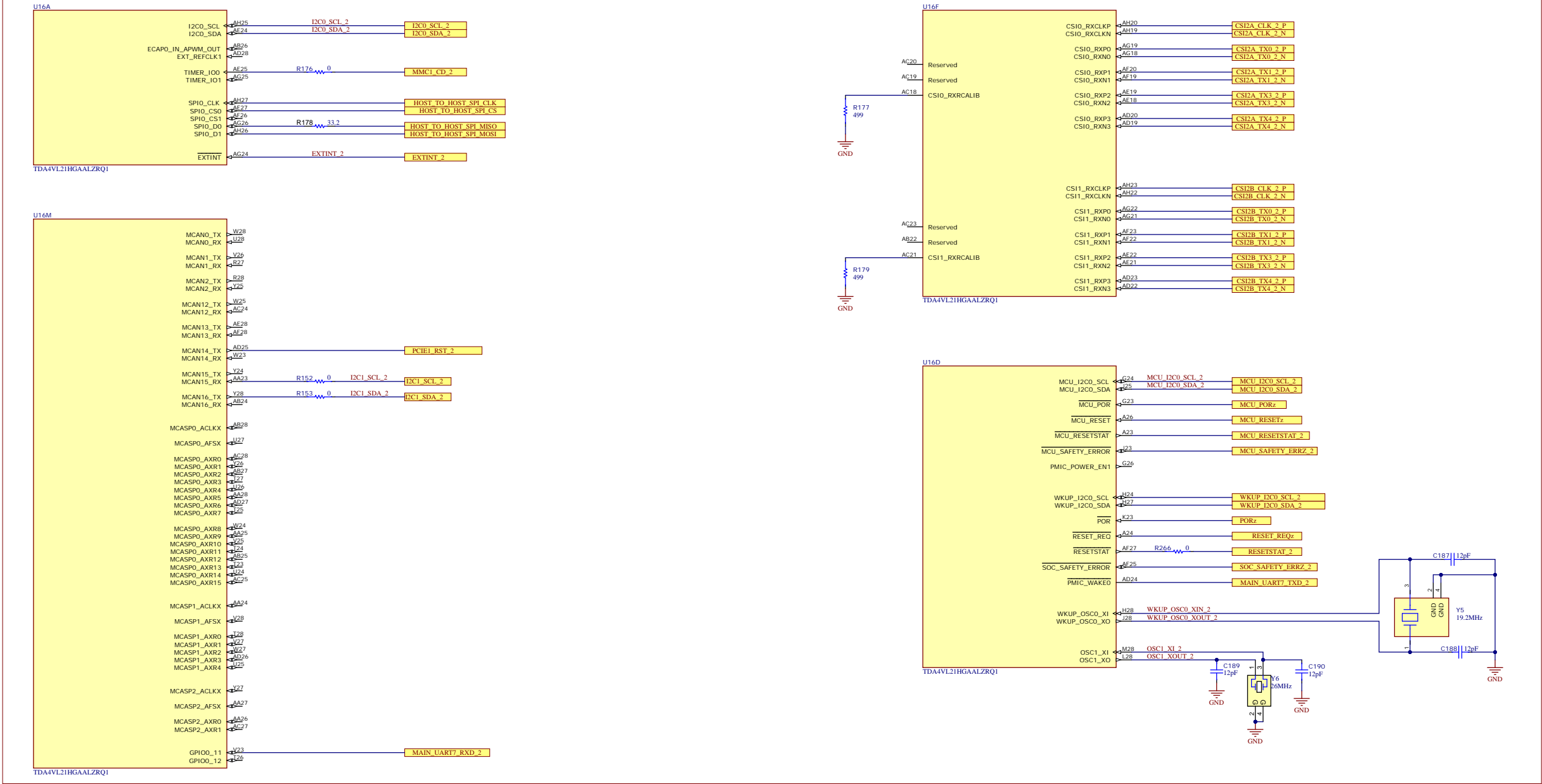
## VOLTAGE ISOLATION



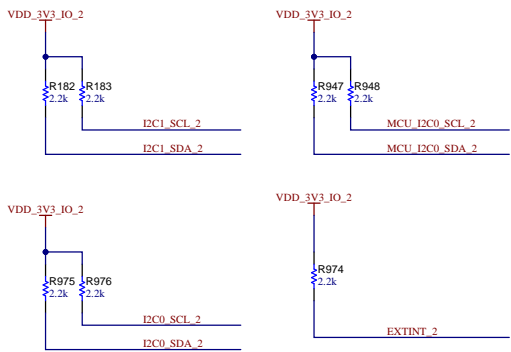
## BOARD ID EEPROM



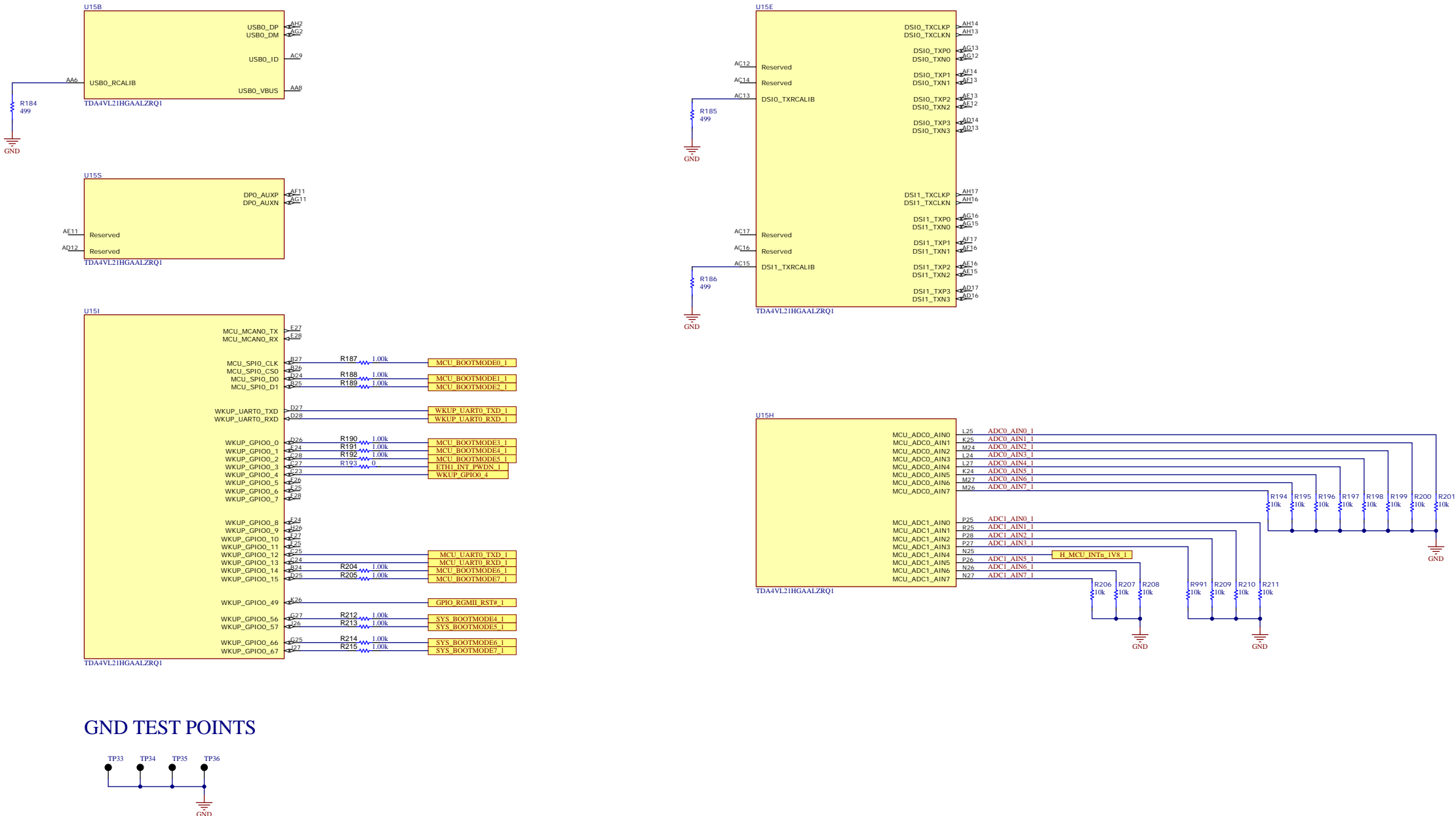
PROCESSOR IO SECTION 2



PULL UPS

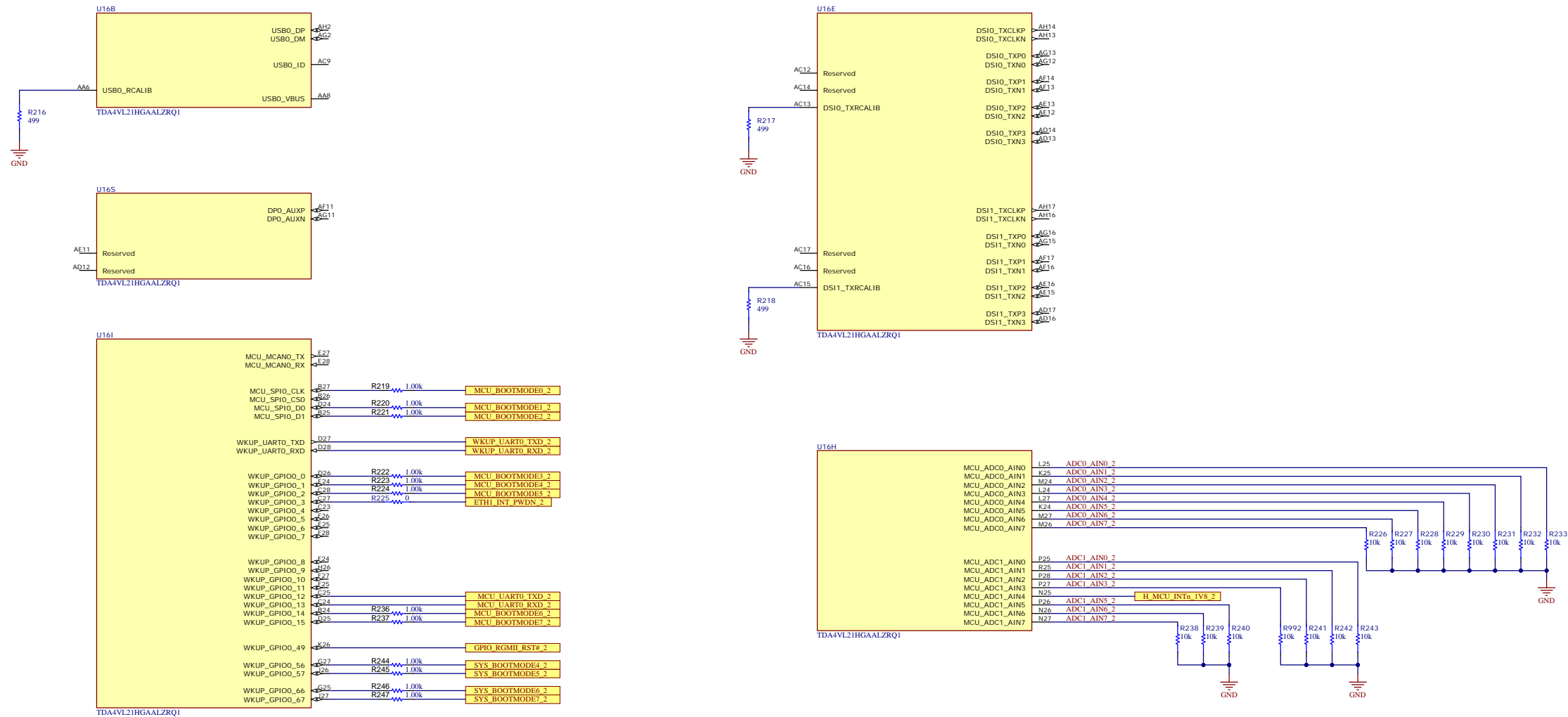


PROCESSOR IO SECTION 1

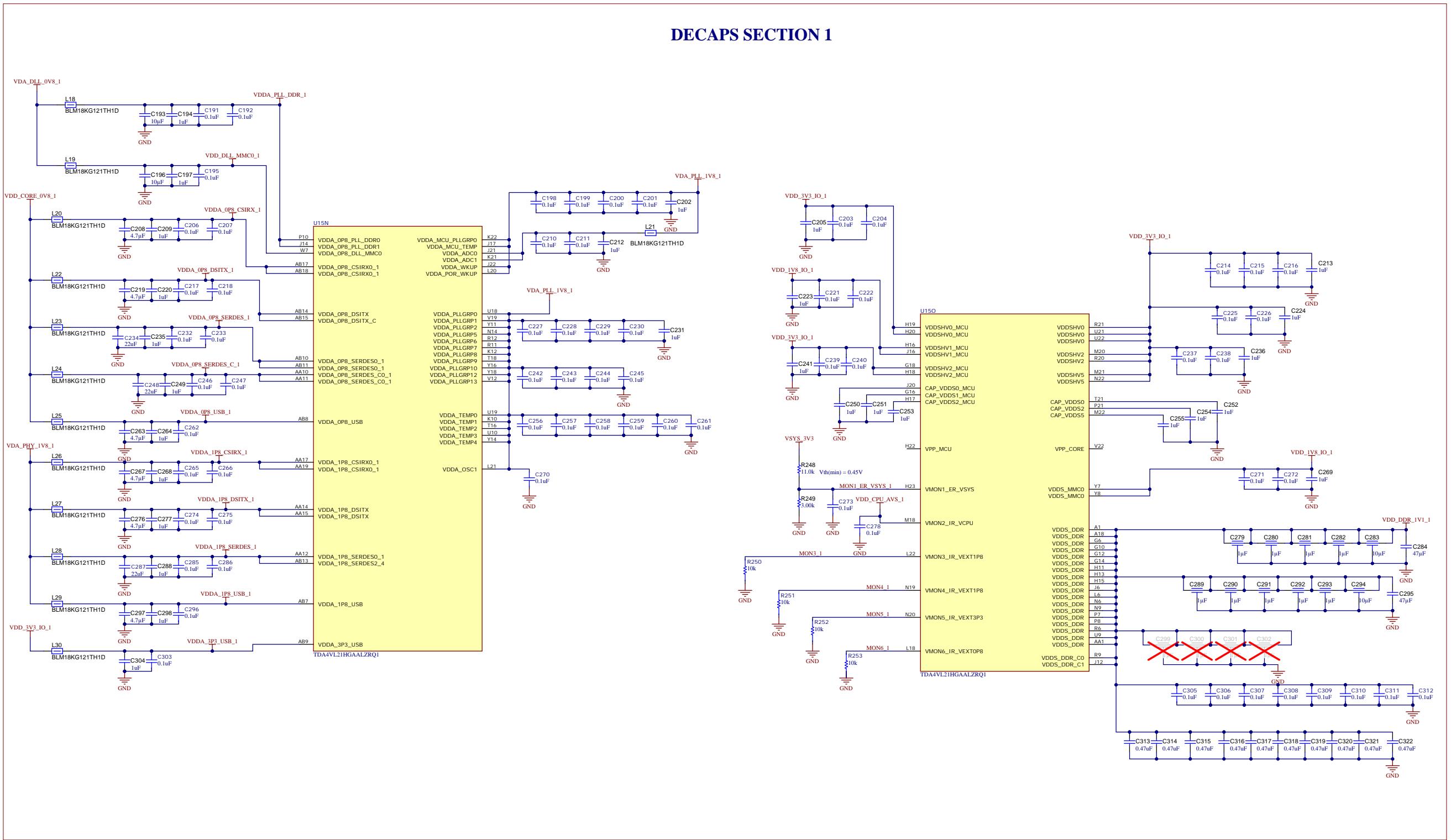




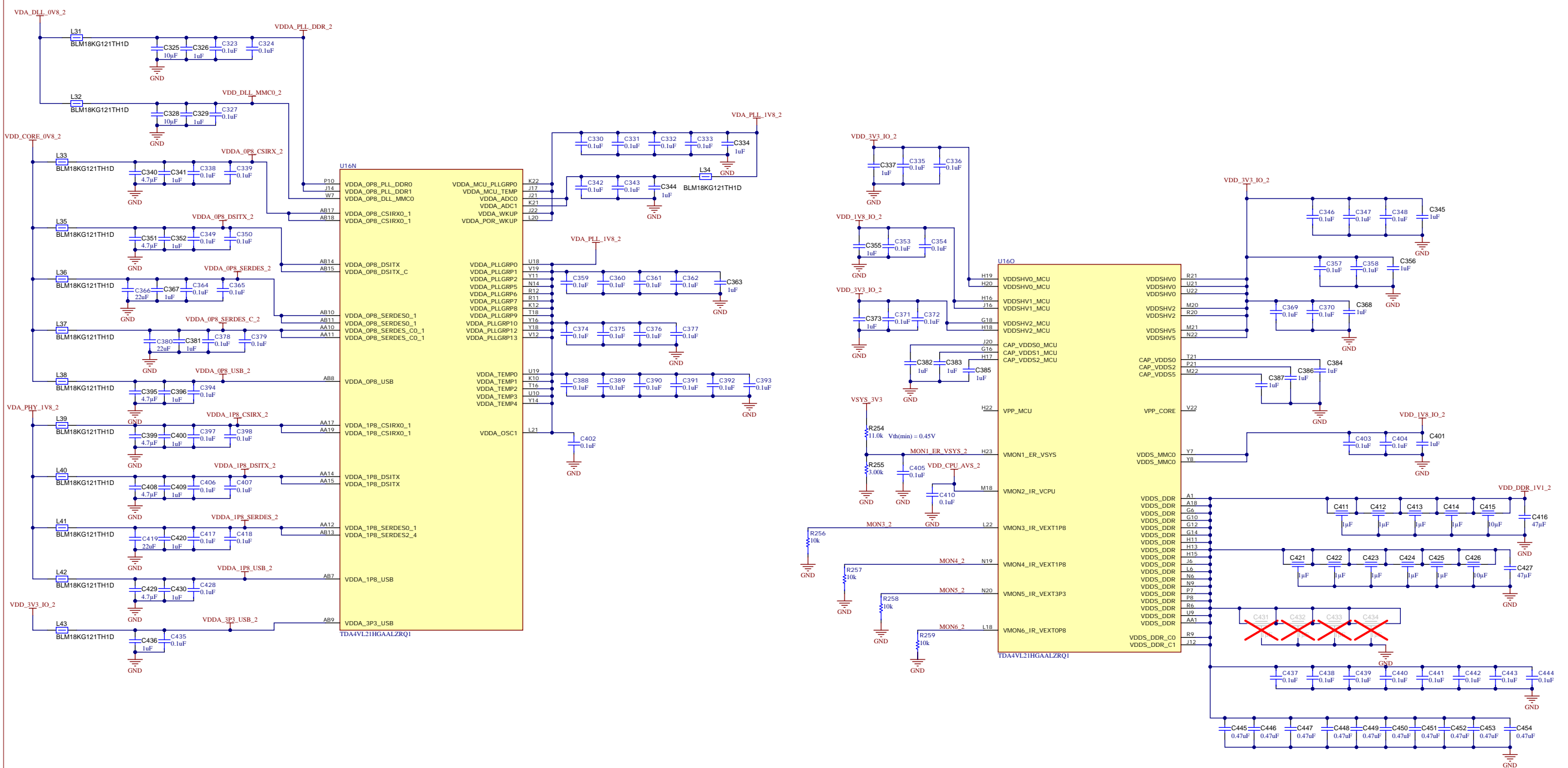
## PROCESSOR IO SECTION 2



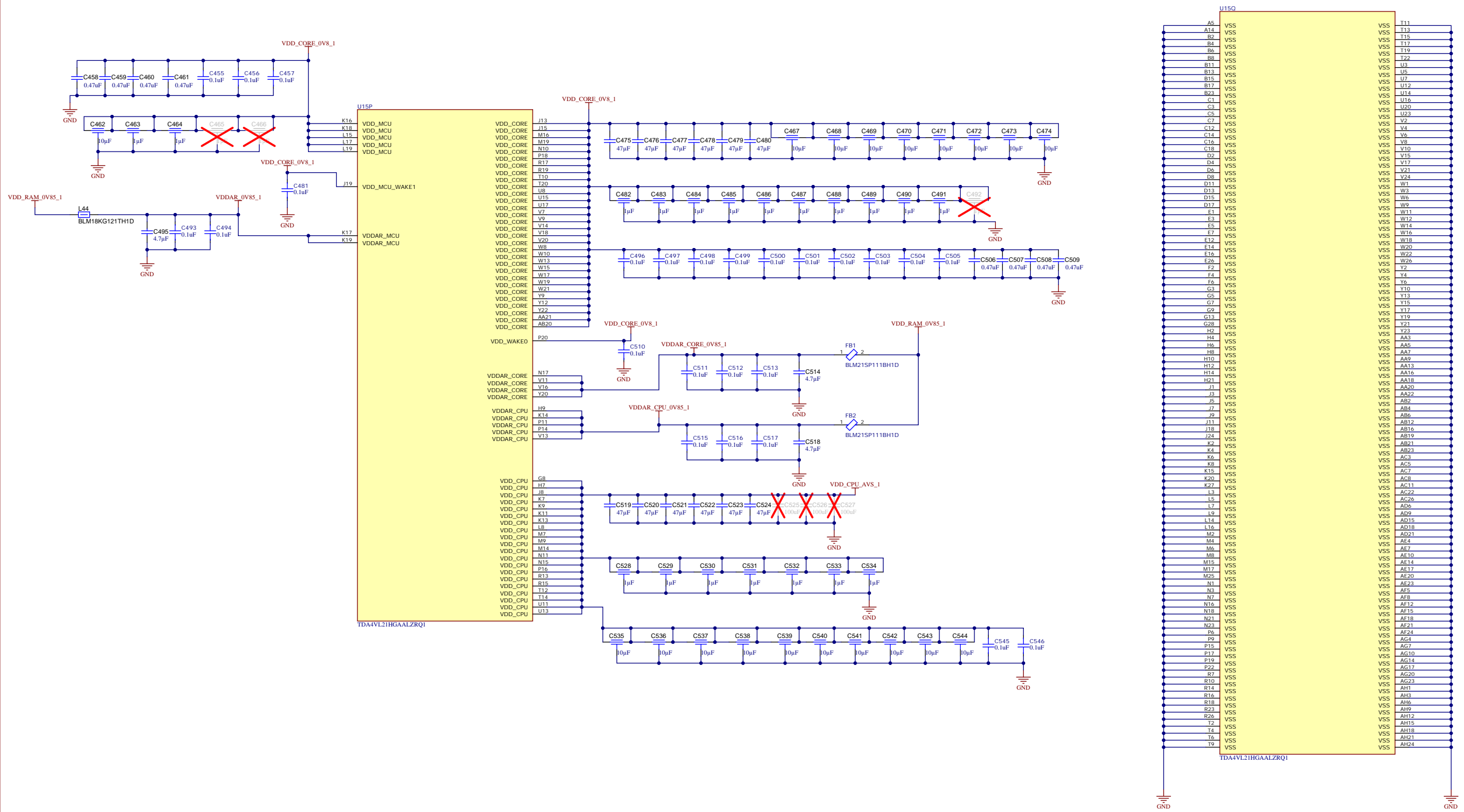
DECAPS SECTION 1



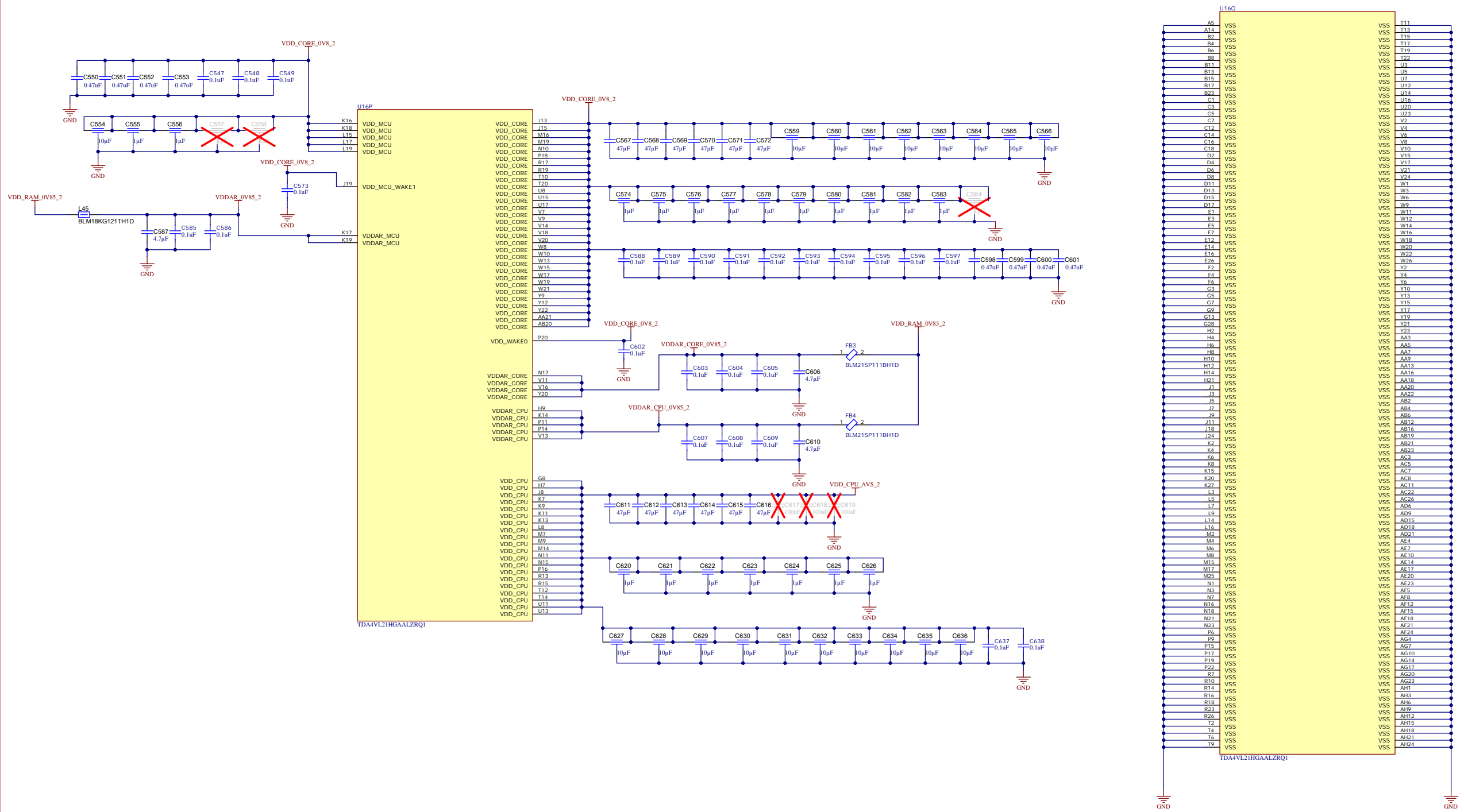
DECAPS SECTION 2



DECAPS SECTION 1

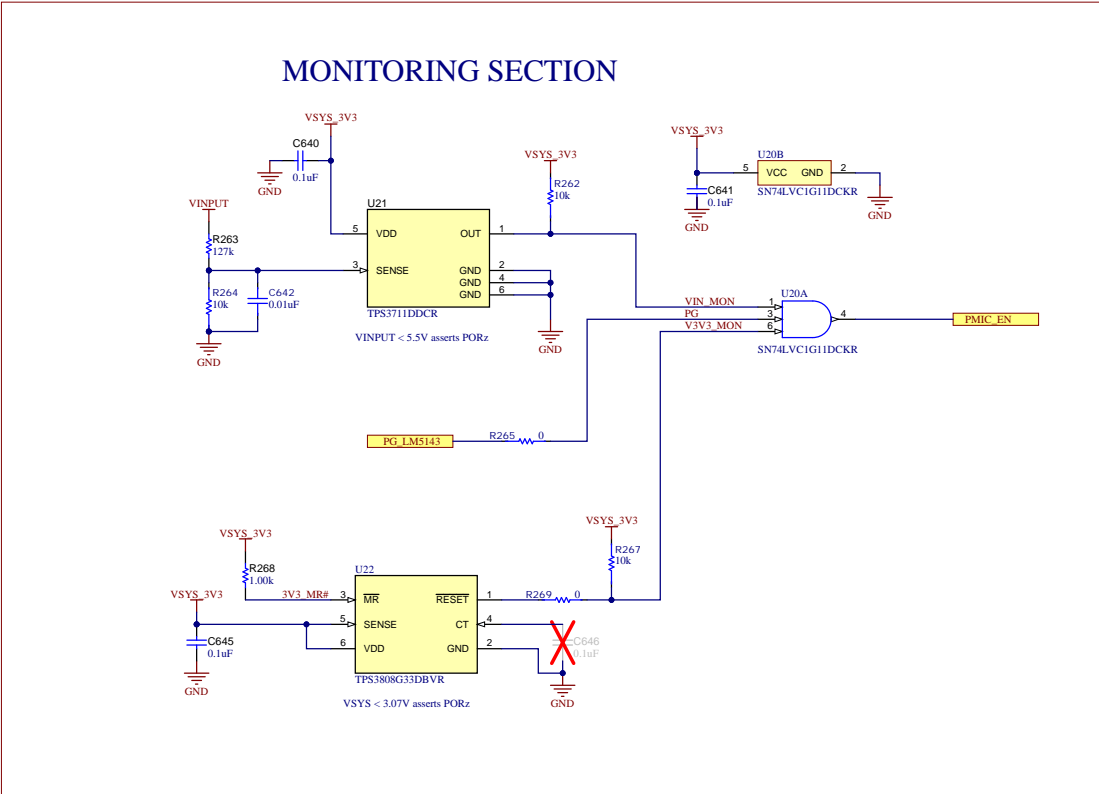
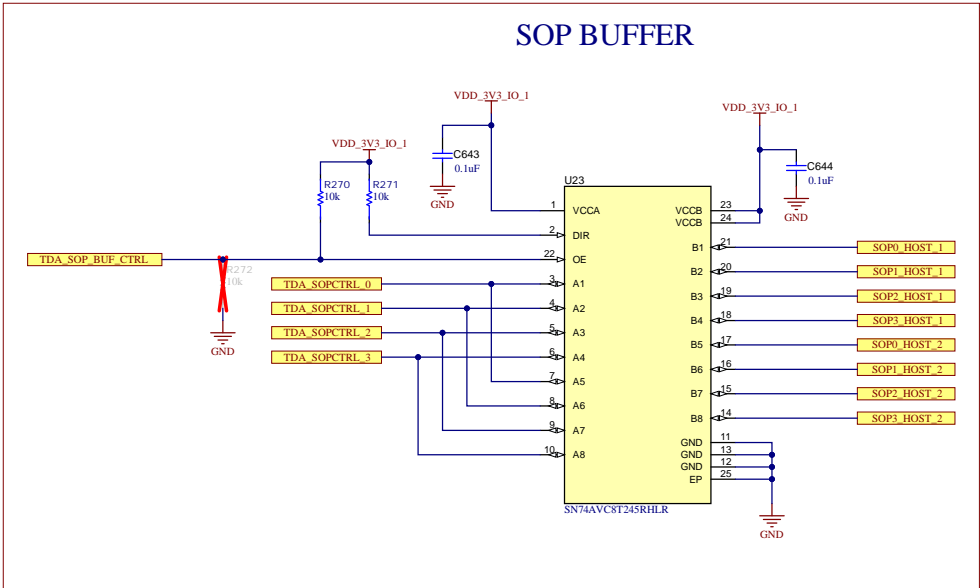
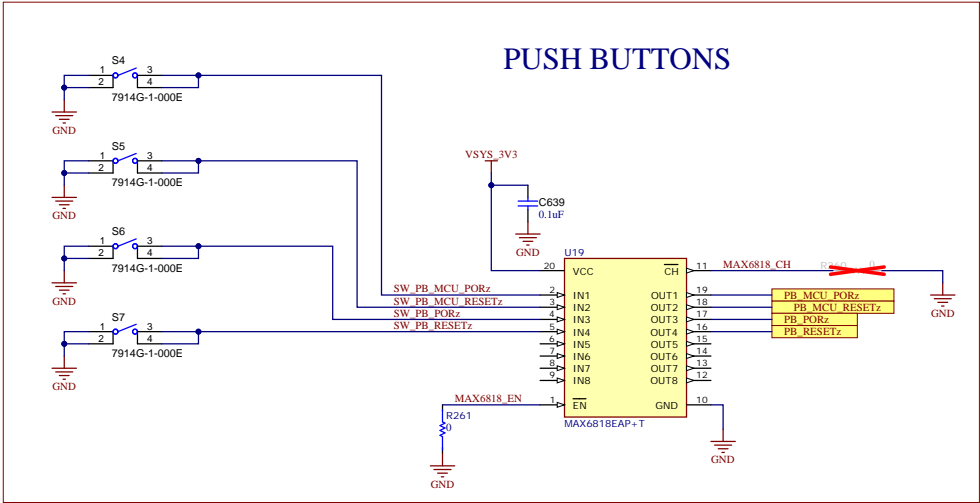


DECAPS SECTION 2



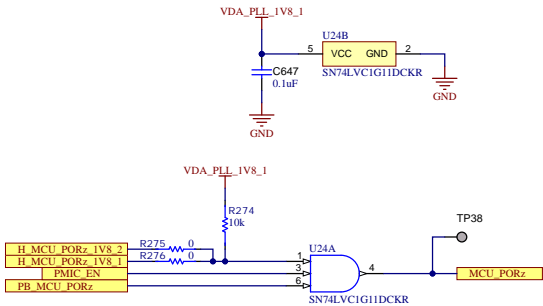


RESET PUSH BUTTONS, SOP BUFFER & MONITORING SECTION

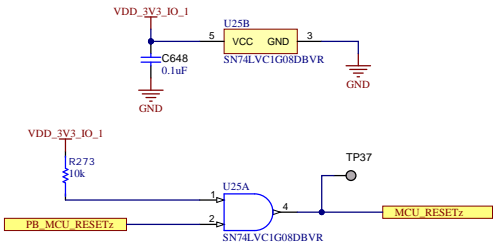


RESET SECTION

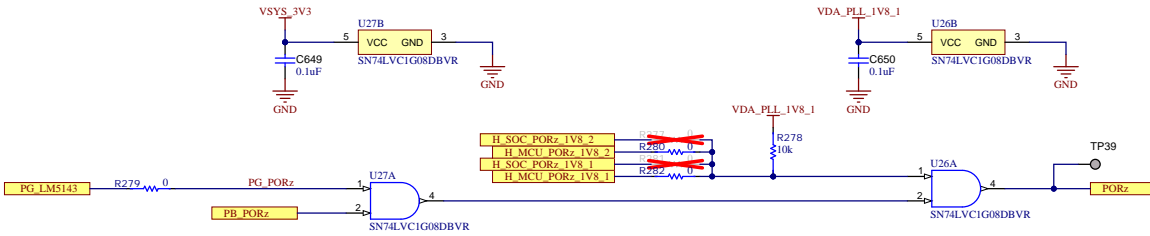
MCU\_PORz



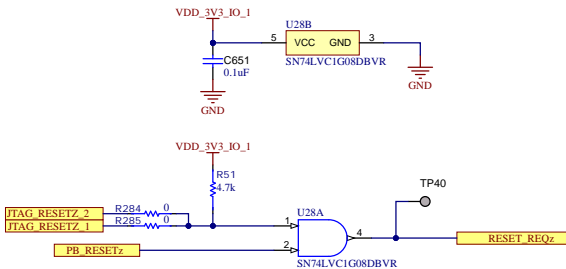
MCU\_RESETz



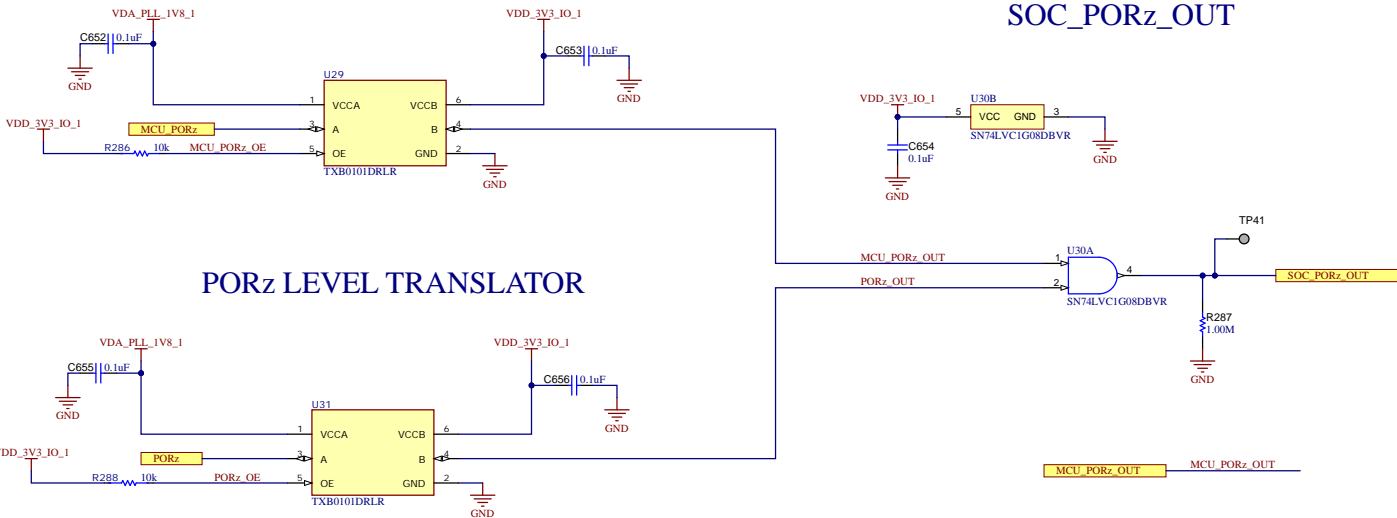
PORz



RESETz

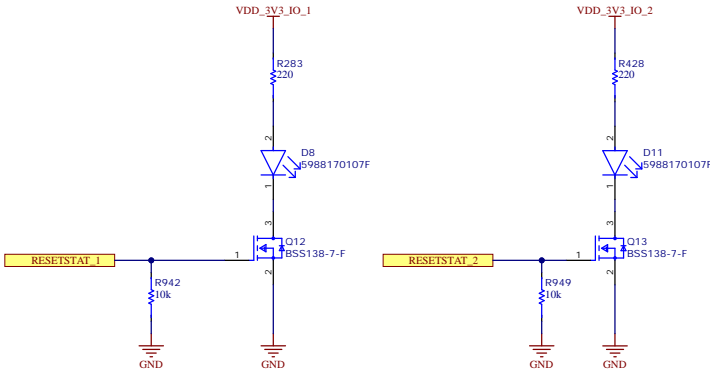


MCU\_PORz LEVEL TRANSLATOR



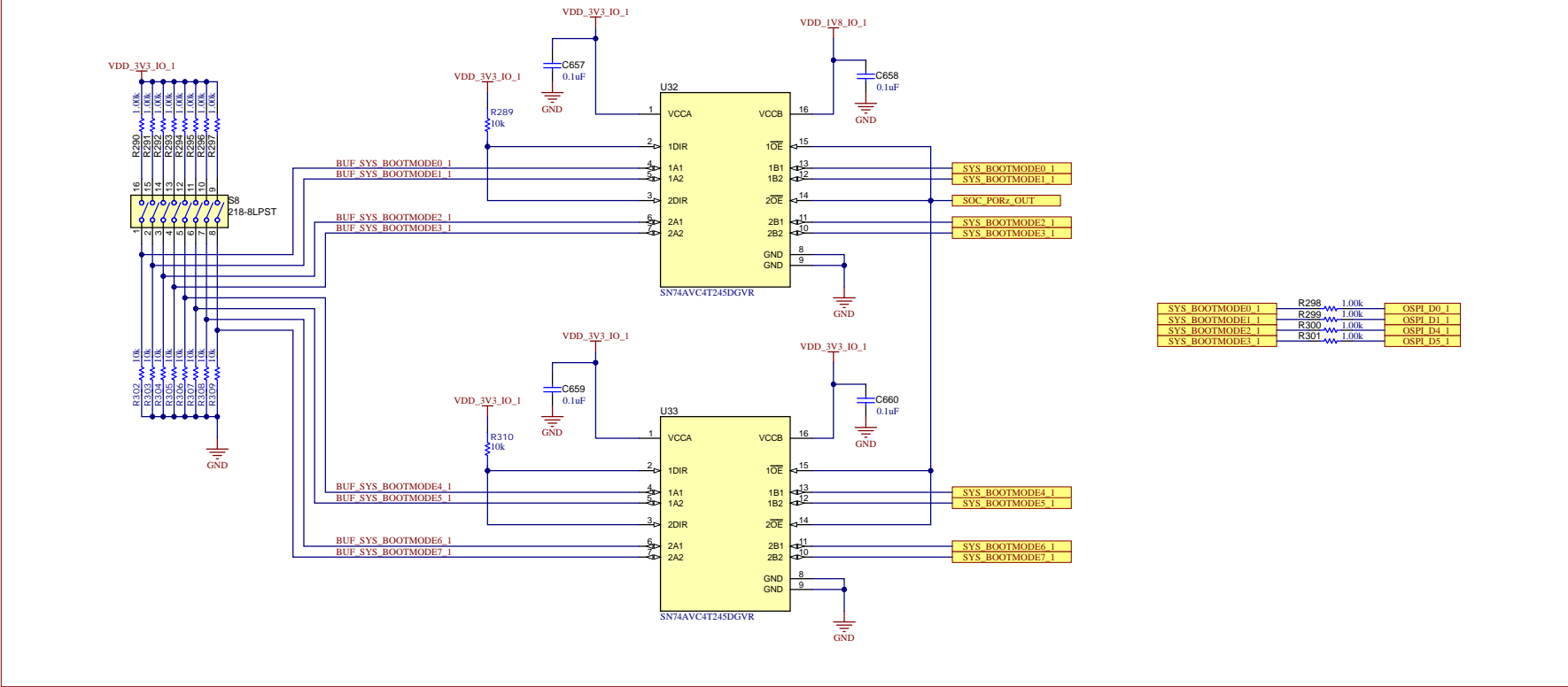
SOC\_PORz\_OUT

RESET LEDs

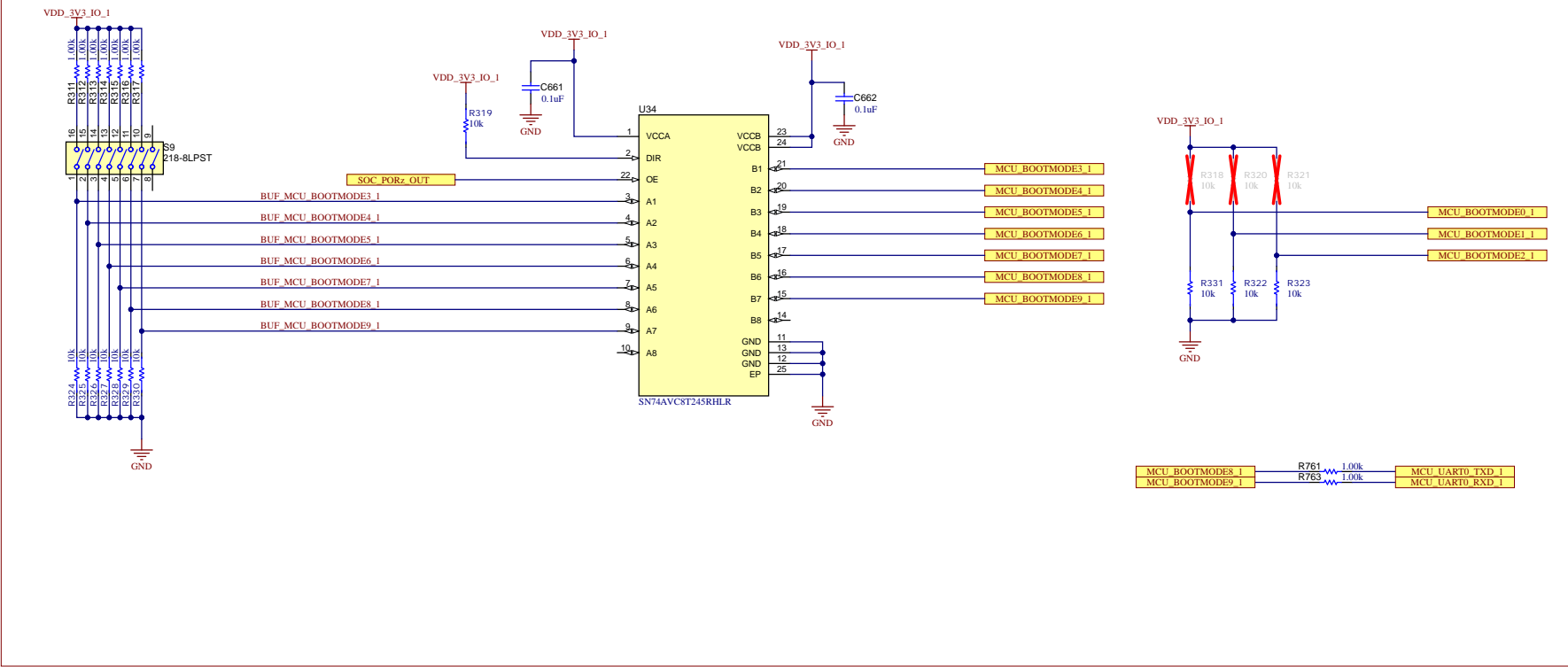


BOOTMODE SWITCHES 1

SYS BOOTMODE SWITCHES

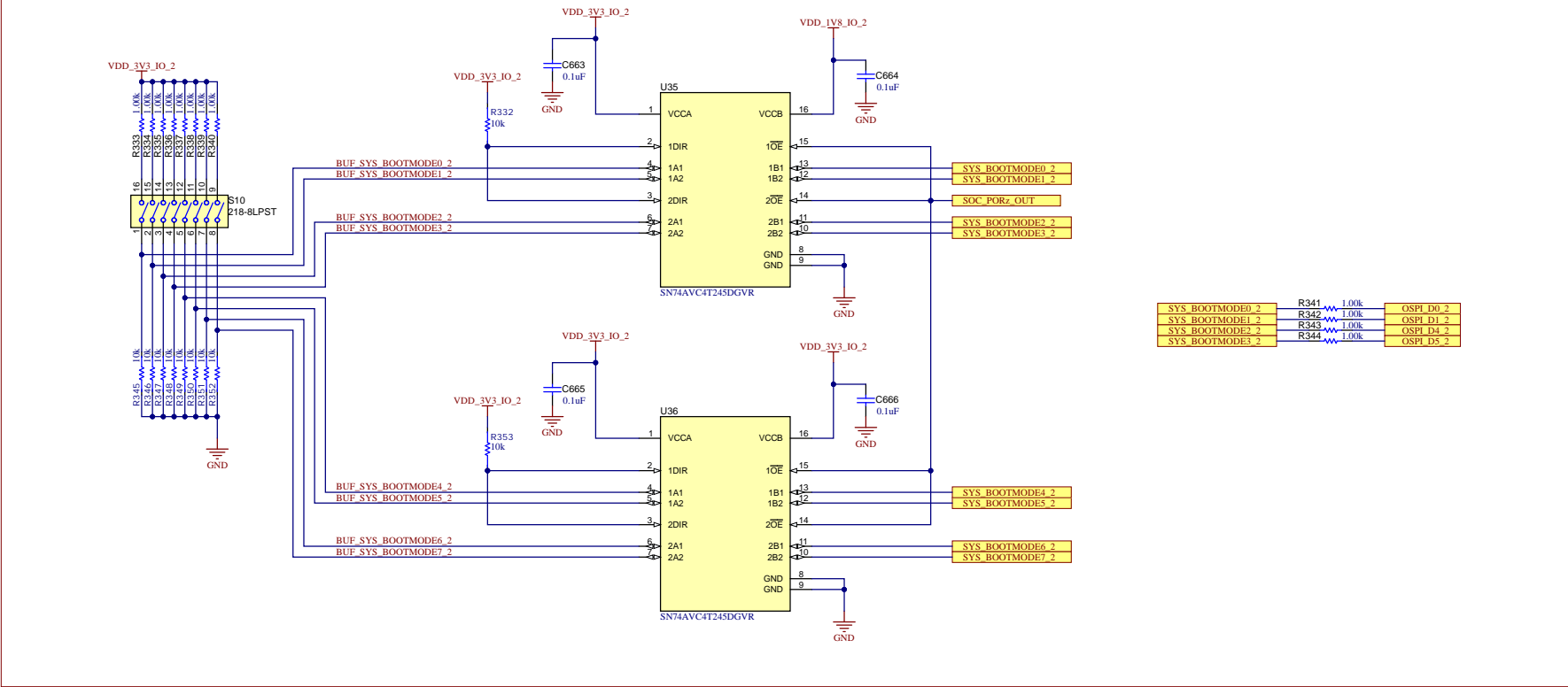


MCU BOOTMODE SWITCHES

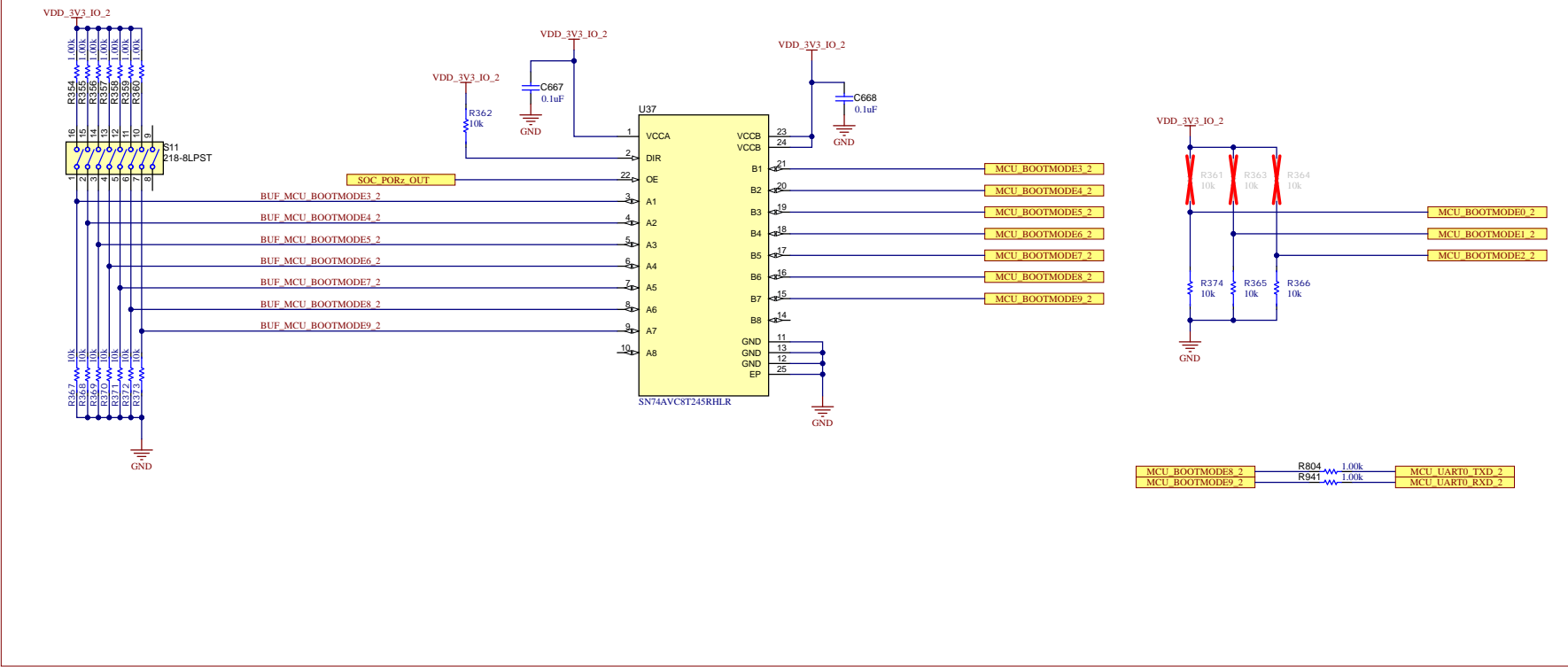


BOOTMODE SWITCHES 2

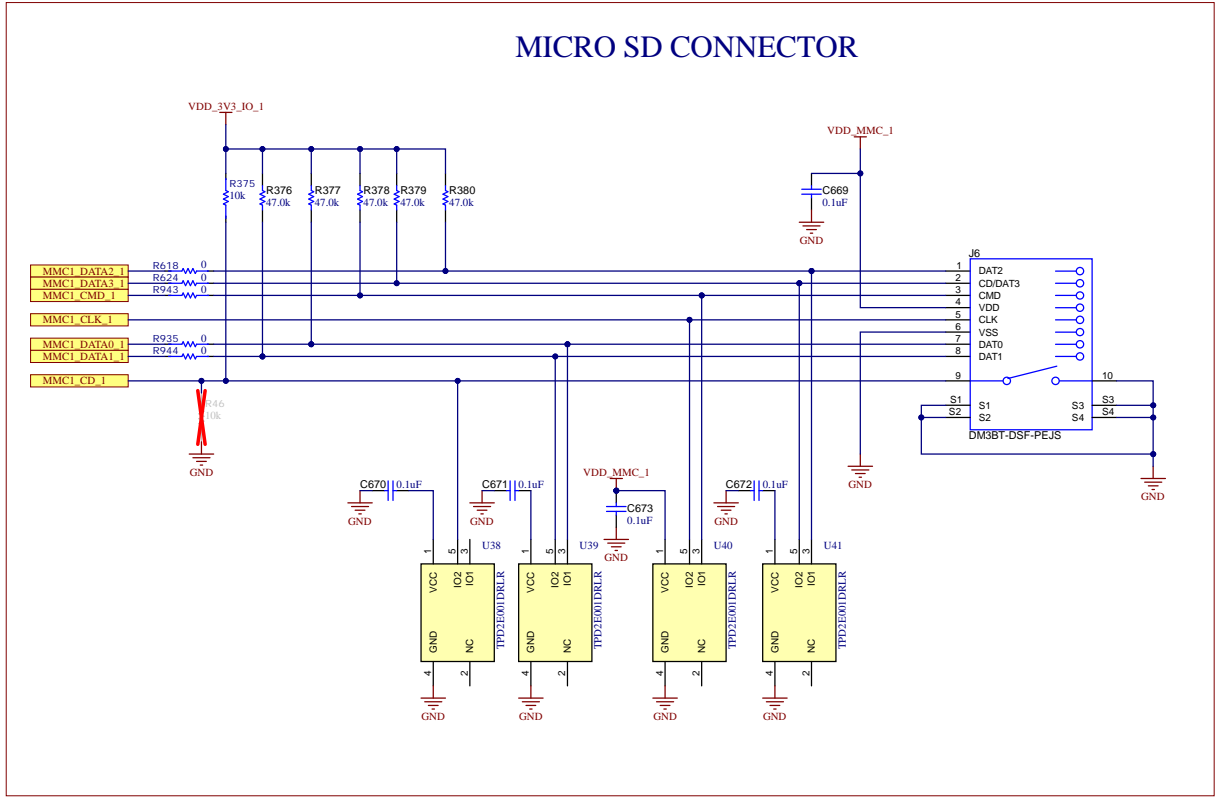
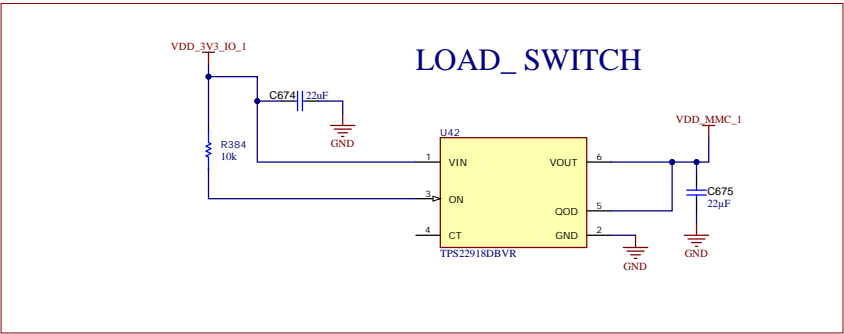
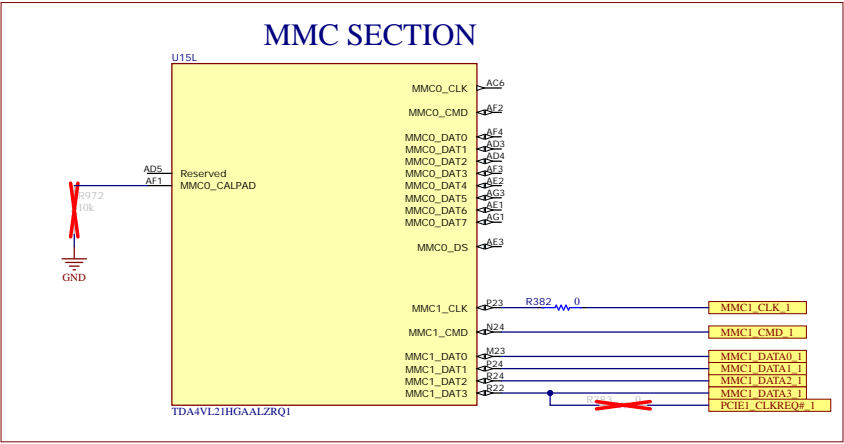
SYS BOOTMODE SWITCHES



MCU BOOTMODE SWITCHES

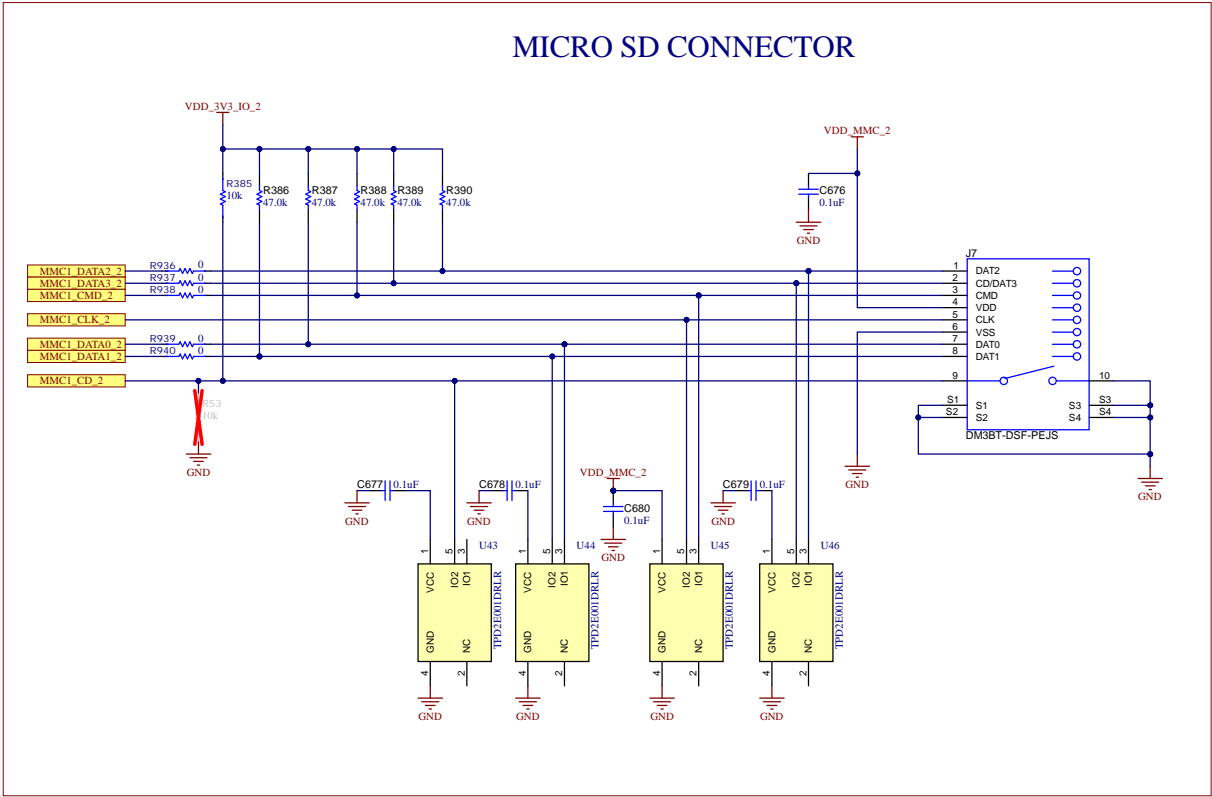
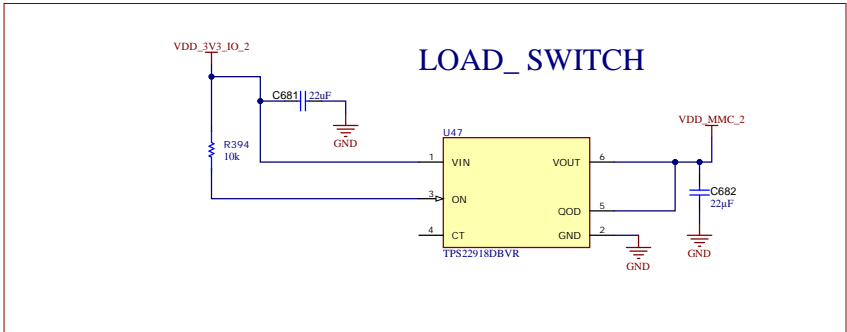
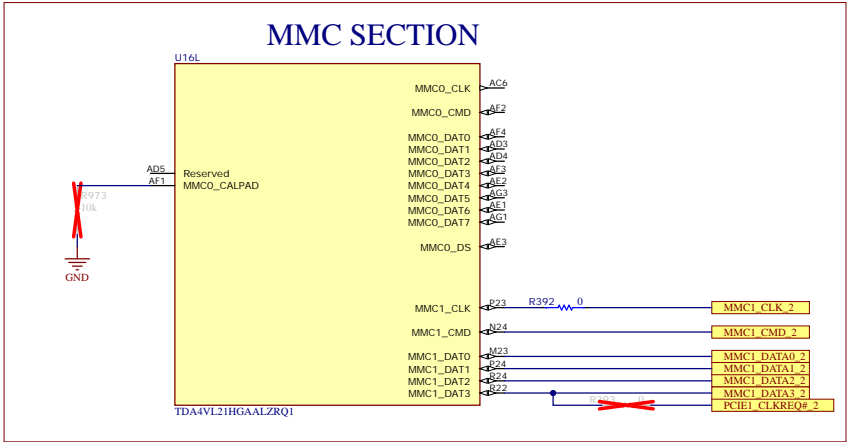


## SD CARD SECTION 1

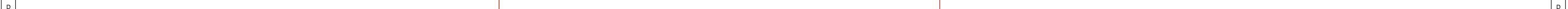




SD CARD SECTION 2

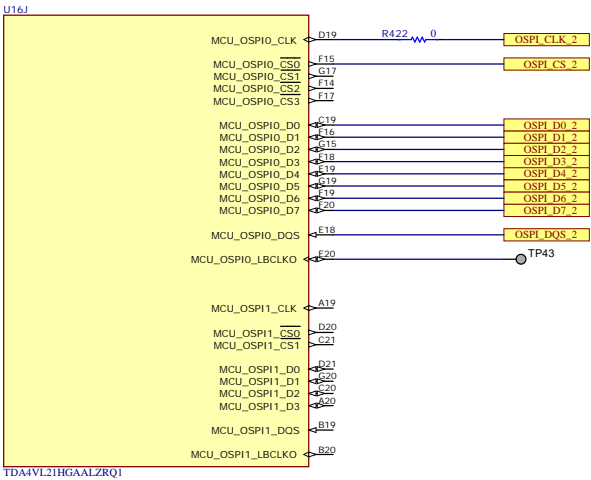


## PROCESSOR SECTION

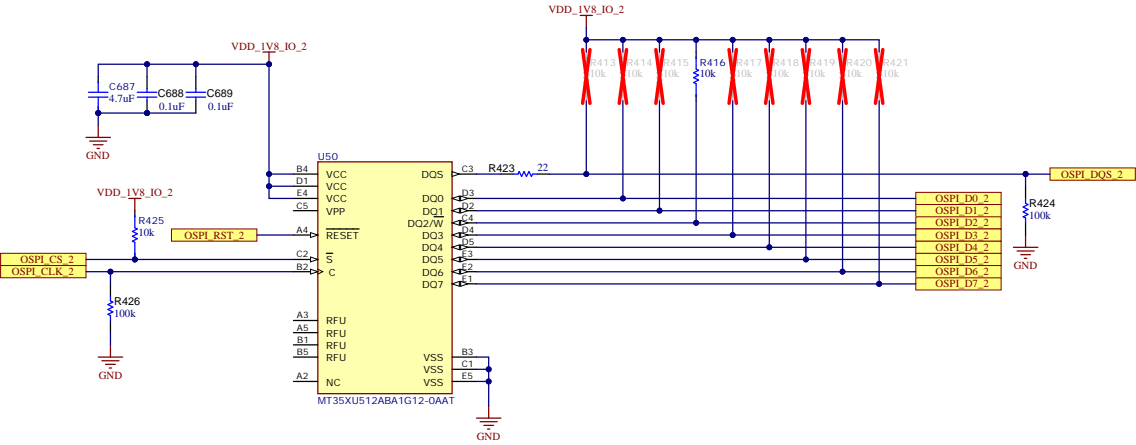
[illegible]

OSPI FLASH SECTION 2

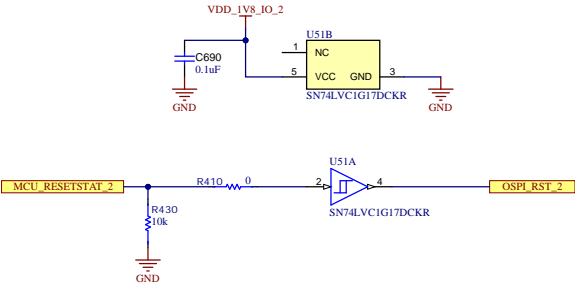
PROCESSOR SECTION



OSPI FLASH

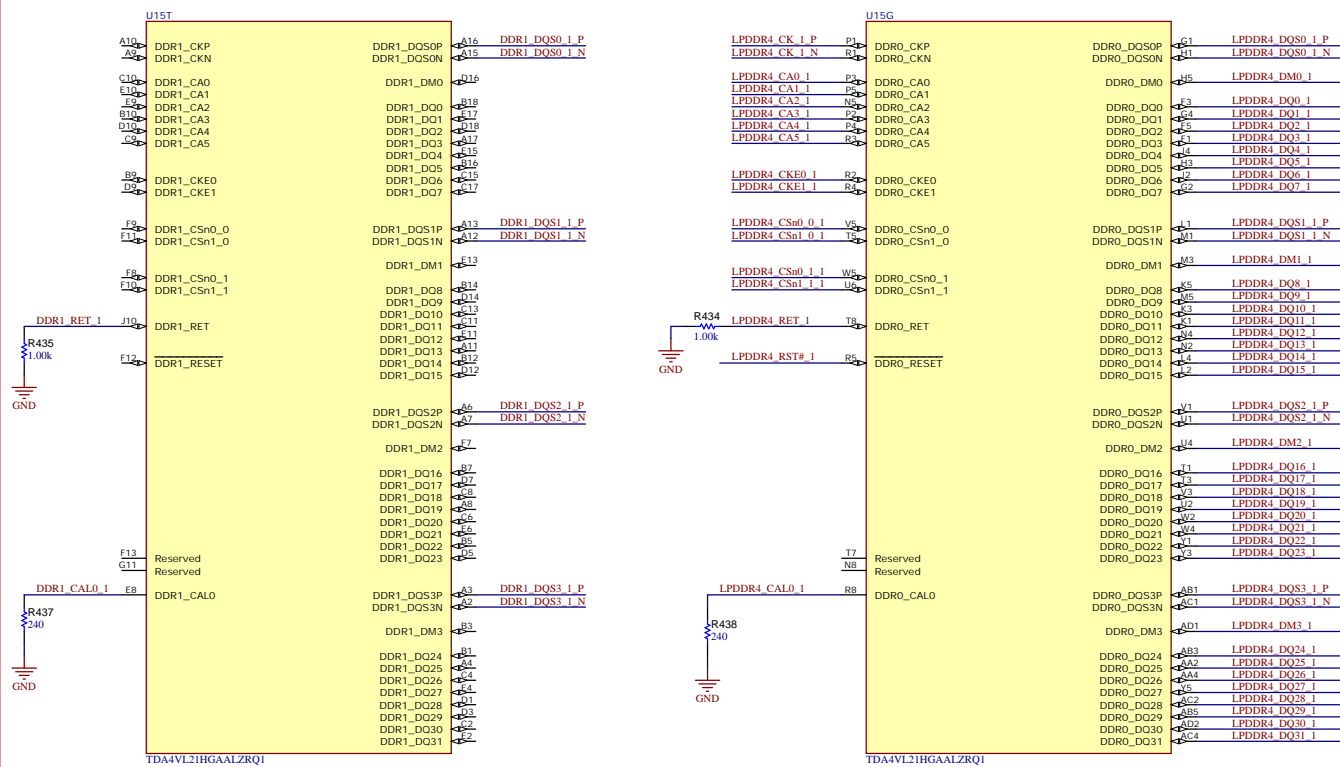


OSPI RESET

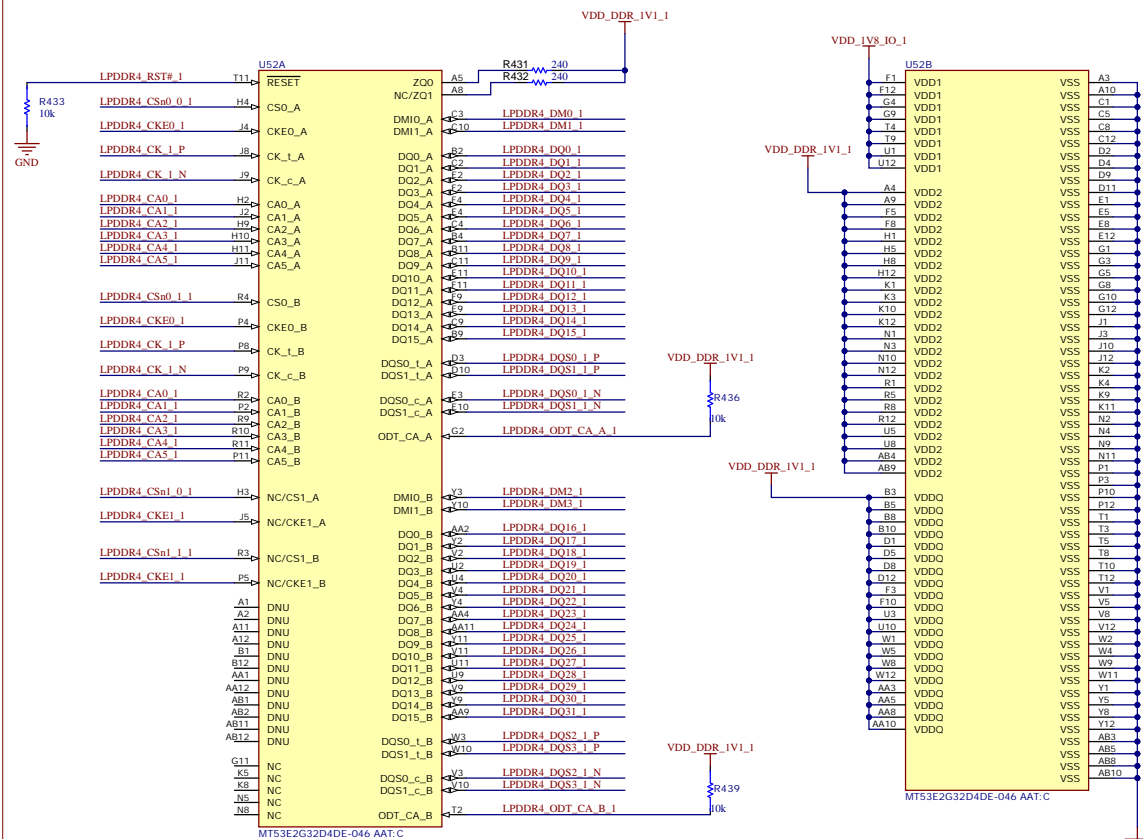


## LPDDR4 1

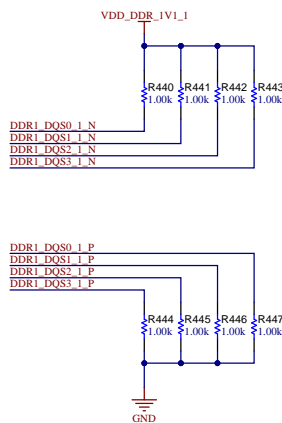
## PROCESSOR SECTION



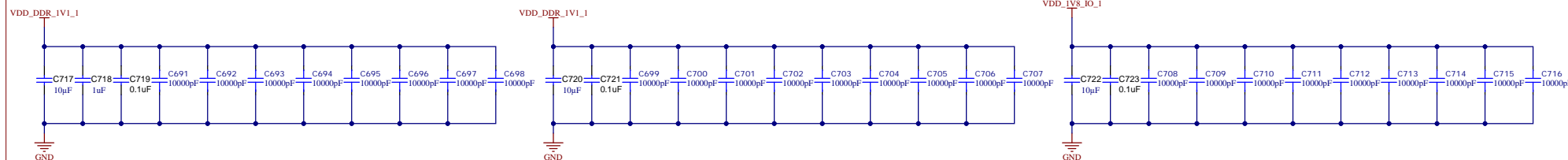
## LPDDR4 SECTION



## PULL UP & PULL DOWN RESISTORS

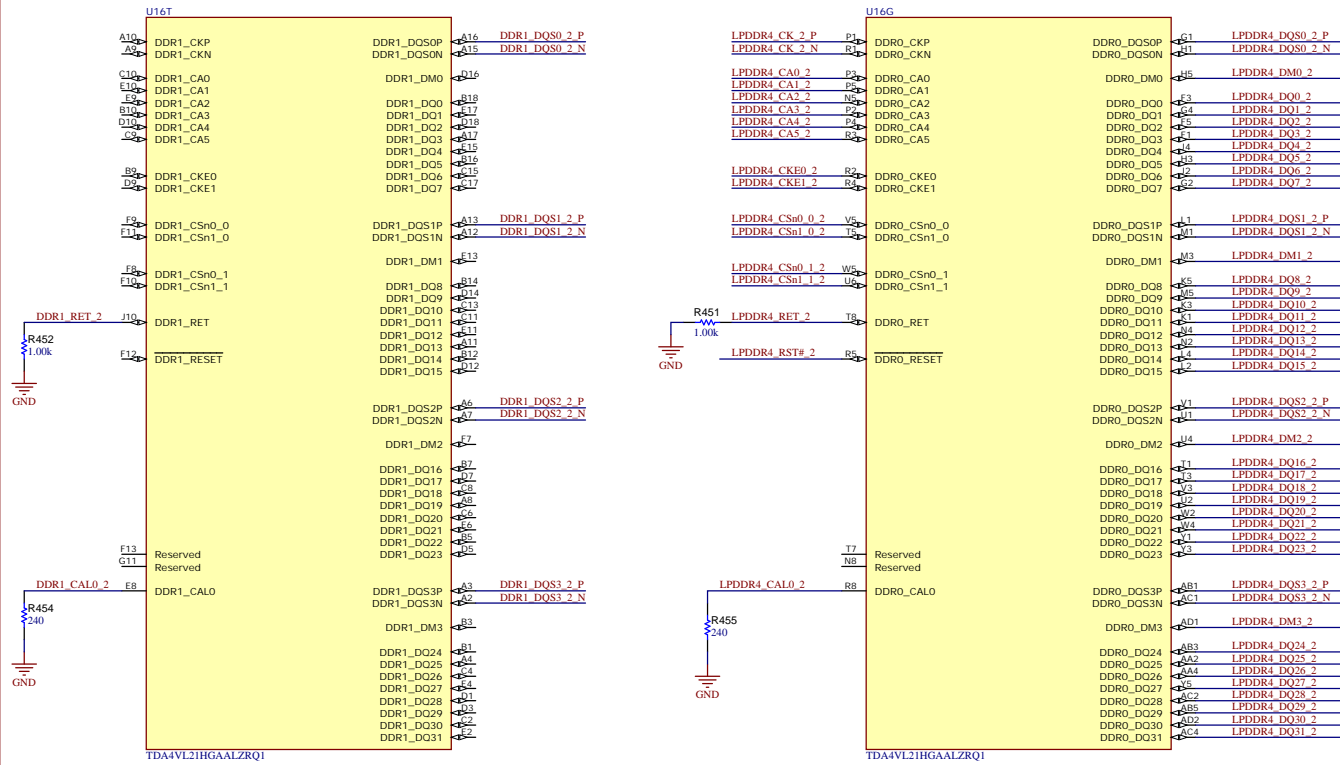


## DECAPS SECTION

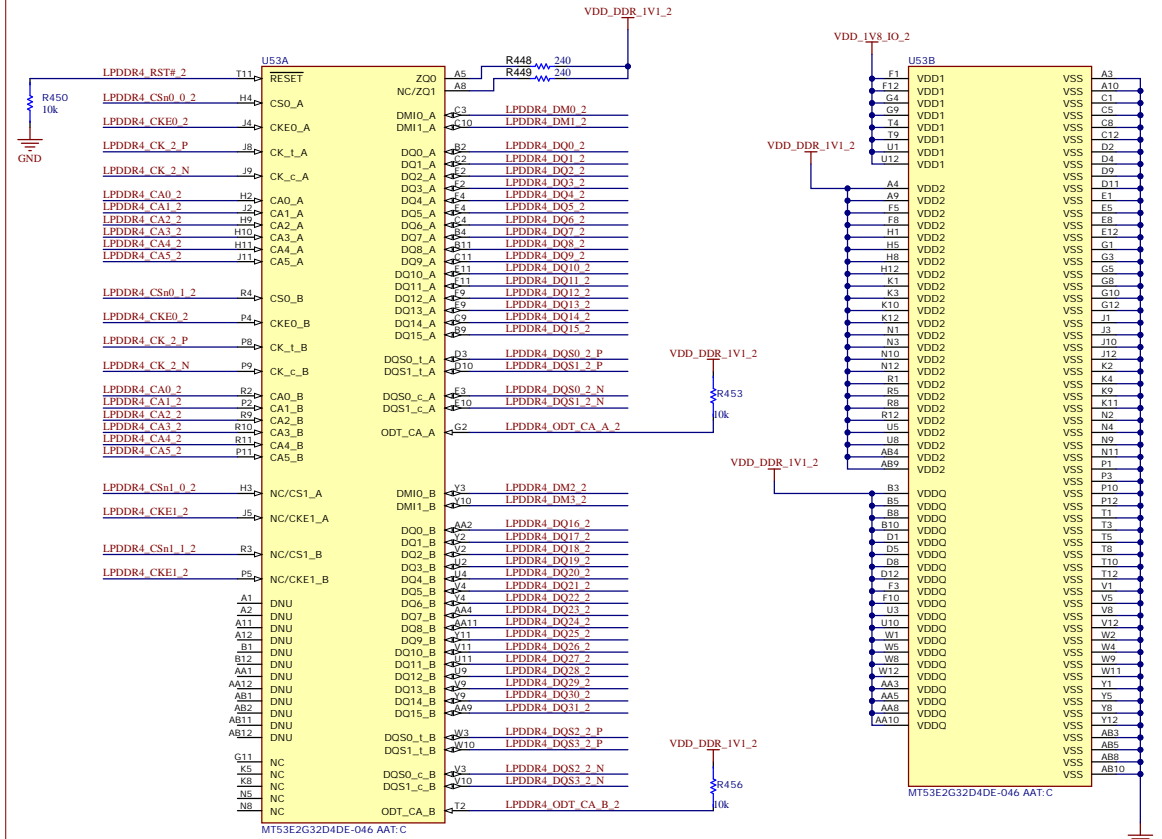


## LPDDR4 2

### PROCESSOR SECTION

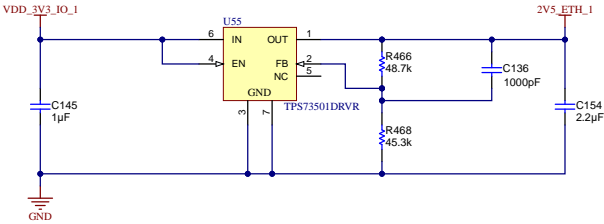


### LPDDR4 SECTION

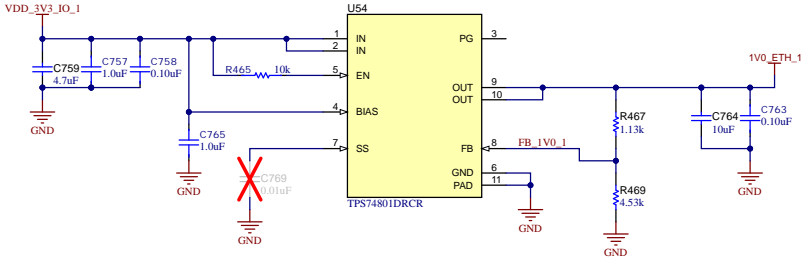


ETHERNET POWER 1

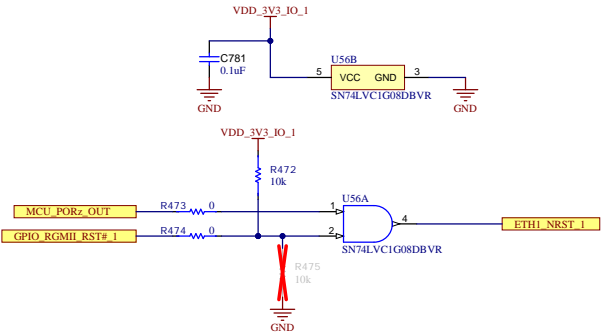
2V5 LDO



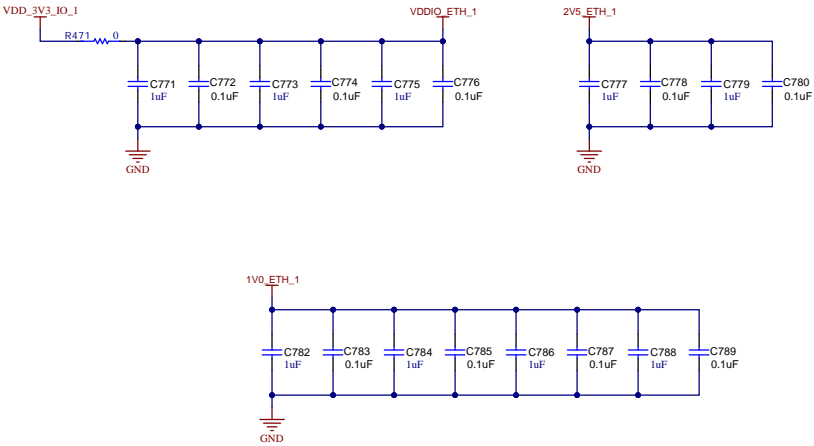
1V0 LDO



ETHERNET RESET

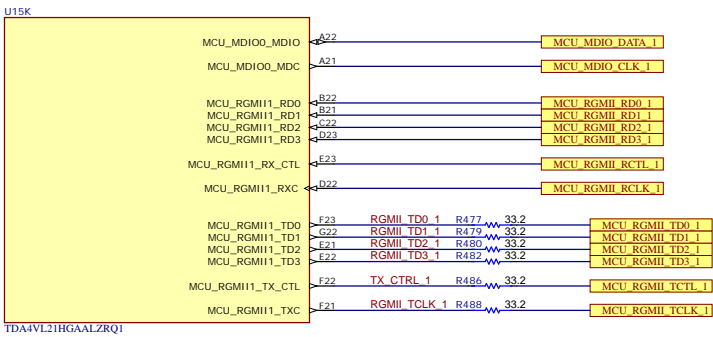


DECOUPLING CAPS

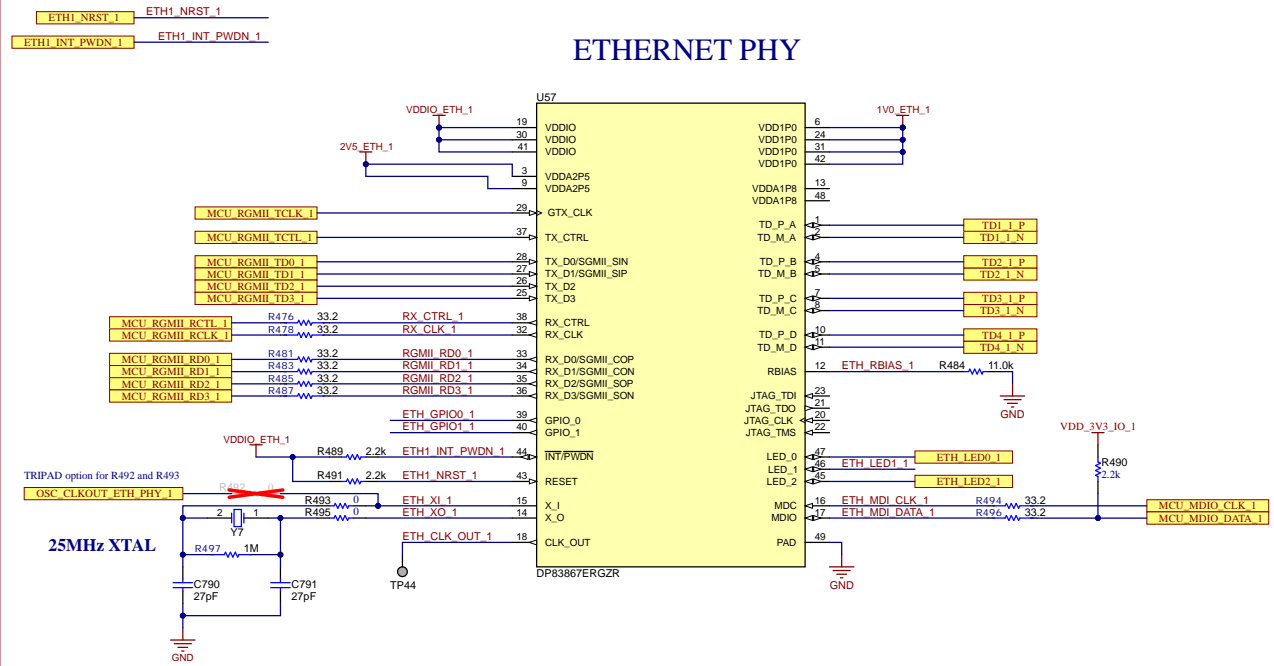


ETHERNET PHY SECTION 1

ETHERNET SECTION

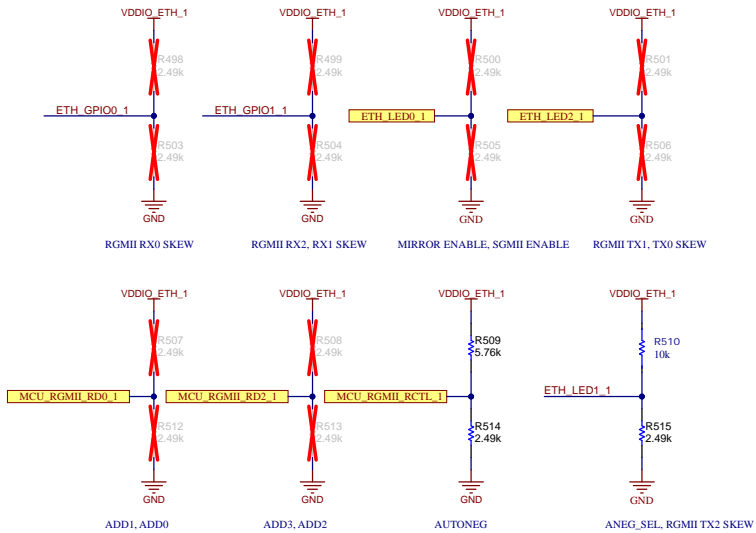


ETHERNET PHY



BOOTSTRAP CONFIGURATION PINS

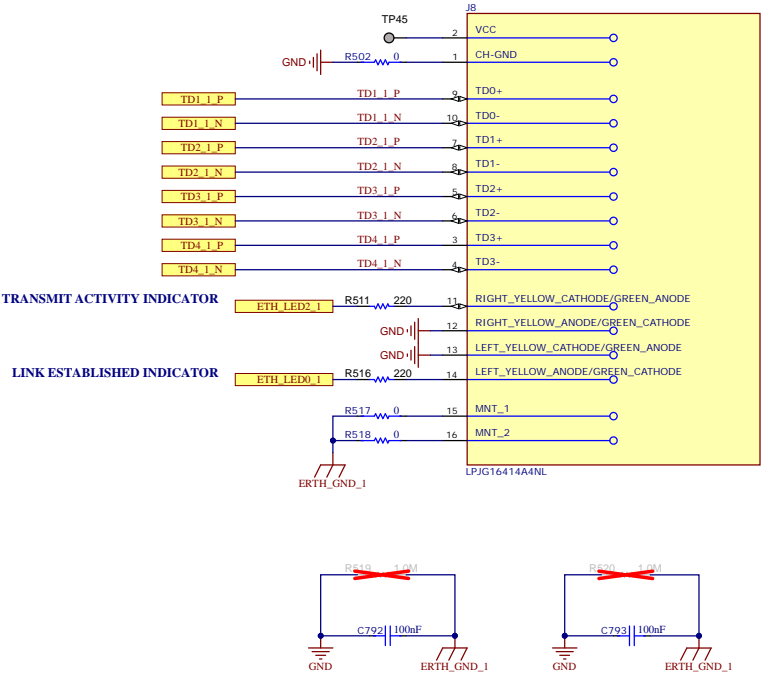
Resistor Values must be changed to change Modes, refer to datasheet for proper values



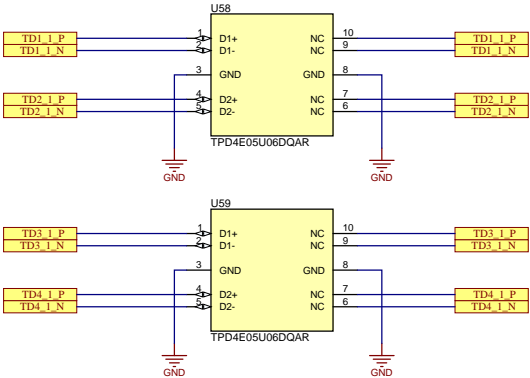
DEFAULT CONFIGURATION:  
ADD1, ADD0 = 0  
ADD3, ADD2 = 0  
AUTONEG = 1  
RGMII RX0 SKEW = 0  
RGMII RX2, RX1 SKEW = 0, 0  
RGMII TX1, TX0 SKEW = 0, 0  
ANEG\_SEL, RGMII TX2 SKEW = 0, 1  
MIRROR ENABLE, SGMII ENABLE = 0, 0

ETHERNET MAGNETICS

RJ45 WITH MAGJACK



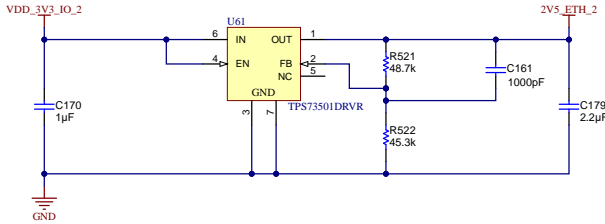
ETHERNET ESD PROTECTION



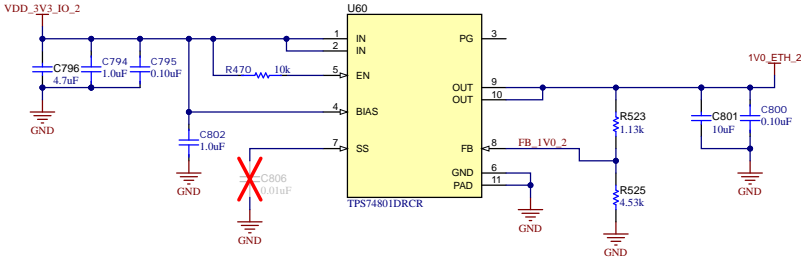


ETHERNET POWER 2

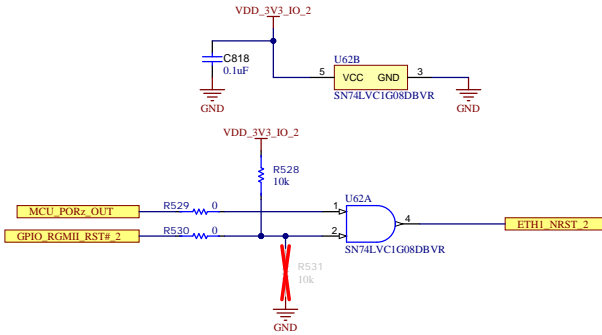
2V5 LDO



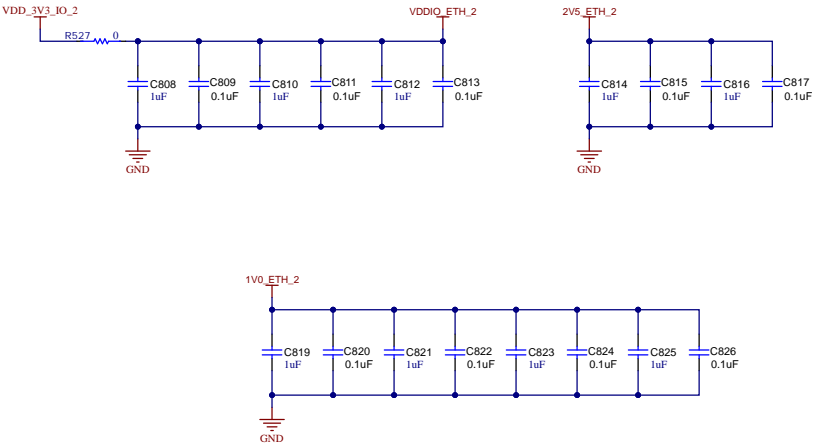
1V0 LDO



ETHERNET RESET

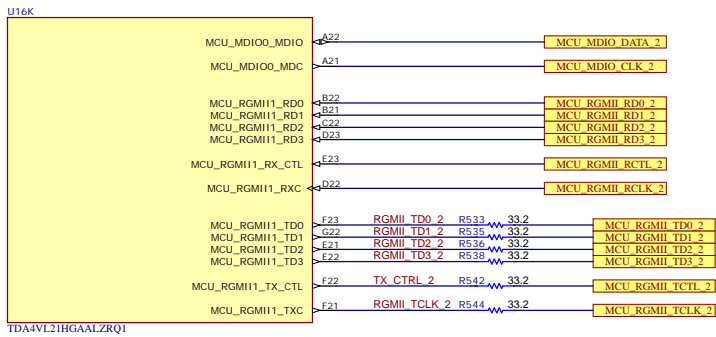


DECOUPLING CAPS

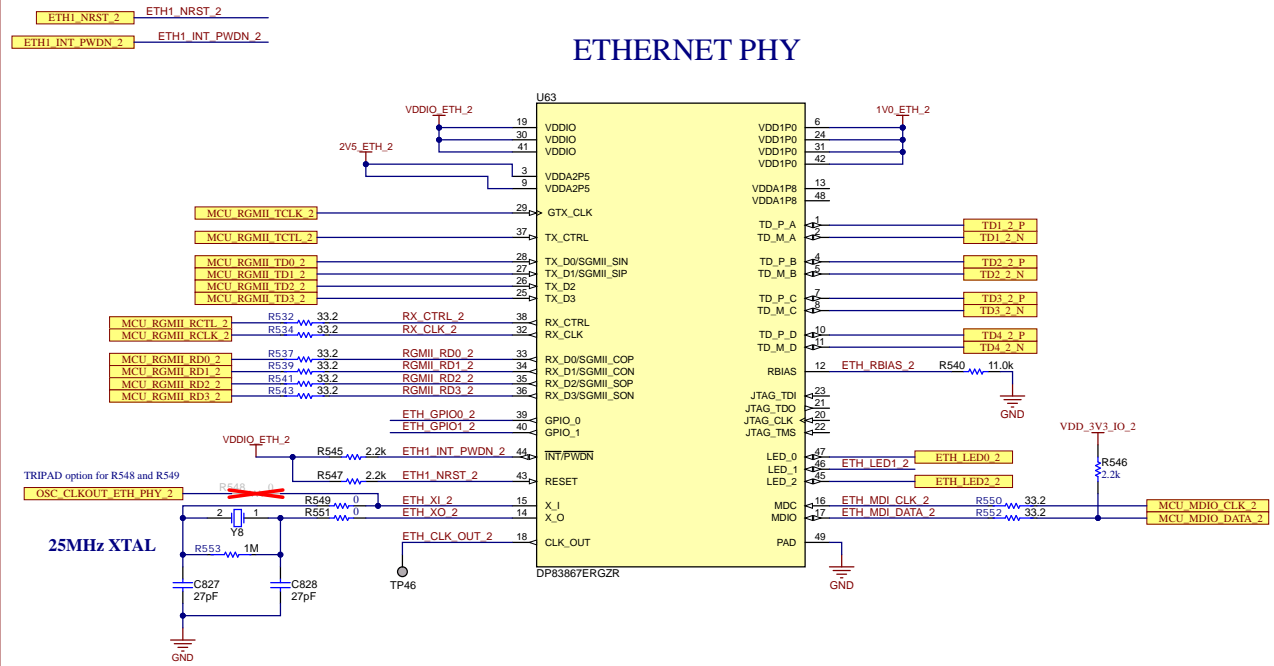


ETHERNET PHY SECTION 2

ETHERNET SECTION

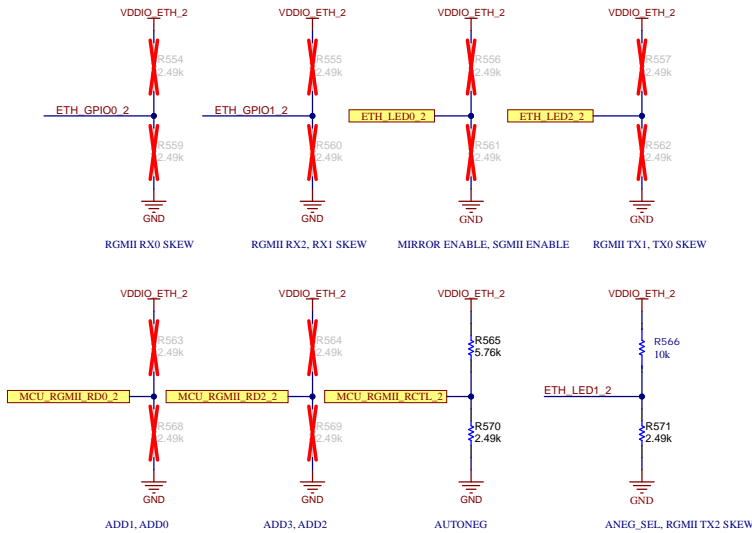


ETHERNET PHY



BOOTSTRAP CONFIGURATION PINS

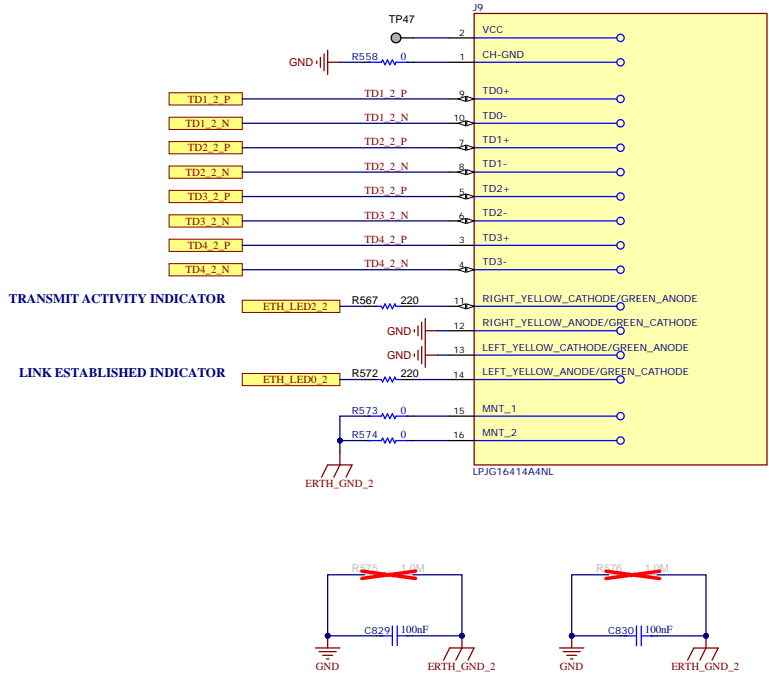
Resistor Values must be changed to change Modes, refer to datasheet for proper values



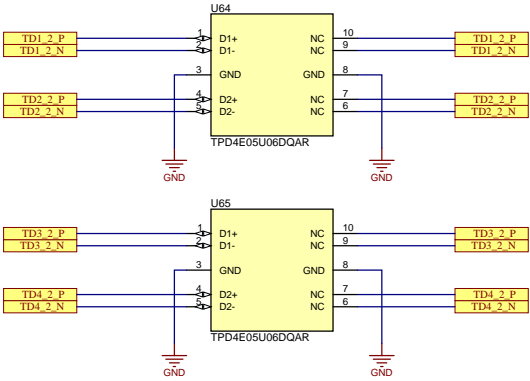
DEFAULT CONFIGURATION:  
ADD1, ADD0 = 0  
ADD3, ADD2 = 0  
AUTONEG = 1  
RGMII RX0 SKEW = 0  
RGMII RX2, RX1 SKEW = 0, 0  
RGMII TX1, TX0 SKEW = 0, 0  
ANEG\_SEL, RGMII TX2 SKEW = 0, 1  
MIRROR ENABLE, SGMII ENABLE = 0, 0

ETHERNET MAGNETICS

RJ45 WITH MAGJACK

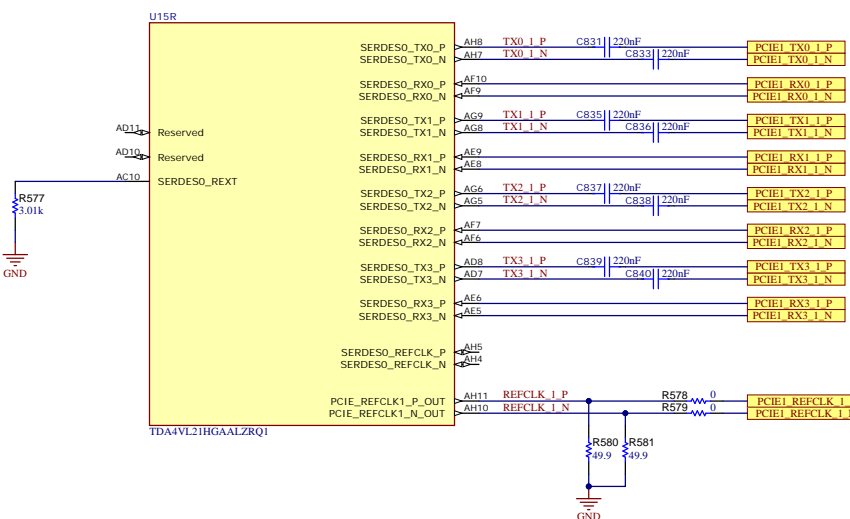


ETHERNET ESD PROTECTION

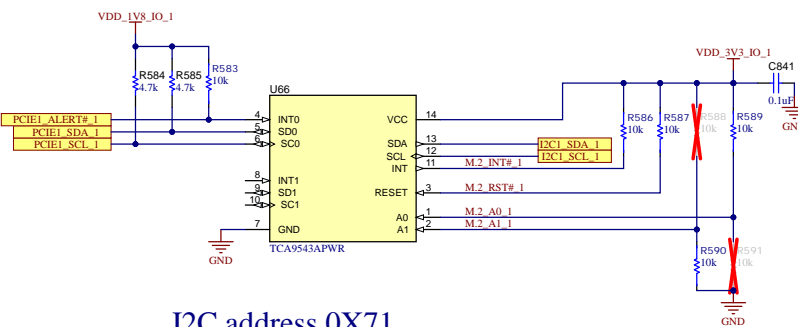


## PCIe M.2 CONNECTOR 1

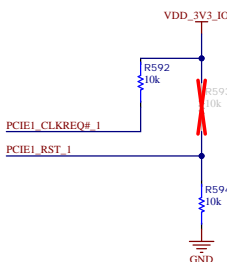
## M.2 PCIE SECTION



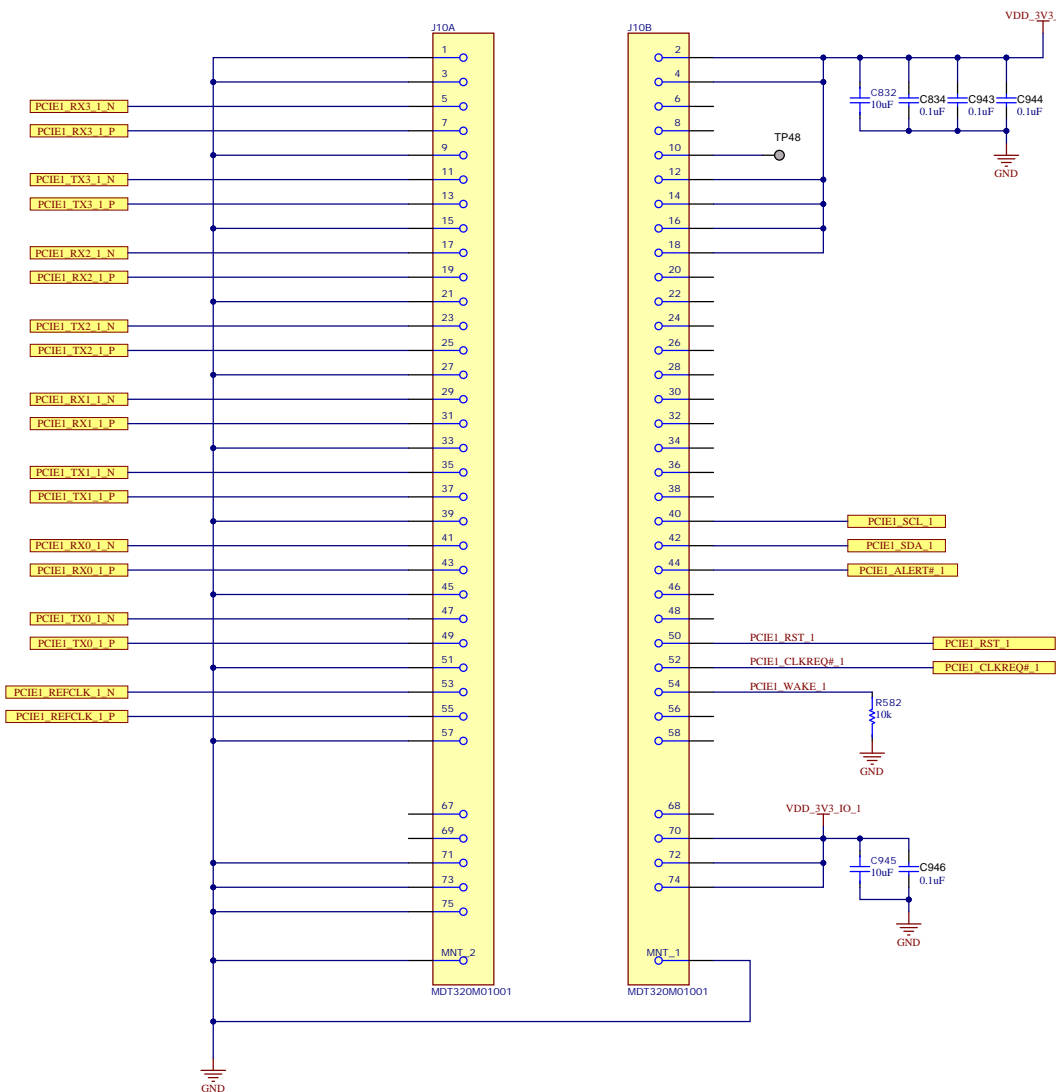
## LEVEL TRANSLATOR



## PULL UP and PULL DOWN OPTIONS

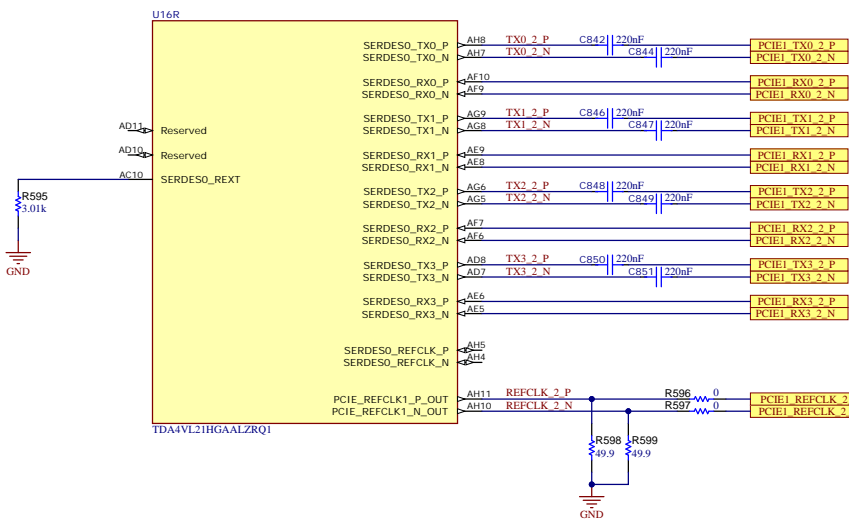


## M.2 PCIE CONNECTOR

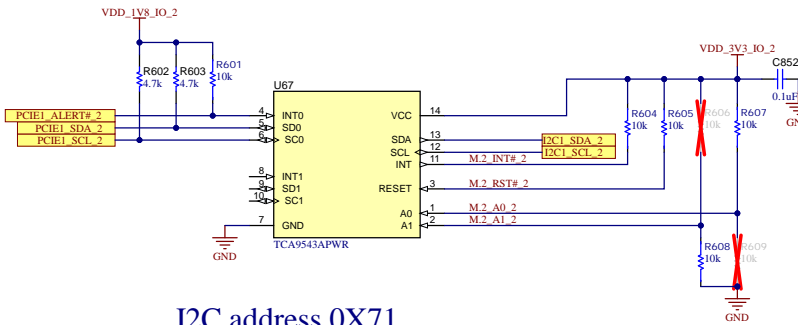


## PCIe M.2 CONNECTOR 2

## M.2 PCIE SECTION

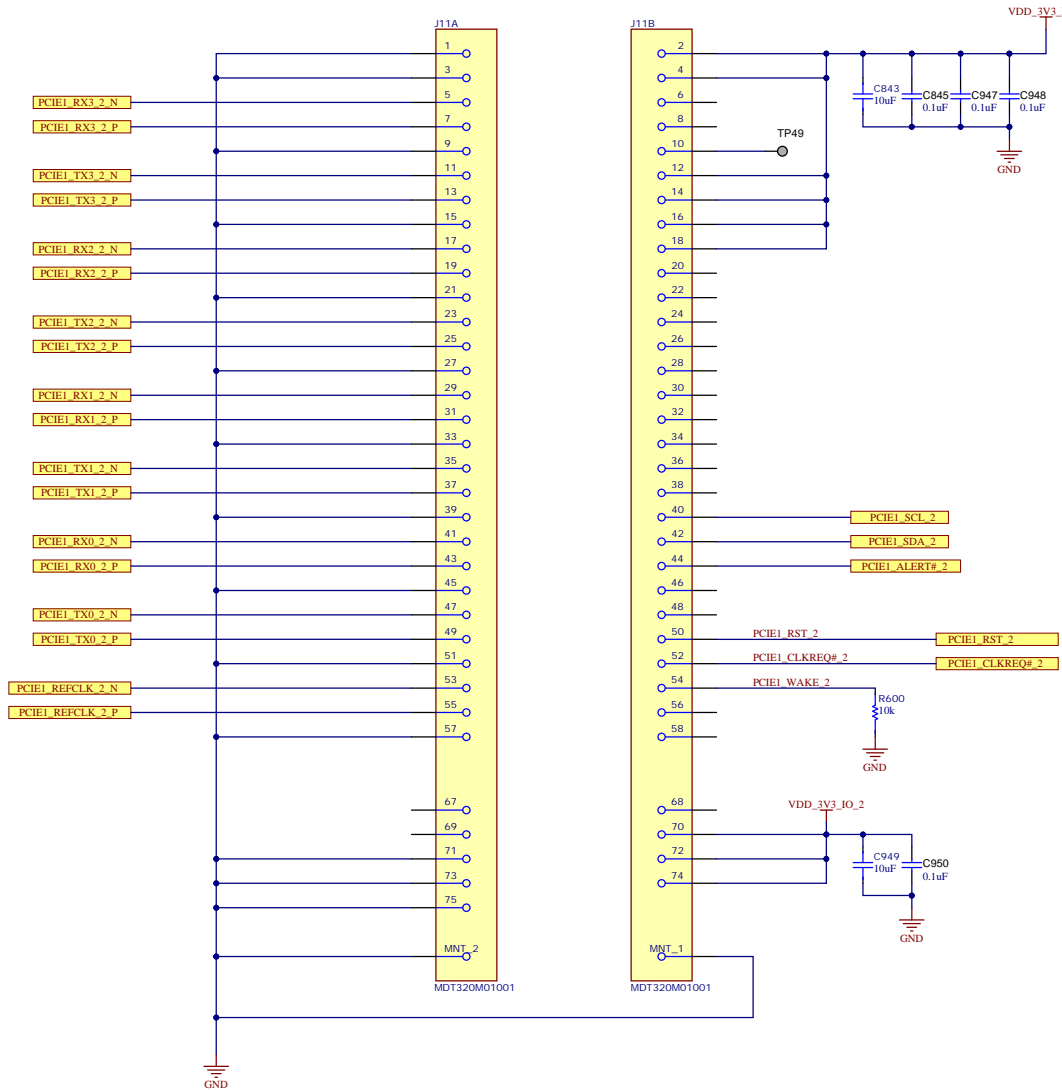


## LEVEL TRANSLATOR

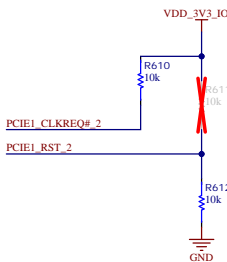


I2C address 0X71

## M.2 PCIE CONNECTOR

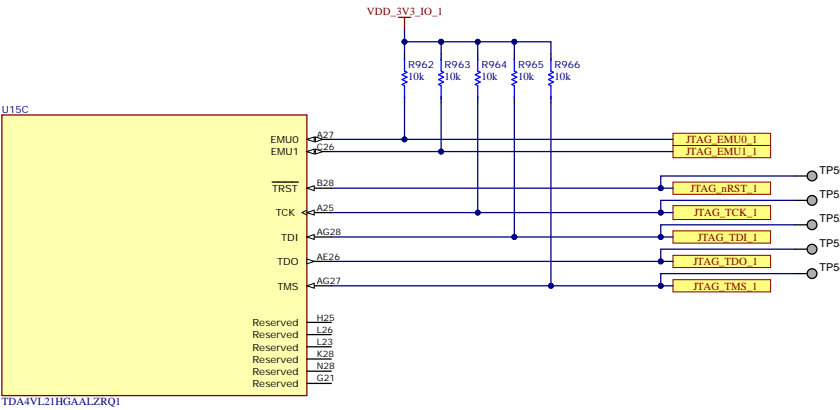


## PULL UP and PULL DOWN OPTIONS

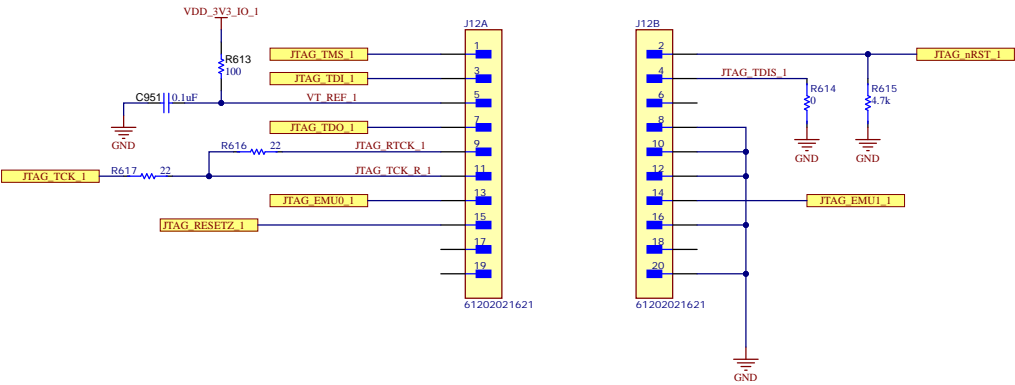


JTAG & DEBUG CONNECTOR 1

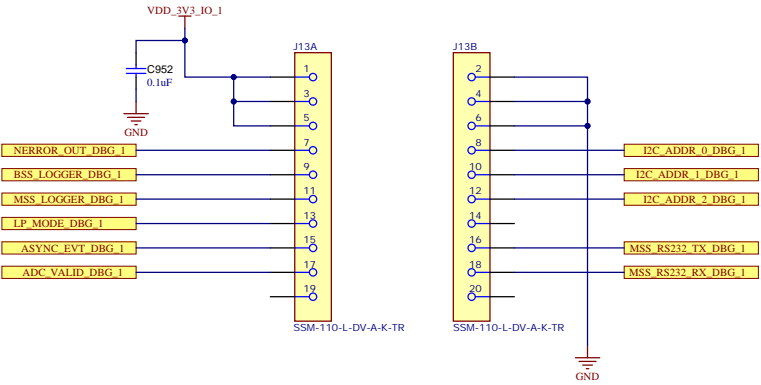
JTAG SECTION



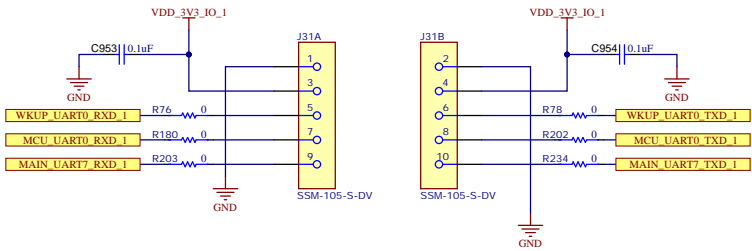
JTAG CONNECTOR



RADAR A DEBUG CONNECTOR

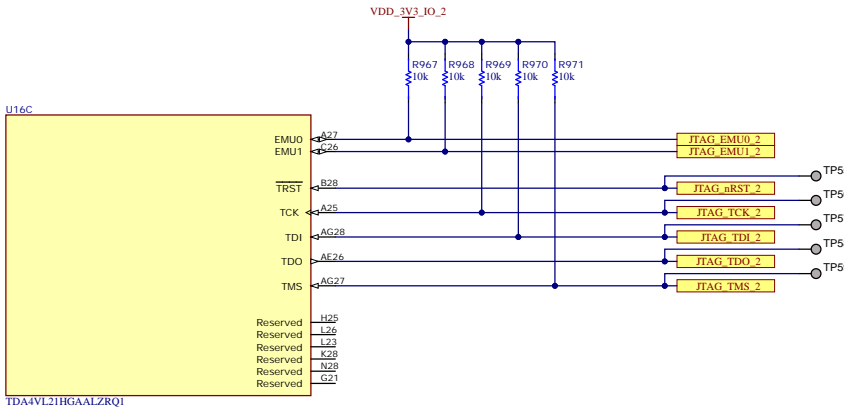


TDA A DEBUG CONNECTOR

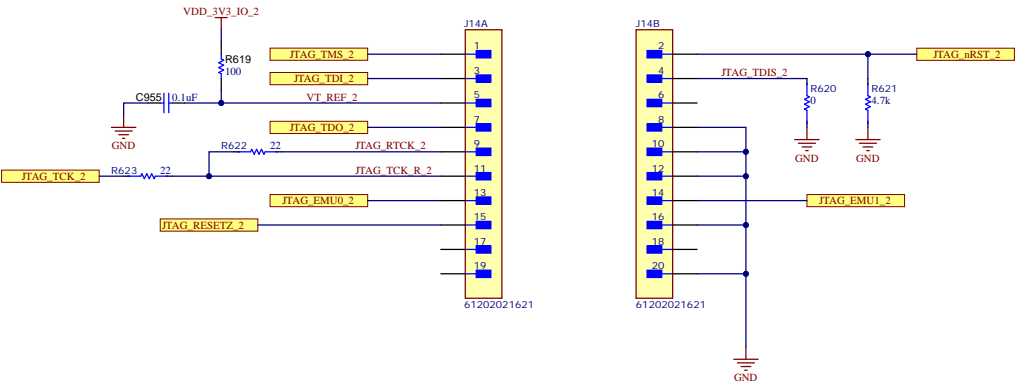


JTAG & DEBUG CONNECTOR 2

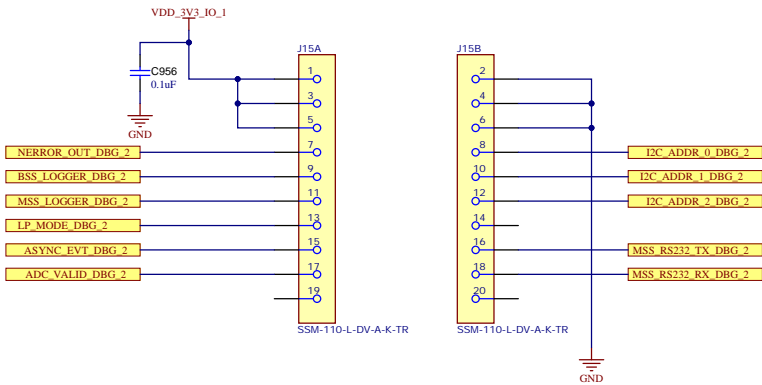
JTAG SECTION



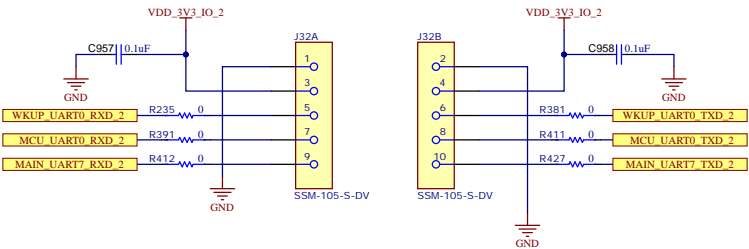
JTAG CONNECTOR



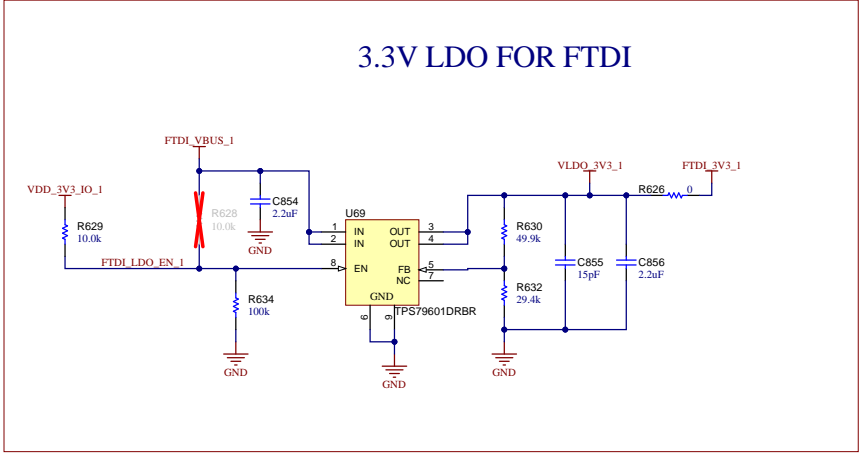
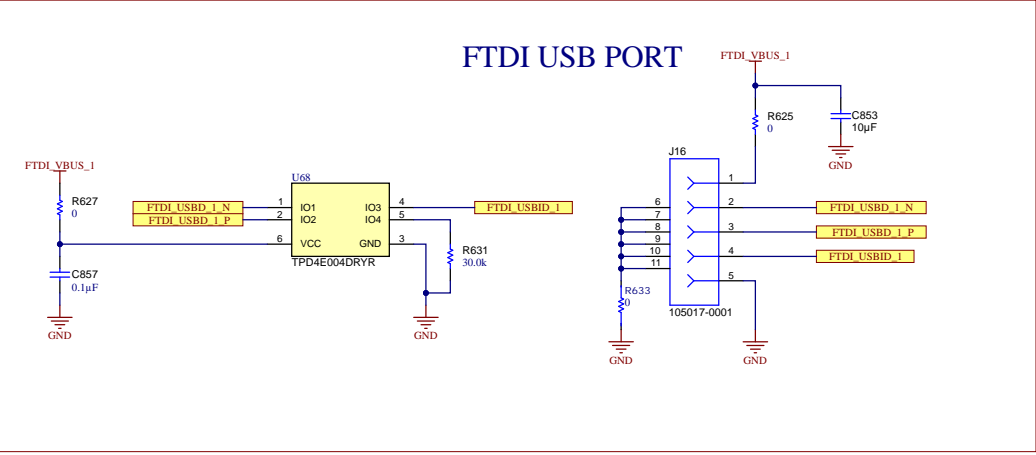
RADAR B DEBUG CONNECTOR



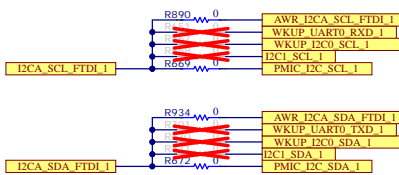
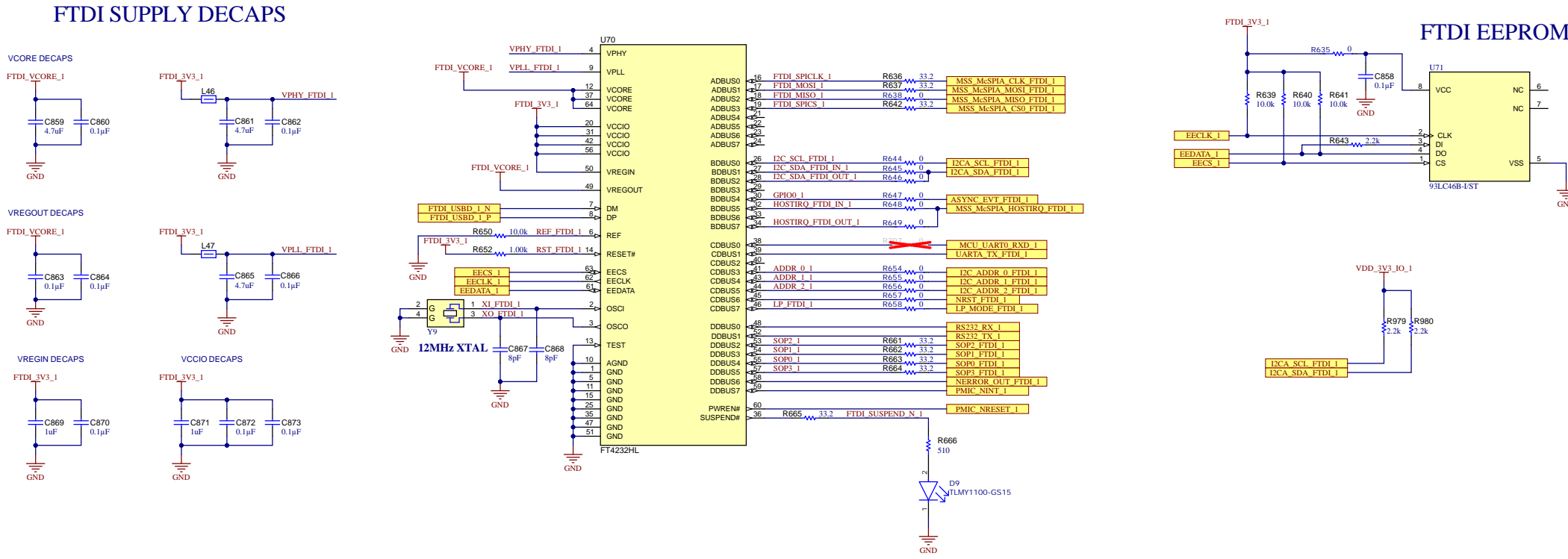
TDA B DEBUG CONNECTOR



## FTDI SECTION 1



## FTDI SECTION

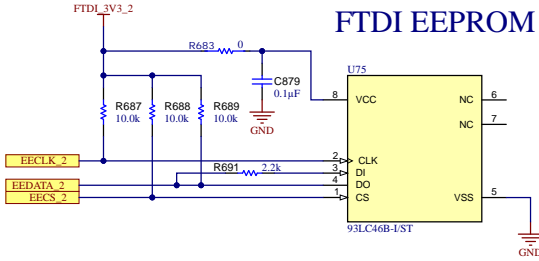




## FTDI SECTION 2



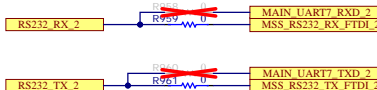
## FTDI SECTION



## CHANNEL B MUX OPTIONS

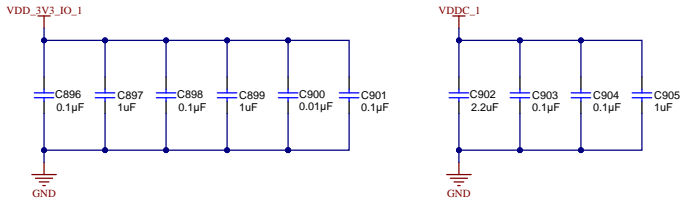


## CHANNEL D MUX OPTIONS

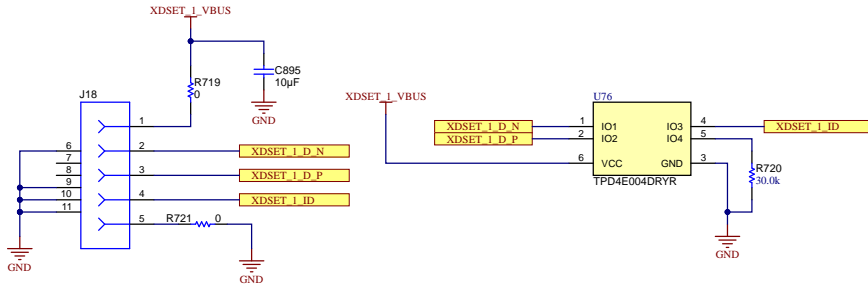


## XDS110 SECTION 1

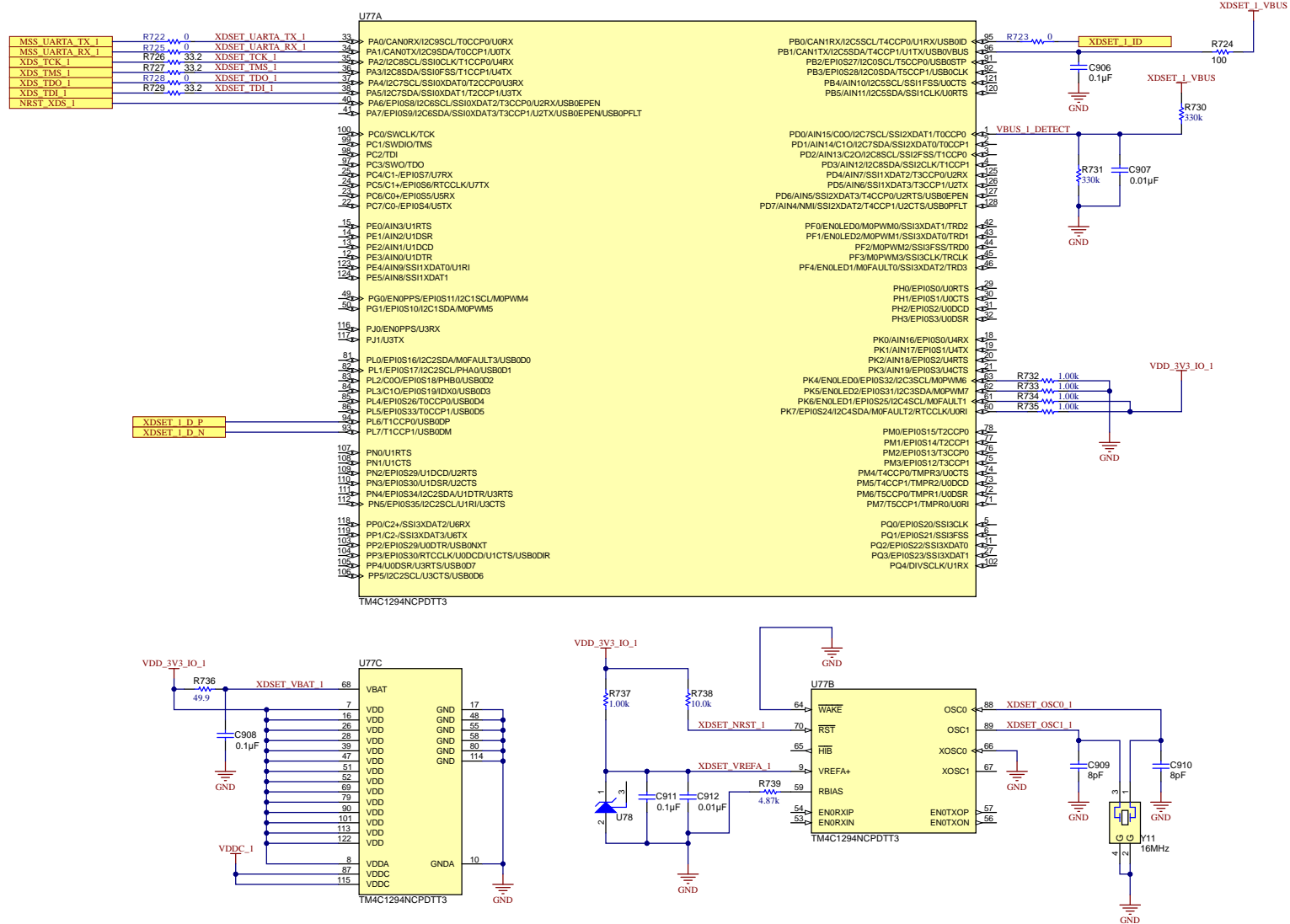
## XDS110 DECOUPLING CAPS



## XDS110 USB PORT

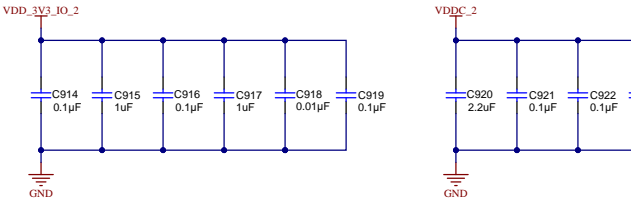


## XDS110 SECTION

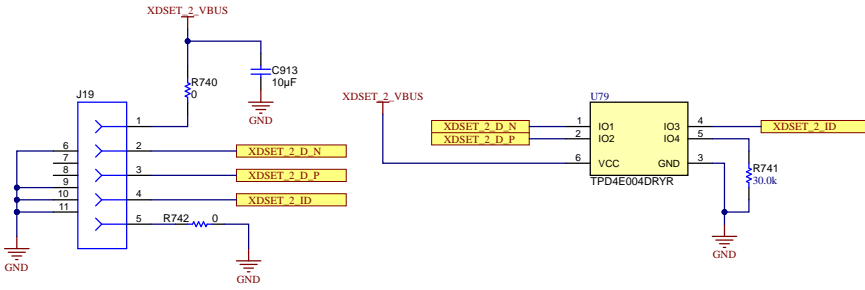


## XDS110 SECTION 2

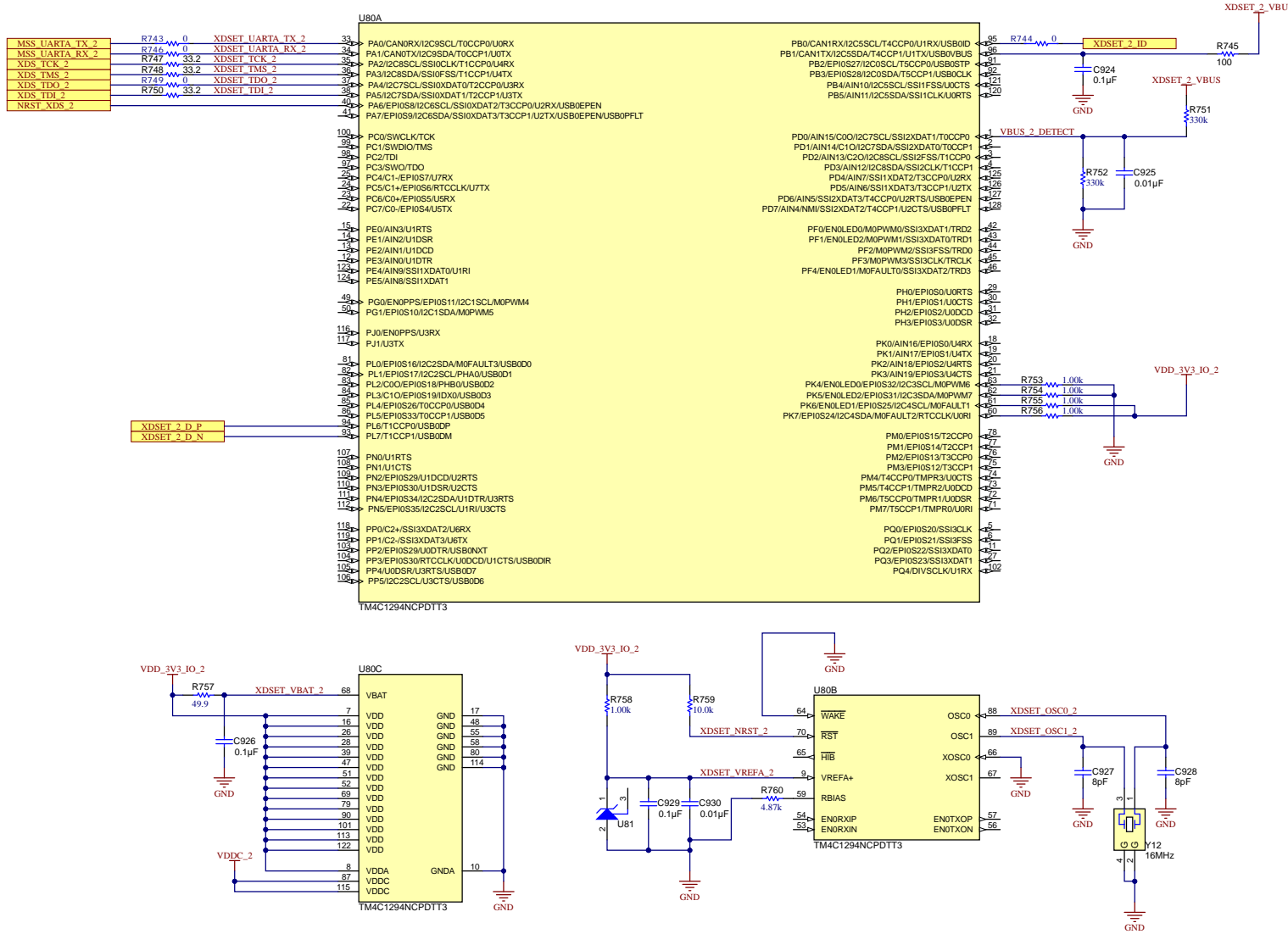
## XDS110 DECOUPLING CAPS



## XDS110 USB PORT

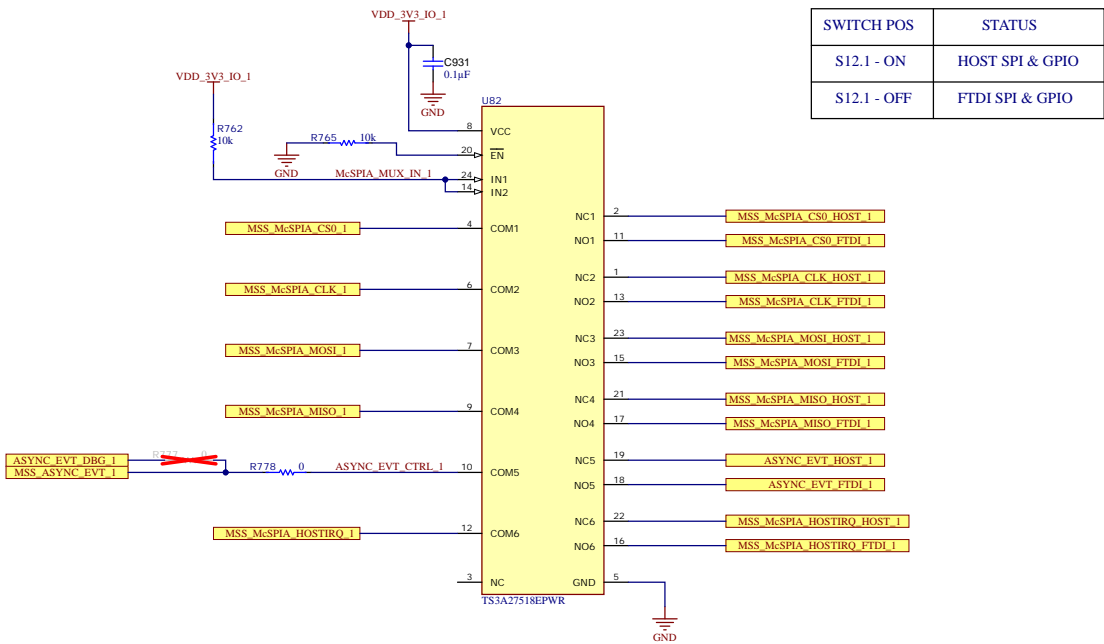


## XDS110 SECTION

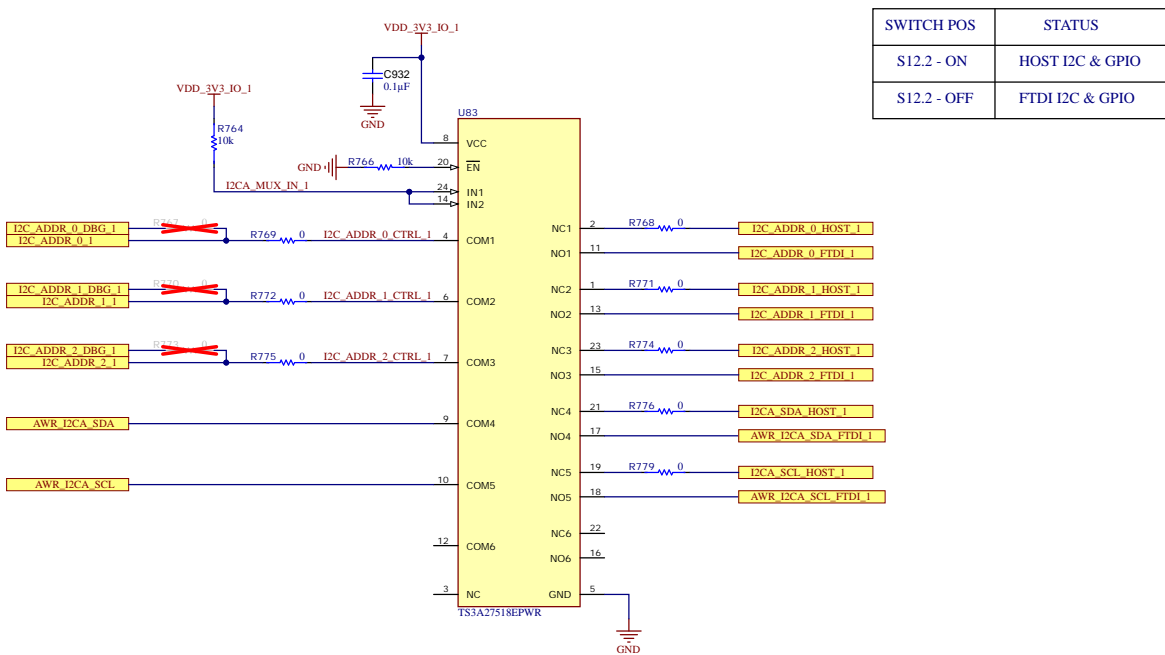


MUX SECTION 1

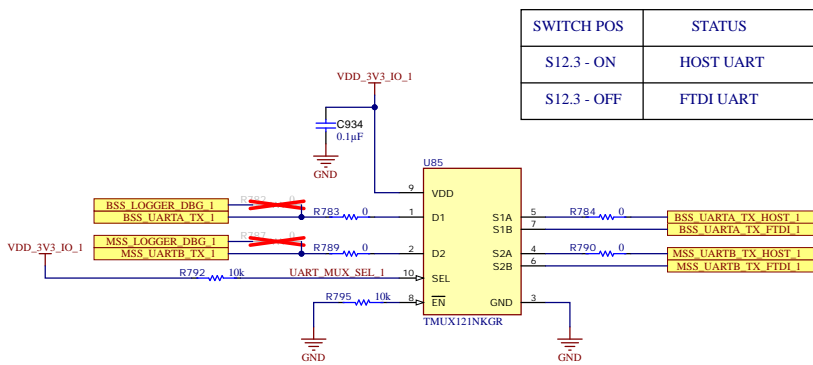
SPI\_MUX(FTDI or HOST)



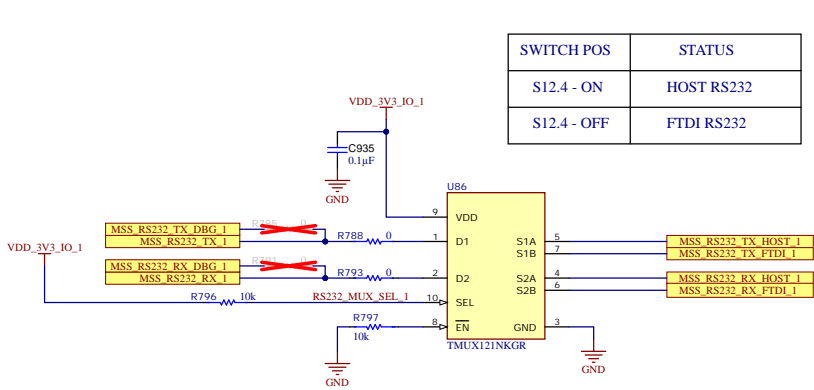
I2CA\_MUX(FTDI or HOST)



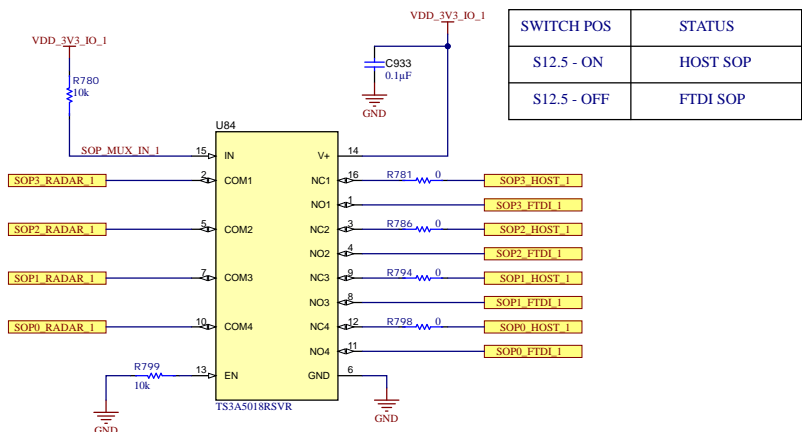
UART\_MUX(FTDI or HOST)



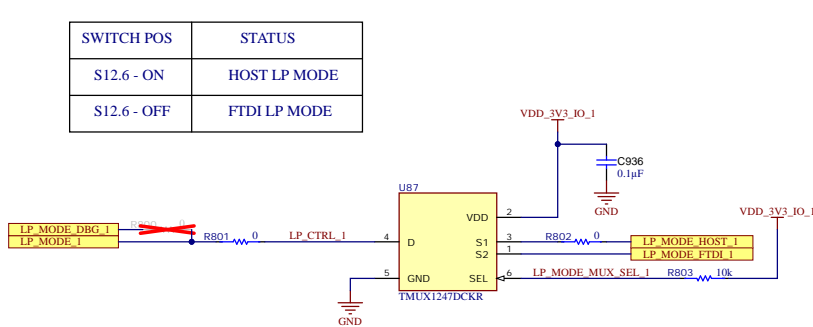
RS232\_MUX(FTDI or HOST)



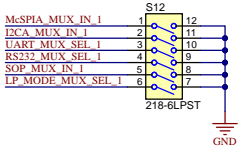
SOP\_MUX(FTDI or HOST)



LP\_MODE\_MUX(FTDI or HOST)

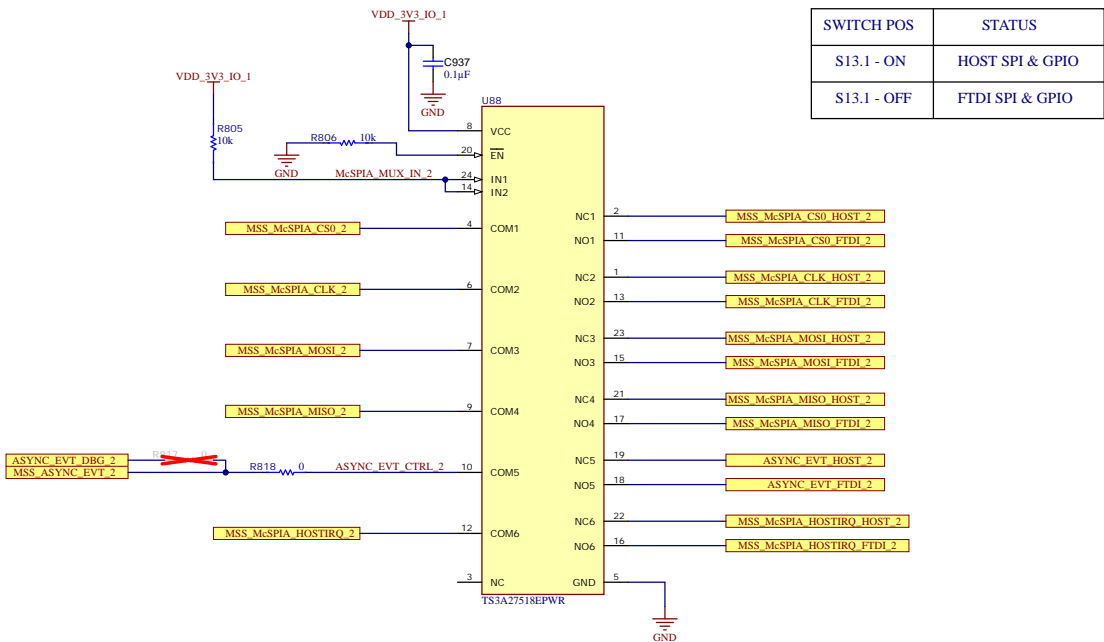


MUX SELECTION SWITCH

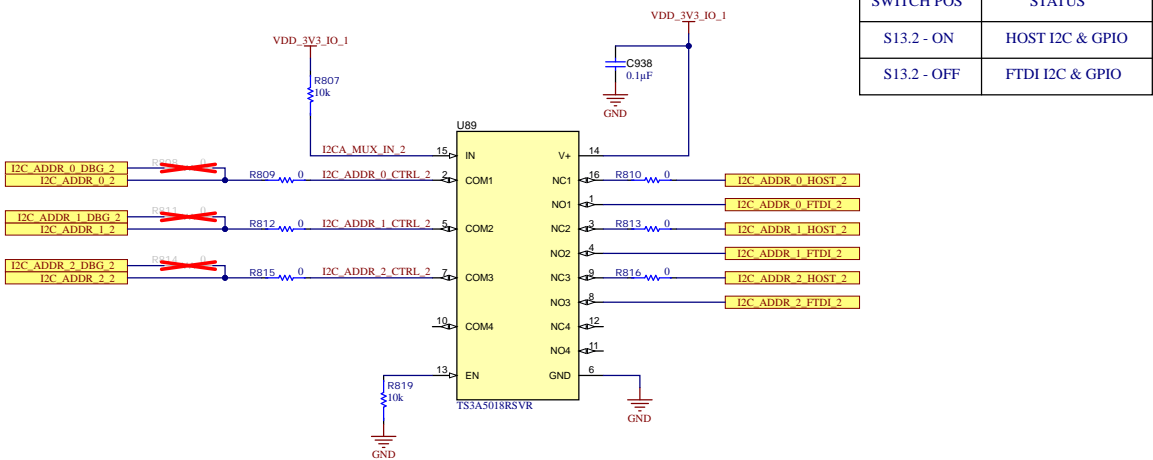


MUX SECTION 2

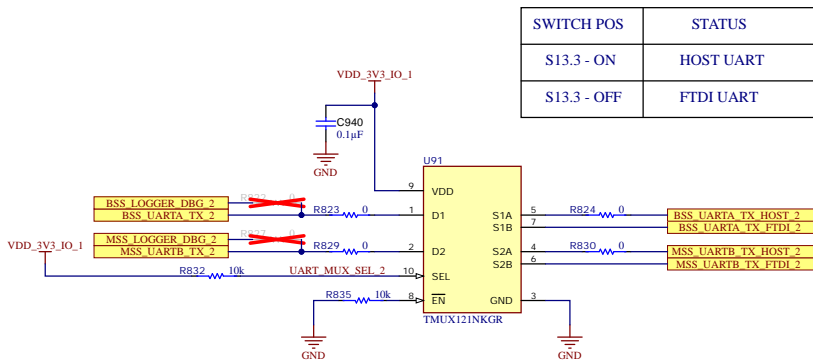
SPI\_MUX(FTDI or HOST)



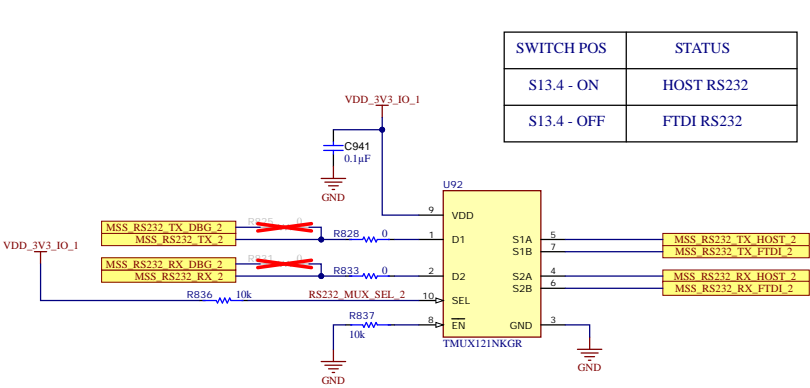
I2CA\_MUX(FTDI or HOST)



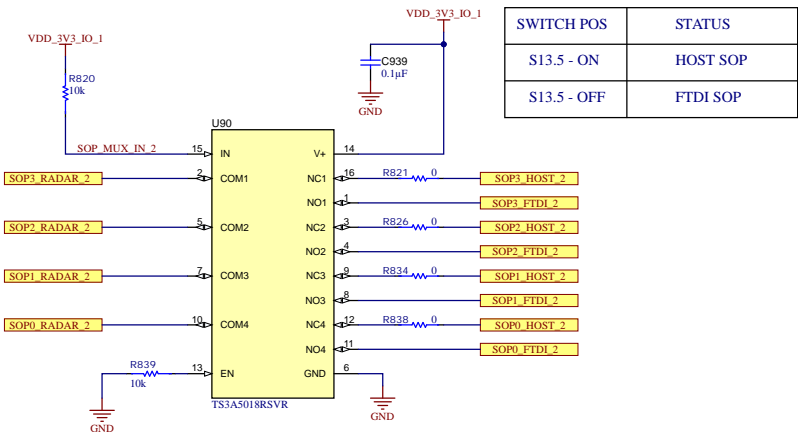
UART\_MUX(FTDI or HOST)



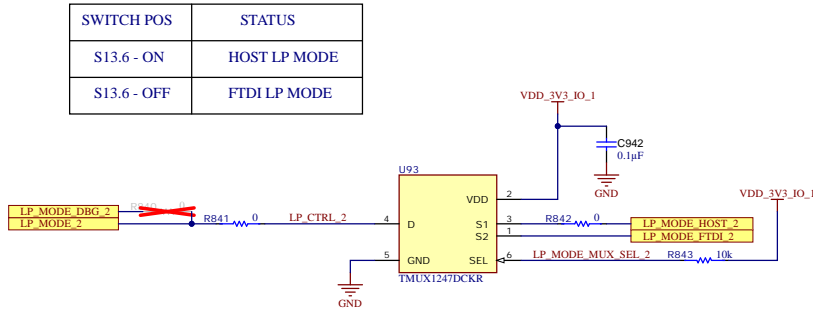
RS232\_MUX(FTDI or HOST)



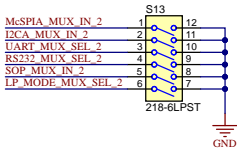
SOP\_MUX(FTDI or HOST)



LP\_MODE\_MUX(FTDI or HOST)

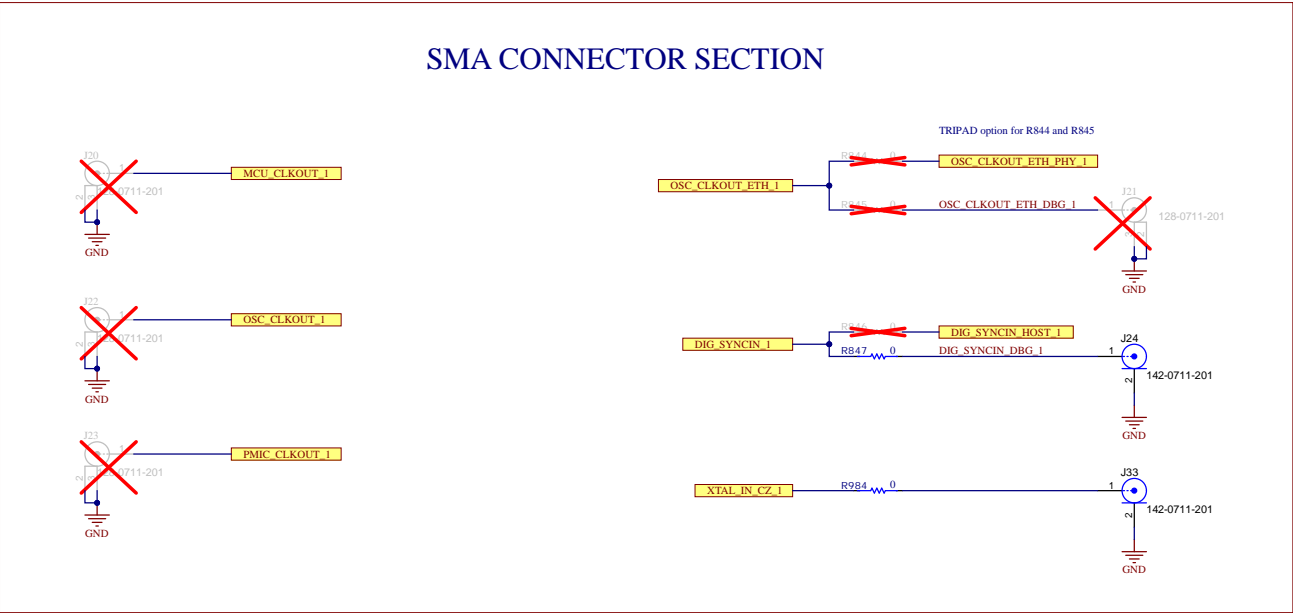


MUX SELECTION SWITCH

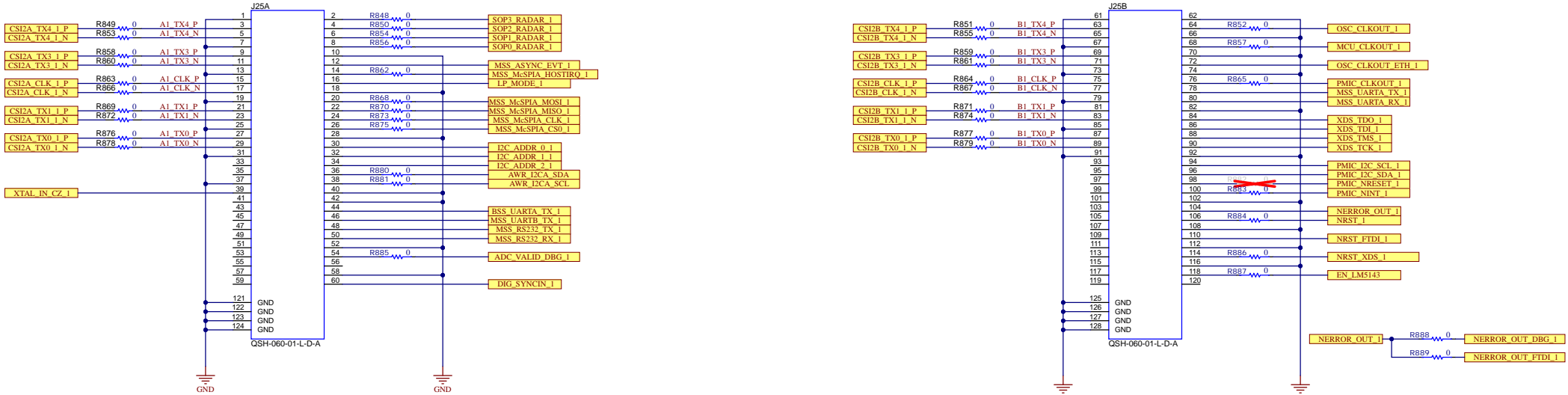


120 PIN CONNECTOR SECTION 1

SMA CONNECTOR SECTION

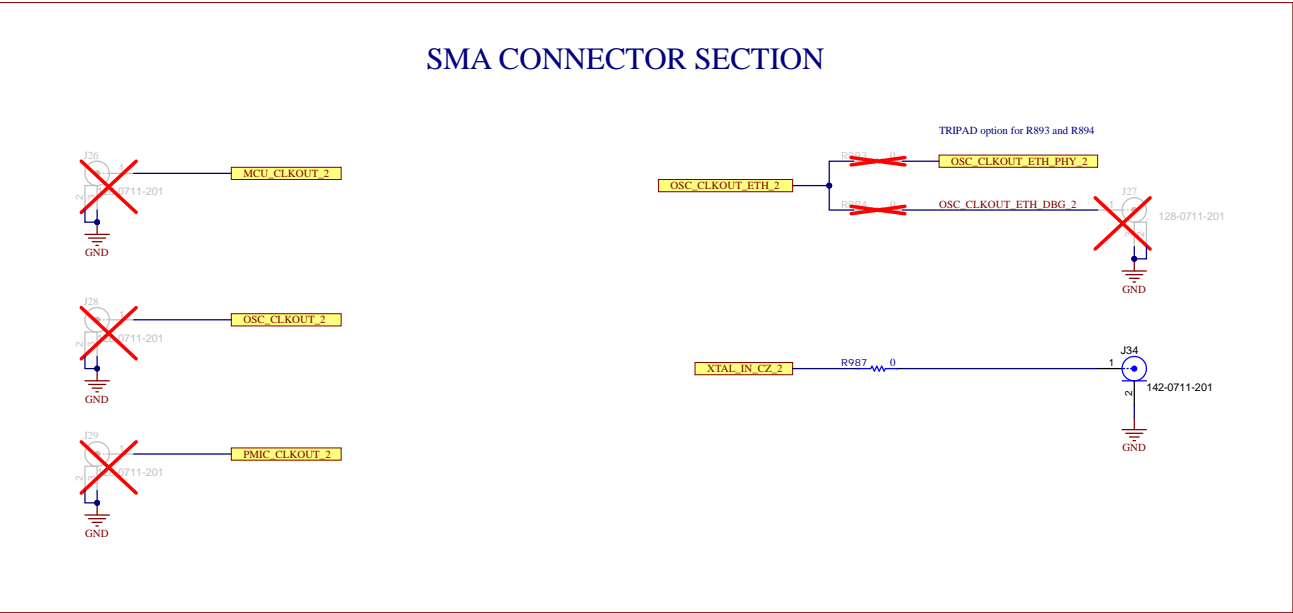


120 PIN CONNECTOR SECTION



120 PIN CONNECTOR SECTION 2

SMA CONNECTOR SECTION



120 PIN CONNECTOR SECTION

