Application Note

Mitigating UART Receiver Glitches While Switching Modes on RS-485 Transceivers

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ABSTRACT

When the receiver line “R” is pulled high on a RS-485 transceiver, a transition from transmitting to receiving can initiate a start condition in UART. When a half-duplex transceiver is switched from transmitting to receiving, the R line can experience a temporary voltage drop. The voltage drop on the R line can cause an unexpected start bit, generating a communication error. This application note explores the cause behind this false start condition and how to remove the false start.

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Trademarks

1 Introduction

RS-485 is a long-distance differential interface that can communicate at relatively high speeds with enhanced signal integrity. When designing for a RS-485 transceiver in a system, it can be efficient to minimize the amount of logic lines that connect to each transceiver where possible. A microcontroller can have limited GPIOs to control the RS-485 transceiver. One method to reduce the logic lines is to combine the driver and receiver enable pin as shown in Figure 1-1.

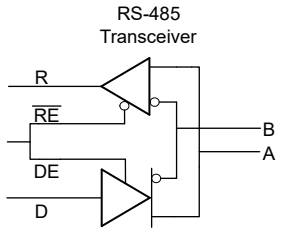

Figure 1-1. Shorted nRE and DE Pins on a Half-duplex RS-485 Transceiver

When the driver and receiver enable pins are shorted together, there are particular setups that can cause glitches. If the RC time constant on the bus is long enough, a low voltage can be read on the receiver pin right after the device is switched from transmitting to receiving. This voltage low can be read as a 0 bit. Because the R line is held high, this 0 bit can be interpreted as a start condition by the UART protocol.

This document includes the theoretical analysis behind these undesired behaviors. A half-duplex RS-485 transceiver is tested to demonstrate the majority of RS-485 transceivers. A timer-based fail-safe transceiver is also tested as the glitch can trigger this feature. Specifically, THVD1400 is representative of all general half-duplex devices in testing, and THVD2410 is tested to demonstrate the timer-based fail-safe scenario. Finally, a combination of workarounds are provided, followed with test data showcasing this.

2 Overview of RS-485

RS-485 is a standardized, physical layer communication method. Standardized by the Telecommunications Industry Association (TIA) and Electronic Industries Alliance (EIA), RS-485 defines the electrical characteristics of a multi-point differential system. This provides designers with improved noise immunity, data rates up to 50Mbps, and the capability to transmit over 1.2 km at 100kbps or less with multiple transceivers on the bus. Figure 2-1 demonstrates a typical setup with a half-duplex RS-485 transceiver.

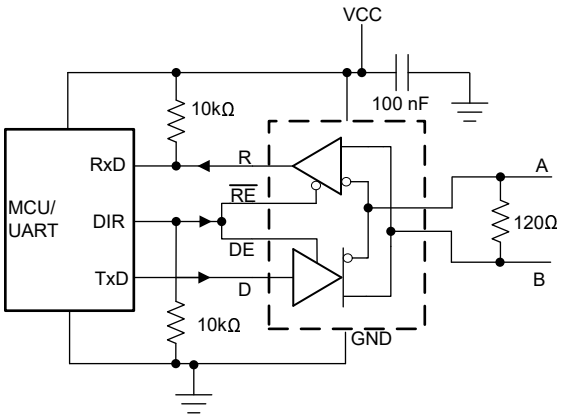

Figure 2-1. Typical RS-485 Half-duplex Setup with nRE and DE Shorted

A microcontroller can send and receive data using a variety of protocols since RS-485 only defines the physical layer. In the transmit mode, the transceiver receives data through the D pin from the MCU. The transceiver can then output dominant and recessive values to the bus via the differential outputs: A and B. A is typically the non-inverting bus line, while B is the inverting bus line. In receiving mode, the transceiver can output a digital signal to the R pin by reading the difference of the A and B bus lines.

3 Shorting DE and nRE Pins

Focusing on the nRE (denoted as *not* RE) and DE pins of the transceiver, we notice a single MCU pin—labeled DIR—controls whether the device receives or drives data on the A and B bus lines. When nRE and DE are a logic high voltage, the transceiver is only driving signals on the bus. Likewise when nRE and DE are low, the transceiver is only receiving signals. From this setup, switching from driver to receiver modes when the RC time constant is long enough can cause the receiver to output invalid voltage levels.

4 General R Pin Glitch Background

When the shorted DE and nRE line transitions from high to low, the transceiver switches from transmitting on the bus to reading the bus. R is pulled up with a resistor to VCC, meaning it has a high idle state. When a high level of bus capacitance is present, the last remaining bit can be outputted on the R pin from when the transceiver was previously transmitting. This is due to the capacitance slowing the rate of discharge on the bus. This can be a particular problem for systems using the UART protocol. If the R pin temporarily drops low, the MCU can read this as false start condition.

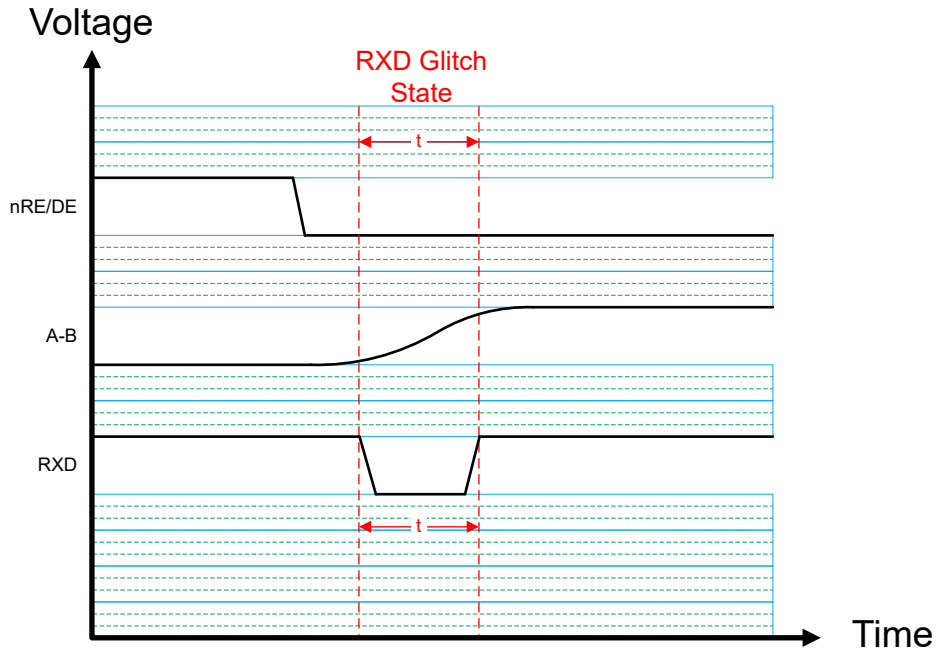

Figure 4-1. Theoretical RXD Glitch State

Figure 4-1 represents what this glitch can look like graphically. The nRE/DE pin is switched into receiving mode, and the A-B bus differential transitions slowly to a high voltage. Because of capacitance on the A-B bus lines, the RXD voltage reads from when the device was previously transmitting. In this case, the R pin shows a voltage low, outlined as the “RXD Glitch State”. Voltage drops greater than 1V can throw a UART error. For this article, any voltage drop greater than 1V can be considered a glitched state.

When the time to discharge the differential output (A-B) lines is greater than the time to turn on the receiver mode, the RXD pin experiences a voltage change seen in Equation 1. The differential bus is still discharging while the receiver is starting to read the bus. Due to the various bus setups and capacitance, this discharge time can vary widely.

$$t_{RXD\ ON} < t_{V_{OD}\ Discharge} \quad (1)$$

5 Theoretical Glitch Case for RS-485 Transceivers

For a RS-485 transceiver to exhibit this RXD error, several setup conditions must be present in conjunction:

- The TXD voltage is less than or equal to $V_{IL,max}$.
- The RXD line is pulled high to VCC.
- nRE and DE pins are shorted together.
- High relative levels of capacitance are on the bus.
- The transceiver is recently switched from transmitting to receiving on the bus.

Due to the change in modes, the RXD pin switches from high impedance to actively outputting the bus differential. With little capacitance on the bus line, the RXD line stay at a high voltage because of the pull-up resistor. But due to various sources of capacitance, the RC constant effectively resists the RXD voltage pulling to a high voltage value. If the RC constant is large enough, the voltage discharge on the bus can reflect on the RXD line as a drop in voltage as Figure 4-1 shows.

The THVD1400 can be tested for this case and is representative of standard half-duplex RS-485 devices. Similar results can apply to other RS-485 half-duplex transceivers with shorted enable pins.

6 Theoretical THVD24XX Idle Fail-safe Case

The THVD24XX series is another RS-485 transceiver line that adds additional fault protection and other protection features. Namely, THVD24XX devices have a fail-safe feature that can detect if there is open, short or idle circuit on the differential bus lines. All three of these conditions can result in the bus having near 0 voltage. To detect these conditions, if the bus voltage is inside the V_{TH_FSH} range for longer than time of $t_{D(OFS)}$, the device can output a logic high state. Equation 2 shows this:

$$\text{If} \quad V_{TH_FSH-} < V_{Bus} < V_{TH_FSH+} \quad \text{For} \quad t_{D(OFS)} \text{Then} \quad V_{RXD} = \text{Logic High} \tag{2}$$

Similar to the general RS-485 glitch case, the half-duplex THVD24XX devices can experience a voltage shift on the RXD line with high enough capacitance present. The same conditions mentioned previously must be met for the THVD24XX device to have a change in voltage: TXD is at less than $V_{IL,max}$, RXD is pulled high with a resistor, and the shorted nRE/DE pins recently switched the device into the receiver mode.

However, the key difference for the THVD24XX fail-safe devices is that the devices can enter fail-safe mode with enough capacitance on the bus when entering a receiver mode. This is different from general RS-485 devices as the devices can show voltage drops for various times.

Since the voltage on the A-B bus differential is changing slowly due to capacitance, the R pin can follow the last state of the bus. If this state is a voltage low around 0V, the state can trigger the fail-safe feature if the voltage is inside the threshold range. Once triggered, the R pin can output low until this fail-safe timer has expired. Although the fail-safe feature is not intended for this scenario, the feature provides a predictable time of $t_{D(OFS)}$ until the bus is ready to be read after switching modes.

THVD2410 can be tested with these conditions, and THVD2450 can also have similar results.

7 RS-485 Testing Setup

Both the THVD1400 and THVD2410 are tested on the setup found in Figure 7-1. For the logic side, the RXD pin has 1 kΩ resistor tied to VCC. The nRE/DE pins are connected to a 5kHz square wave to simulate the transceiver changing modes. The TXD or D pin is held at 0V. For the bus side, a 60 Ω resistor is used to simulate a load, and C1 represents the various capacitance to be tested. The R line, nRE/DE line and the differential A-B lines can be measured.

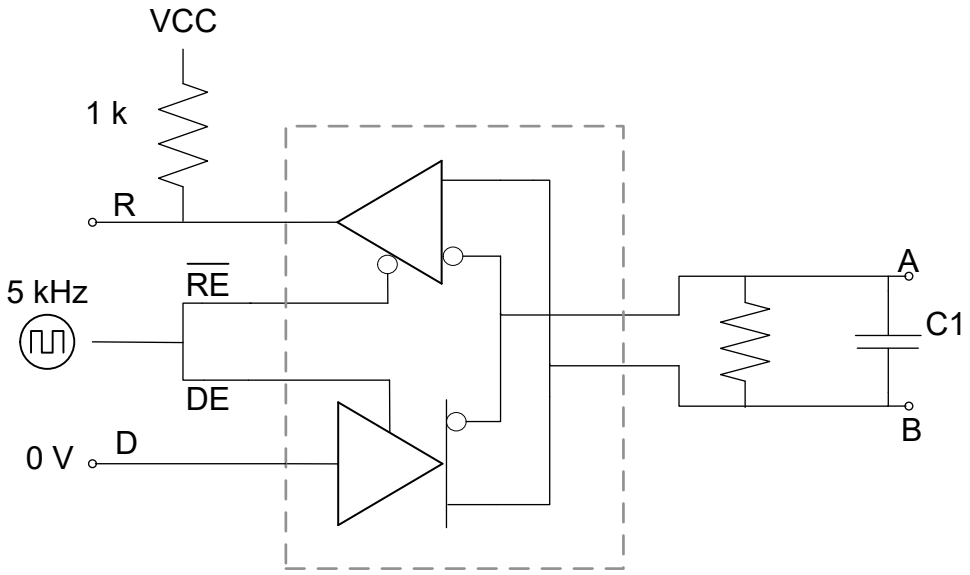

Figure 7-1. THVD 1400 and THVD2410 Setup

Two sources of capacitance can be tested on the differential bus lines: single-ended and differential. Single-ended capacitance is where capacitors (C1 and C2) are tied from each differential bus line to ground. Differential capacitance is a single capacitor (C3) tied from line A to line B. Both setups can be tested between 50pF to 1000pF.

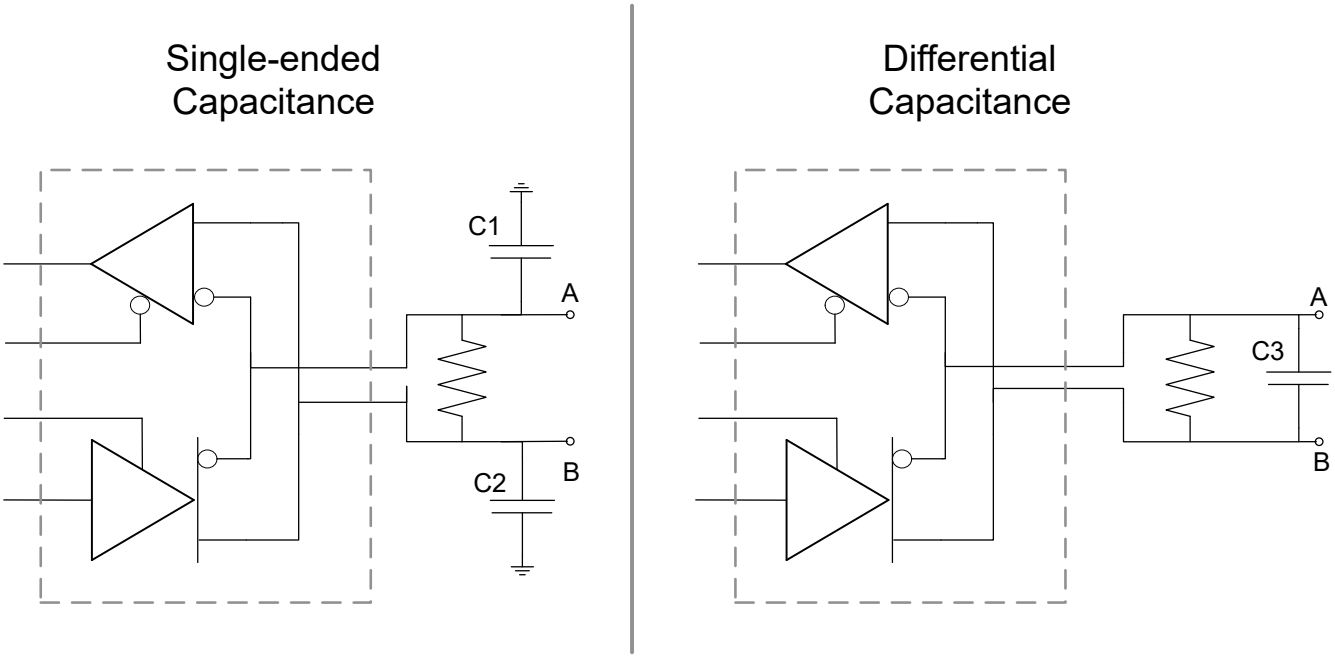

Figure 7-2. Single-ended and Differential Capacitance

8 THVD1400 Capacitance Results

With the setup and conditions described previously, the waveforms with highest and lowest tested capacitance can be shown. Table 8-1 lists the voltage drop times for all single-ended and differential capacitance with D held at 0V.

For 50pF single-ended capacitance,Figure 8-1shows that the yellow nRE/DE line is switched from transmitting to receiving. The orange A-B line demonstrates the differential bus gradually pulling to a high voltage due to the RC constant. As a result, the R pin has a voltage drop that lasts 112ns.

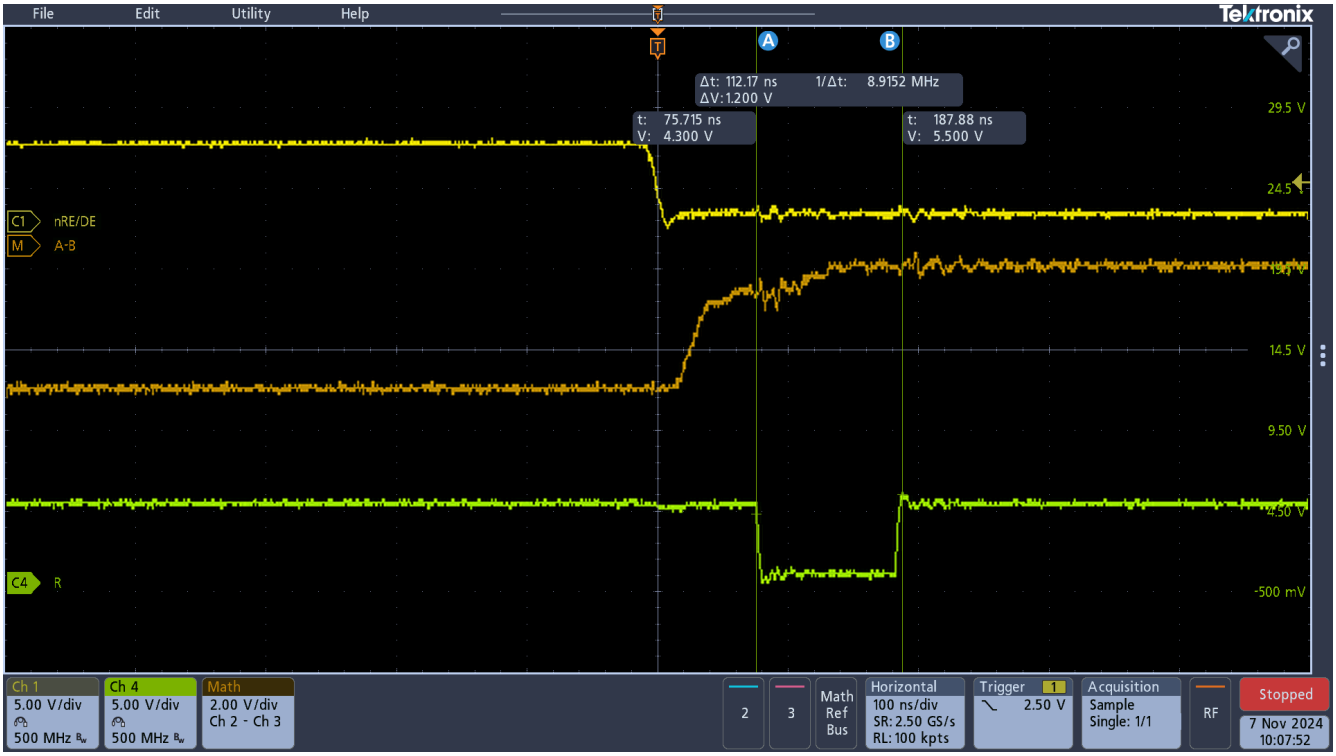

Figure 8-1. THVD1400 50pF Single-ended Capacitance

Figure 8-2 shows that when a 1000pF single-ended capacitance is on the bus, a longer voltage drop of 189ns is seen. The A-B bus line requires more time to reach a steady voltage value.

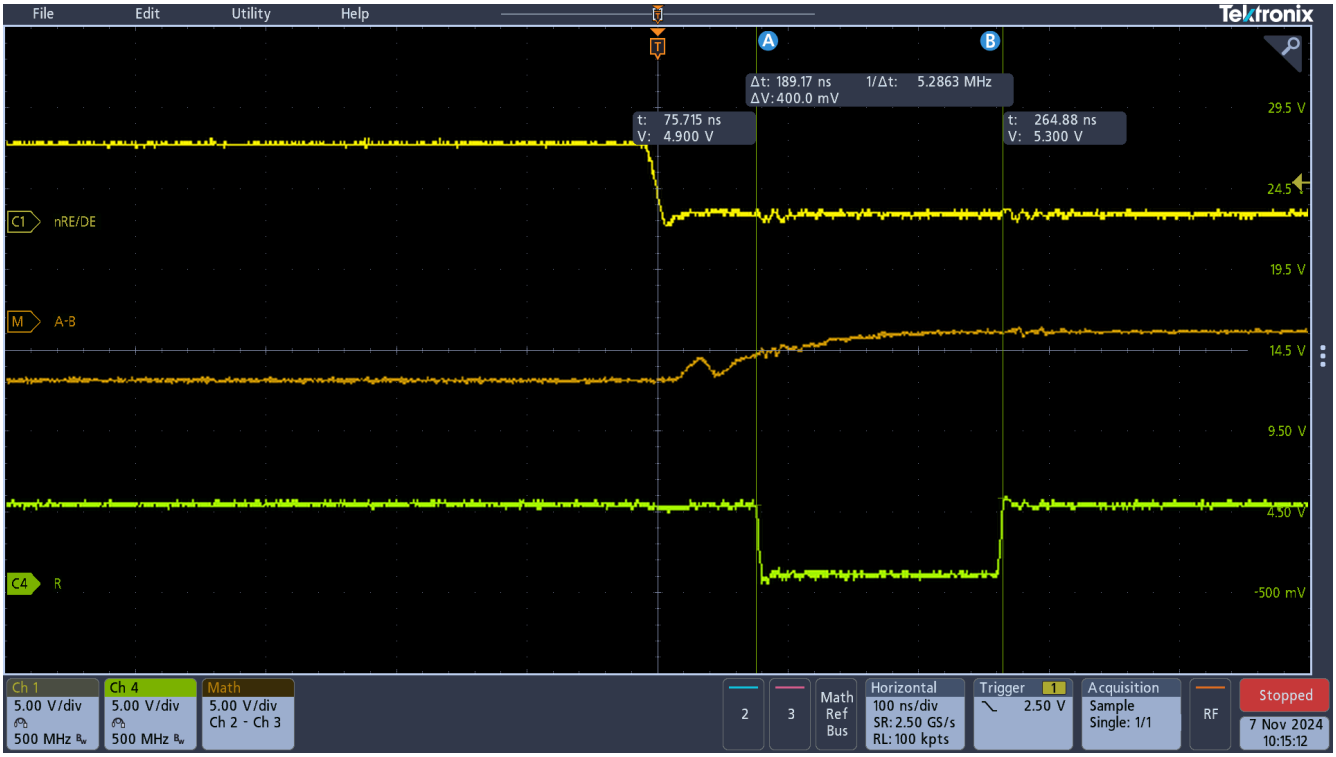

Figure 8-2. THVD1400 1000pF Single-ended Capacitance

For differential capacitance of 50pF, the voltage drop lasts for 114ns in Figure 8-3.

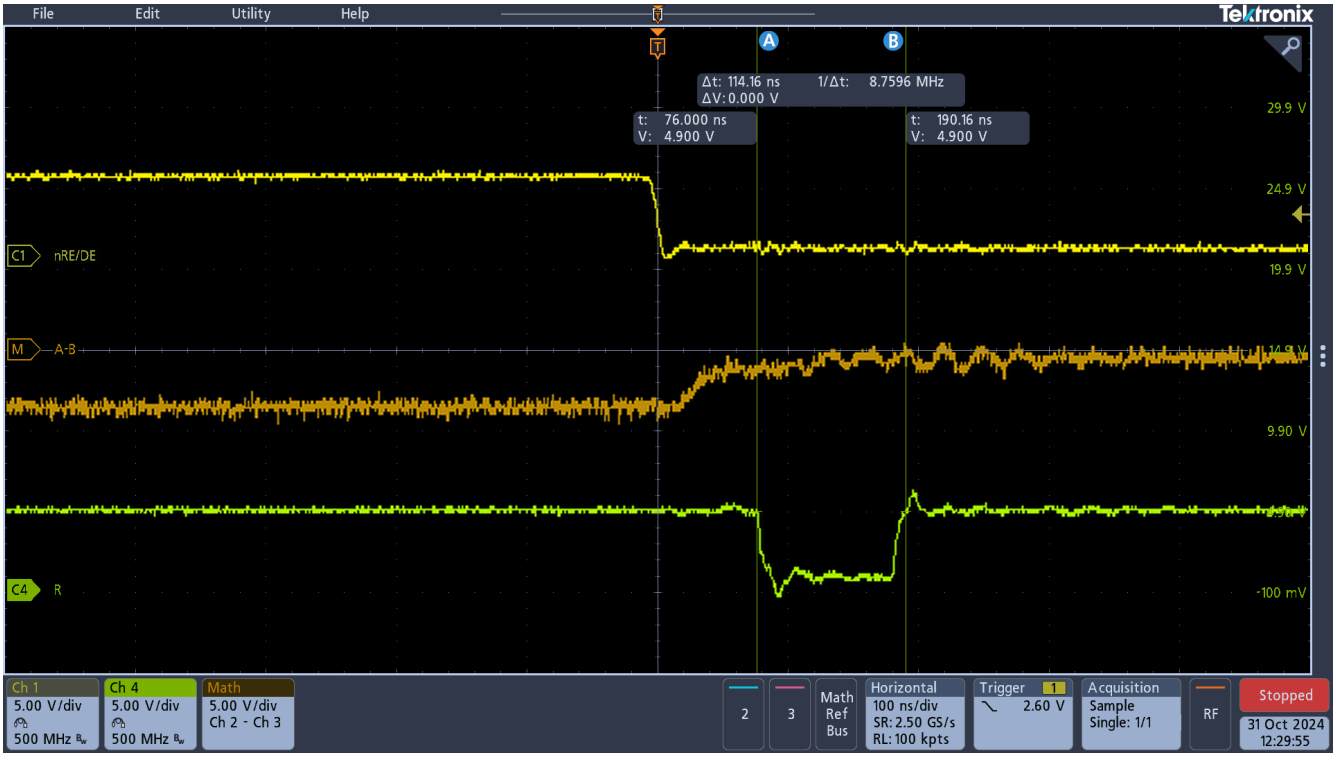

Figure 8-3. THVD1400 50pF Differential Capacitance

For a differential capacitance of 1000pF, the voltage drop lasts for 284ns in Figure 8-4. Again, the A-B bus line can be seen taking more time to reach a voltage high. Hence, the longer voltage drop period.

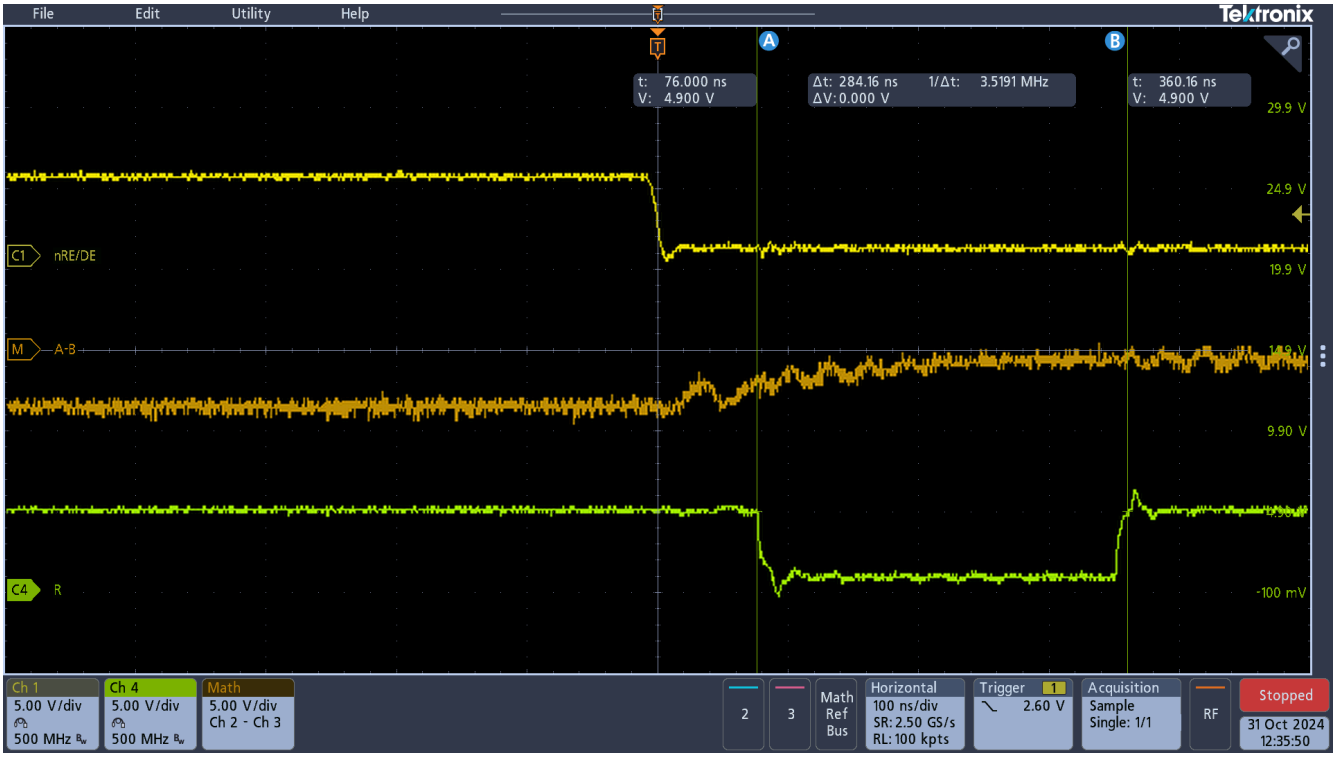

Figure 8-4. THVD1400 1000pF Differential Capacitance

Table 8-1 shows that as the capacitance increases on the bus, the voltage drop time increases.

Table 8-1. THVD1400 Glitch Results

	Capacitance								
	50pF	**100pF**	**220pF**	**330pF**	**470pF**	**570pF**	**760pF**	**860pF**	**1000pF**
Single-ended Glitch Time (ns)	112	121	141	147	159	166	172	181	189
Single-ended Voltage Drop (V)	0.60	0.73	0.69	0.82	0.65	0.72	0.64	0.52	0.61
Differential Glitch Time (ns)	114	124	140	156	184	193	211	249	284
Differential Voltage Drop (V)	0.43	0.39	0.26	0.47	0.30	0.51	0.43	0.48	0.44

9 THVD2410 Capacitance Results

With an identical setup to the THVD1400, THVD2410 shows that idle fail-safe is triggered across every capacitance test. When switching from transmit to receive modes, THVD2410 enters the idle fail-safe for 10 µs.Figure 9-1and Figure 9-2 both show the same fail-safe time of 10 µs at 50pF and 1000pF. These results are consistent across singled-ended and differential capacitances.

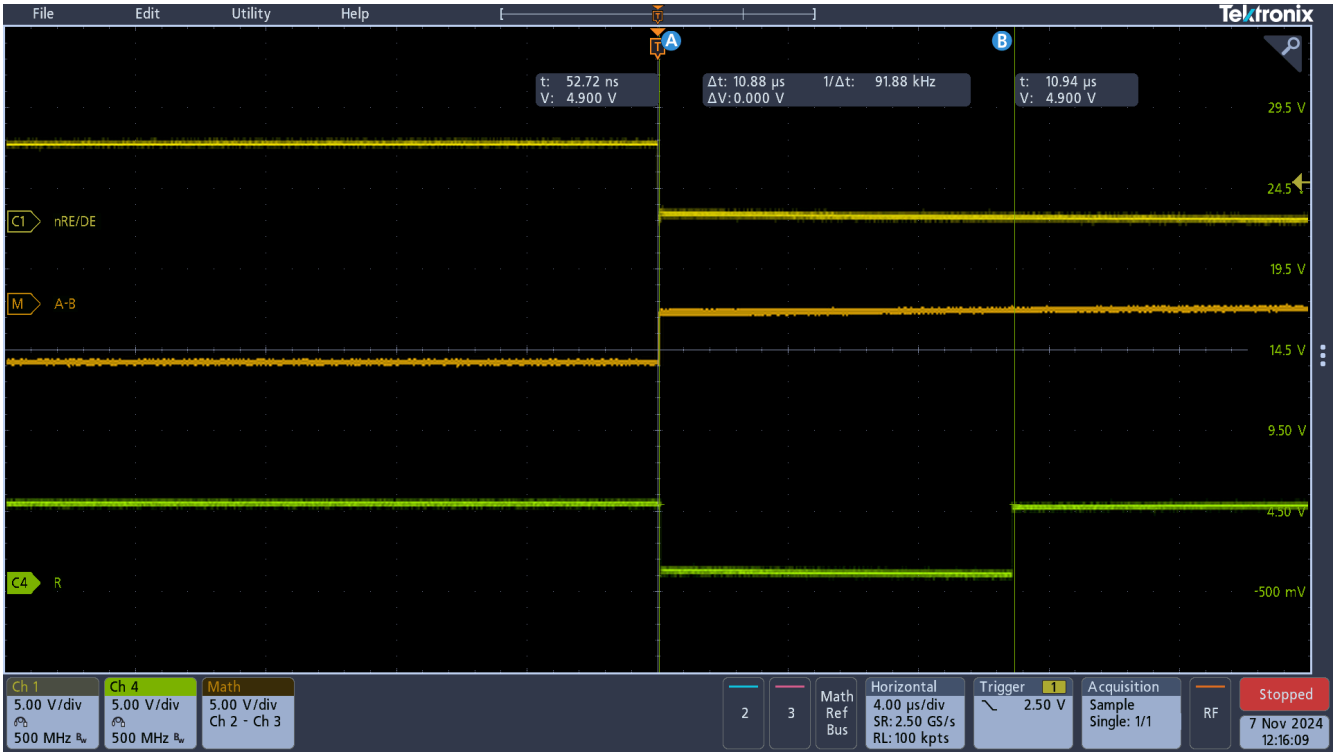

Figure 9-1. THVD2410 50pF Single-ended Capacitance

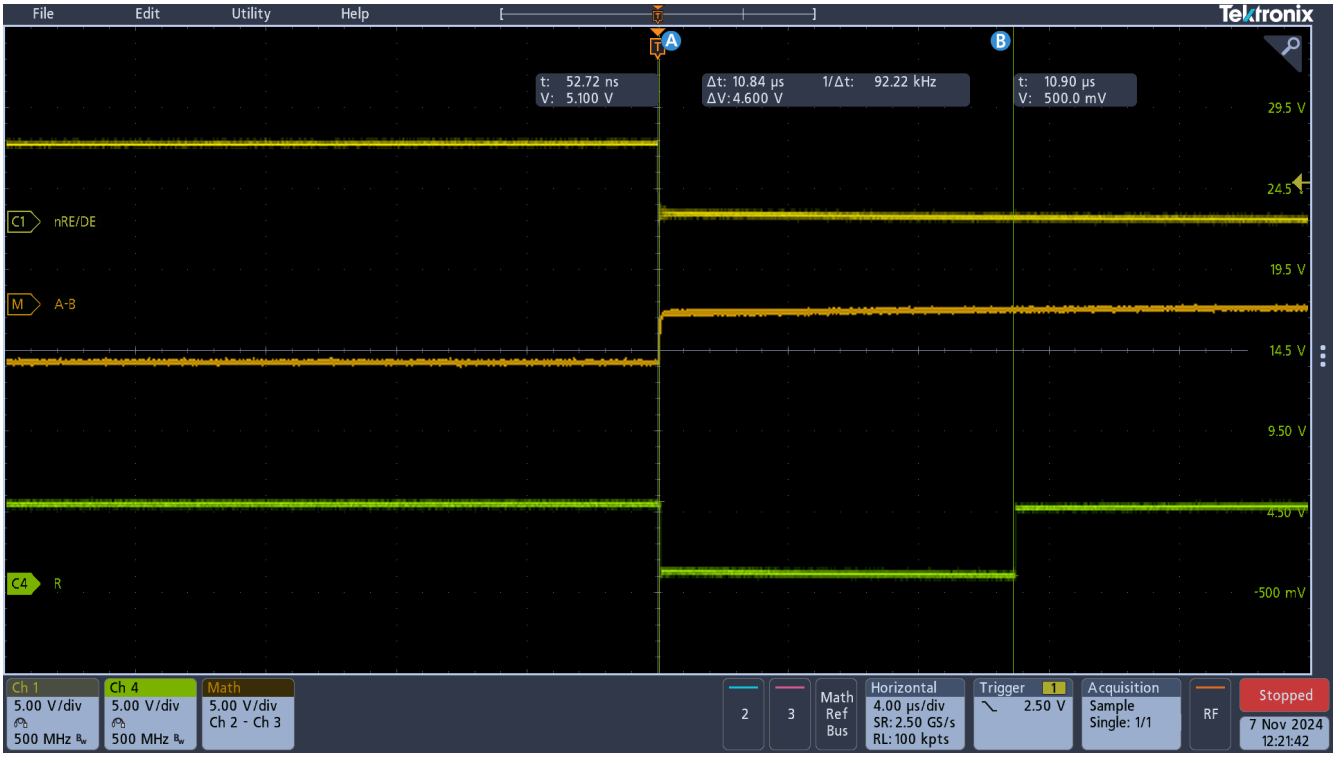

Figure 9-2. THVD2410 1000pF Single-ended Capacitance

Since the bus differential voltage enters the V_{TH_FSH} range for a long enough period of time, THVD2410 enters the idle fail-safe mode.

Table 9-1. THVD2410 Fail-safe Results

	Capacitance								
	50pF	**100pF**	**220pF**	**330pF**	**470pF**	**570pF**	**760pF**	**860pF**	**1000pF**
Single-ended Glitch Time (µs)	10.56	10.67	10.63	10.69	10.65	10.71	10.63	10.65	10.69
Single-ended Voltage Drop (V)	0.60	0.69	0.65	0.64	0.73	0.65	0.48	0.61	0.64
Differential Glitch Time (µs)	10.67	10.76	10.71	10.65	10.67	10.71	10.67	10.68	10.77
Differential Voltage Drop (V)	0.56	0.73	0.72	0.63	0.68	0.56	0.69	0.77	0.65

10 Voltage Drop Workarounds

If a voltage drop on the RXD line is causing issues for a system, there are a variety of methods to solve this voltage drop.

- The main workaround is to end the last transmission with a voltage high on the TXD line. This eliminates the voltage drop on the RXD line. Across the various tests discussed previously, a voltage low was simulated on the TXD line with 0V. When the TXD line is held at a voltage high, there is no voltage drop present as seen for both THVD1400 and THVD2410 in Figure 10-1 and Figure 10-2.

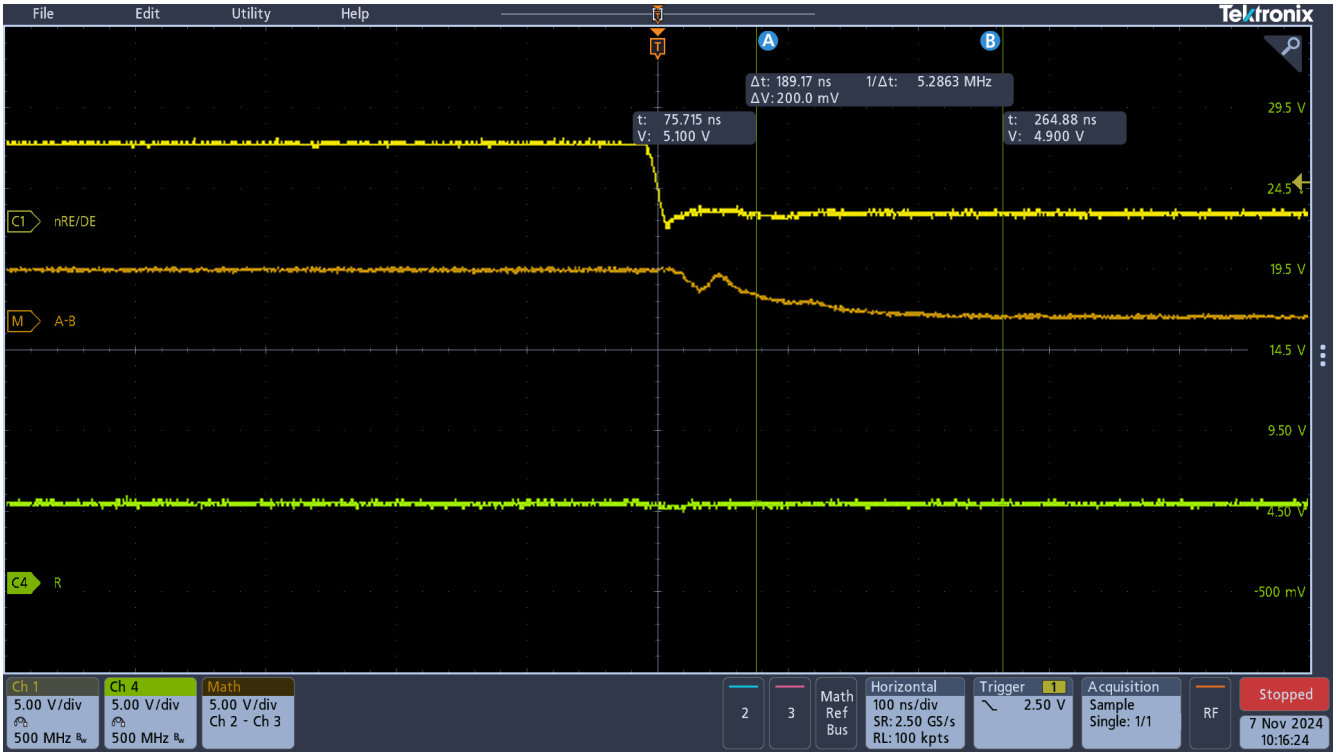

Figure 10-1. THVD1400 1000pF TXD High

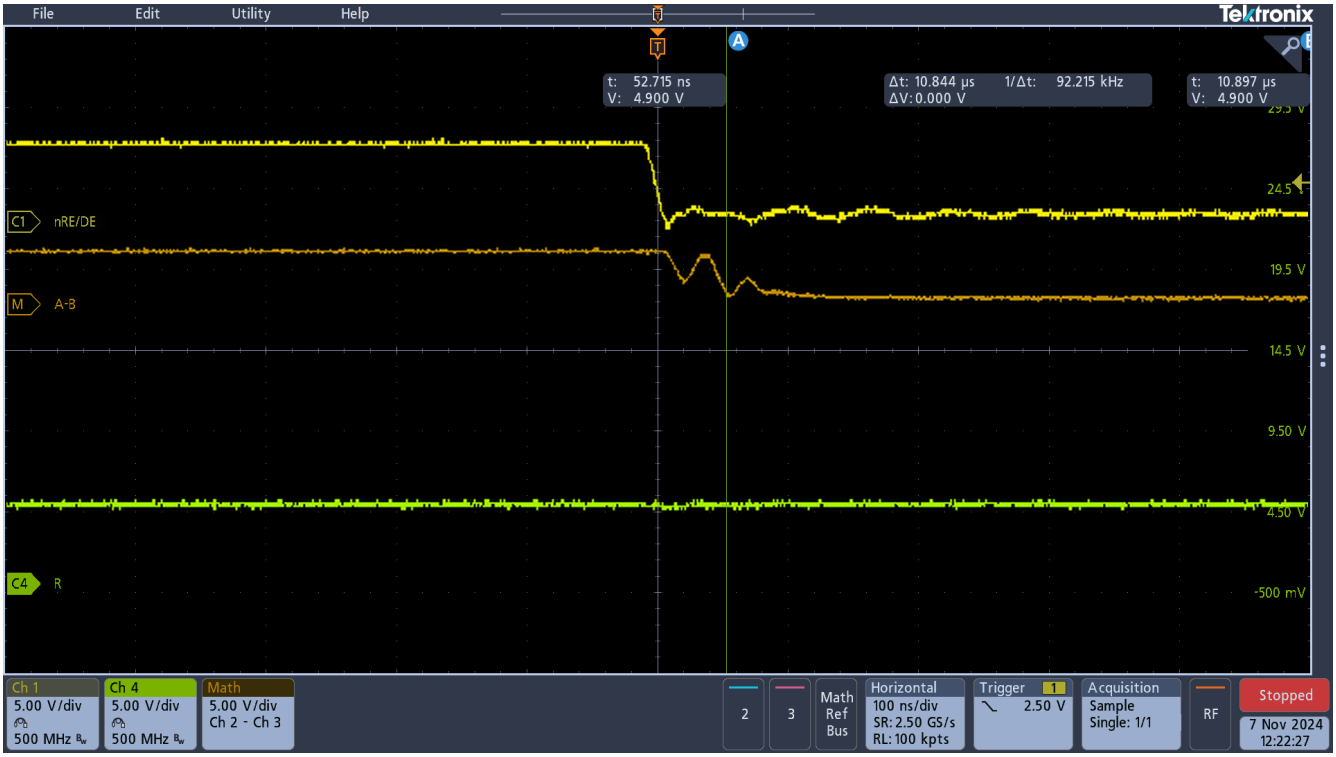

Figure 10-2. THVD2410 1000pF TXD High

Holding the last TXD bit high works for both single-ended and differential capacitance setups for THVD1400 and THVD2410. This workaround can also apply to most RS-485 devices experiencing a voltage drop on the RXD line due to high capacitance.

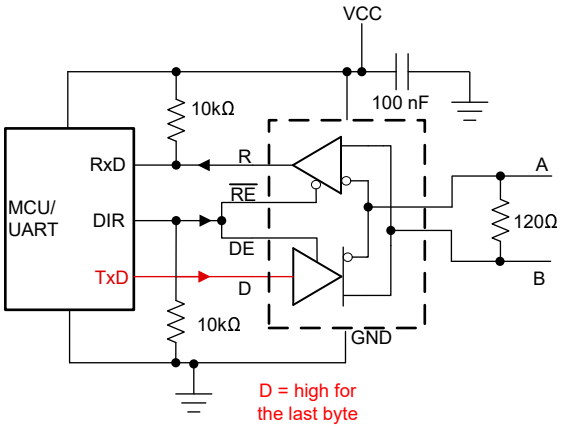

Figure 10-3. DE and RE Shorted with D=High

- Another workaround is to separately control the nRE and DE pins using the MCU. Rather than shorting these together, nRE and DE can be toggled off and on with a slight delay between modes such that the bus has enough time to discharge. This allows the capacitors to fully discharge before the transceiver starts to read the bus.
- Lastly, if the other methods are not possible for a particular system, capacitance on the bus need to be minimized to shorten the RXD voltage drop time. Unnecessary filtering capacitors or other capacitive components need to be removed.

11 Summary

Shorting the driver and receiver enable pins for any half-duplex RS-485 transceiver can potentially create R pin voltage drops with high capacitance after switching into the receiver mode. Testing the application scenario with the THVD1400 and THVD2410 with bus capacitance ranging from 50pF to 1000pF showed the glitch occurring during the TX to RX mode switch. The THVD1400 glitch was a result of the time RC time constant on the differential bus, while the THVD2410 glitch was a combination of the fail-safe delay and the RC time constant on the differential bus. Sending a logic high on the TXD or D pin before entering receiver mode of the transceiver successfully removes any voltage drop caused by bus capacitance. All tested capacitance showed no voltage drops when the TXD pin was held high for both THVD1400 and THVD2410.

12 References

- Texas Instruments, *The RS-485 Design Guide*, application note.
- Texas Instruments, *RS-485 Basics Series*, technical white paper.
- Texas Instruments, *RS-422 and RS-485 Standards Overview and System Configurations*, application note.

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