Application Note

UCC14240-Q1 Simplifies HEV, EV, Bias Supply Design for Isolated Gate Drivers

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ABSTRACT

For hybrid electric vehicles (HEVs) and electric vehicles (EVs), isolated gate drivers are widely used in traction inverters and on-board chargers (OBC). The need for high-reliability gate drive bias architectures can require several independent, isolated power converters where printed circuit board (PCB) space and component height are premium. The *UCC14240-Q1* is a high-efficiency, low-emissions, 3-kV_{RMS} isolated DC-DC converter module capable of delivering up to 1.5-W of power, developed specifically for isolated gate driver bias applications. This application report introduces the benefits of using the UCC14240-Q1 for isolated gate driver bias applications. The focus of this application report is for automotive applications but can easily be extended to cover industrial uses. Design guidelines intended to highlight the ease of use of this fully integrated bias supply solution are also provided.

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1 Introduction

The UCC14240-Q1 is a high-efficiency, low-emissions, 3-kV_{RMS} isolated DC-DC converter module capable of delivering up to 1.5-W of power. The UCC14240-Q1 integrates the control, power switches and transformer into a wide-body, 16-pin SOIC package. This allows systems to reduce size and cost by removing the need for separate isolated power supplies. The UCC14240-Q1 delivers class-leading efficiency in bias supply, power conversion from the primary to the secondary side while removing the need for bulky external transformers or power modules commonly used in existing designs.

This higher level of integration requires fewer components and less printed circuit board (PCB) area as well as significantly reduced height profile compared to discrete and modular power isolation techniques used in the field today. The UCC14240-Q1 operates from an input voltage range of 21 V<VIN<27 V. EV and HEV battery management systems (BMS) and traction inverters use voltage regulators to manage the wide voltage range (typically: 6 V<12 V<40 V) of the 12-V battery. Similarly, an isolated, redundant regulator is sometimes applied to the high-voltage (HV) battery stack with outputs made available to the low-voltage (LV) primary. Either or both of these regulators can easily be programmed to provide 24-V to the UCC14240-Q1 input. The UCC14240-Q1 is then used to convert 24 V from the LV primary to an isolated DC voltage of 18 V<VDD-VEE<25 V on the HV secondary.

Isolated gate driver ICs used in EV and HEV, HV applications are often driving insulated gate bipolar transistors (IGBTs) or silicon carbide (SiC) metal oxide semiconductor field effect transistors (MOSFETs). IGBTs and SiC MOSFETs can switch between zero and a positive voltage (VDD) but more typically require VDD during turn-on and a negative voltage (VEE) during turn-off. The UCC14240-Q1 is easily configurable between single output VDD bias voltage or dual output positive VDD and negative VEE bias voltage.

1.1 Pin Configuration and Functions

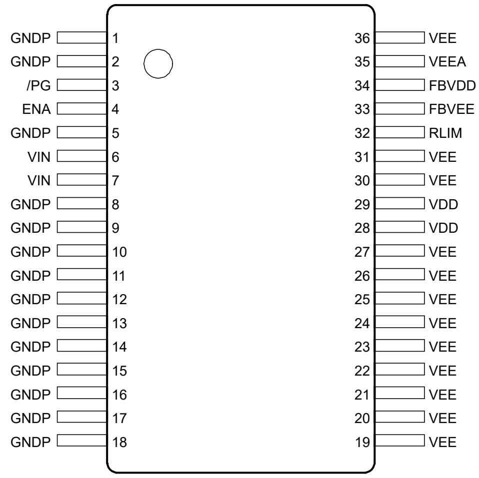

Figure 1-1. DWN Package, 36-Pin SSOP (Top View)

Table 1-1. Pin Functions

PIN		TYPE [1]	DESCRIPTION
NAME	NO.		
GNDP	1, 2, 5, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18	G	Primary-side ground connection for VIN. Place several vias to copper pours for thermal relief. See PCB Layout Considerations.
/PG	3	O	Active low powergood open-drain output pin. /PG pulled low when (UVLO ≤ VIN ≤ OVLO); (UVP1 ≤ (VDD – VEE) ≤ OVP1); (UVP2 ≤ (COM – VEE) ≤ OVP2); $T_{J\_Primary} \le T_{SHUT\_primary}$; and $T_{J\_secondary} \le T_{SHUT\_secondary}$
ENA	4	I	Enable pin. Forcing ENA LOW disables the device. Pull HIGH to enable normal device functionality. 5.5-V recommended maximum.
VIN	6, 7	P	Primary input voltage. Connect a 2.2-μF ceramic capacitor from VIN to GNDP. Connect a 0.1-μF high-frequency bypass ceramic capacitor close the IC pins.
VEE	19, 20, 21, 22, 23, 24, 25,26, 27, 30,31, 36	G	Secondary-side reference connection for VDD and COM. The VEE pins are used for the high current return paths.
VDD	28, 29	P	Secondary-side isolated output voltage from transformer. Connect a 2.2-μF and a parallel 0.1-μF ceramic capacitor from VDD to VEE. The 0.1-μF ceramic capacitor is the high frequency bypass and must be next to the IC pins.
RLIM	32	P	Secondary-side second isolated output voltage resistor to limit the source current from VDD to COM node, and the sink current from COM to VEE. Connect a resistor from RLIM to COM to regulate the (COM – VEE) voltage. See R_{LIM} Functional Description for more detail.
FBVEE	33	I	Feedback (COM – VEE) output voltage sense pin used to adjust the output (COM – VEE) voltage. Connect a resistor divider from COM to VEE so that the midpoint is connected to FBVEE, and the equivalent FBVEE voltage when regulating is 2.5 V. Add a 330-pF ceramic capacitor for high frequency decoupling in parallel with the low-side feedback resistor. The 330-pF ceramic capacitor for high frequency bypass must be next to the FBVEE and VEEA IC pins on the top layer or back layer connected with vias.
FBVDD	34	I	Feedback (VDD – VEE) output voltage sense pin and to adjust the output (VDD – VEE) voltage. Connect a resistor divider from VDD to VEE so that the midpoint is connected to FBVDD, and the equivalent FBVDD voltage when regulating is 2.5 V. Add a 330-pF ceramic capacitor for high frequency decoupling in parallel with the low-side feedback resistor. The 330-pF ceramic capacitor for high frequency bypass must be next to the FBVDD and VEEA IC pins on the top layer or back layer connected with vias.

Table 1-1. Pin Functions (continued)

PIN		TYPE (1)	DESCRIPTION
NAME	NO.		
VEEA	35	G	Secondary-side analog sense reference connection for the noise sensitive analog feedback inputs, FBVDD and FBVEE. Connect the low-side feedback resistors and high frequency decoupling filter capacitor close to the VEEA pin and respective feedback pin FBVDD or FBVEE. Connect to secondary-side gate drive lowest voltage reference, VEE. Use a single point connection and place the high frequency decoupling ceramic capacitor close to the VEEA pin. See PCB Layout Considerations.

(1) P = power, G = ground, I = input, O = output

2 Three-Phase Traction Inverter

The traction inverter is part of the electric drive that controls the electric motor responsible for propulsion of the vehicle. This is a key part of the HEV, EV electrical system used to convert DC power from the HV battery stack to three-phase, AC power used to drive the two or more electric motors.

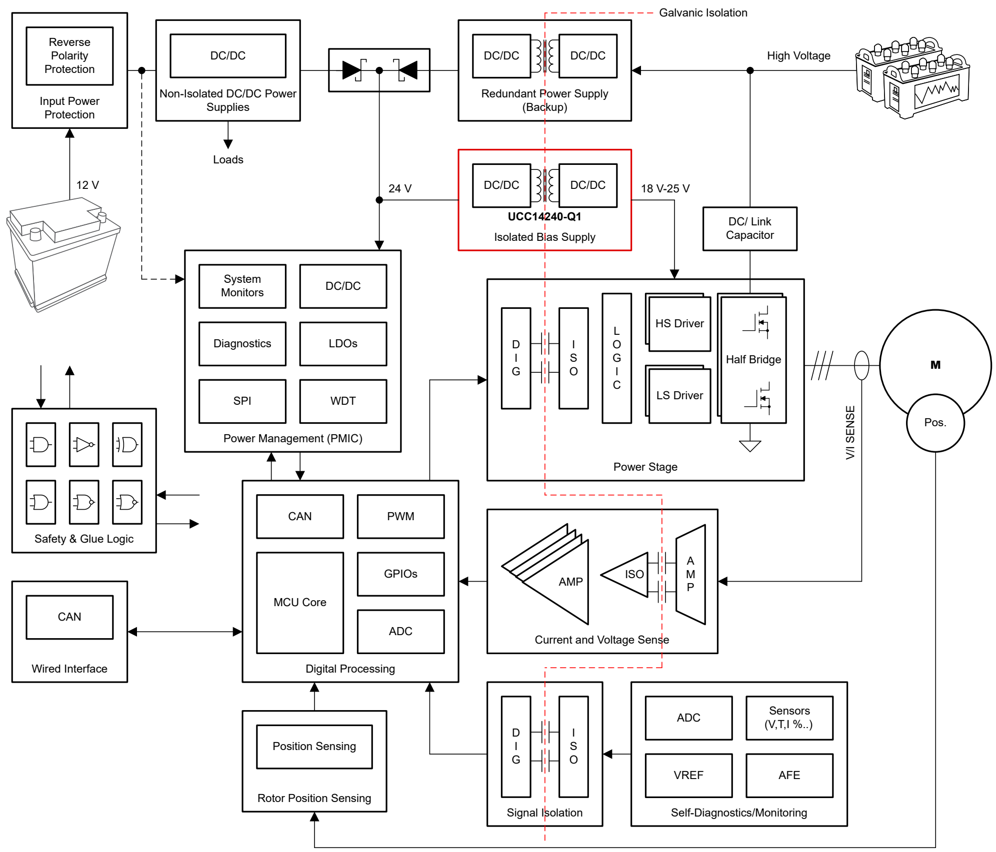

Figure 2-1. Traction Inverter Block Diagram

The galvanic isolation between the LV primary and HV secondary is shown by the red dashed line in the traction inverter block diagram shown in Figure 2-1. Motor diagnostics, voltage and current sensing and a HV DC-DC power converter are a few examples shown where digital signals and power are passing from the HV battery and motor side to the LV battery side. The focus of this application report is on the isolated bias supply, which converts a DC voltage from the LV battery side to the HV battery side used to bias the HS and LS drivers in the power stage.

3 Gate Drive Bias Requirements

Traction inverters have unique gate drive bias architectures based on required levels of safety, isolation, fault detection, reliability and load. The load seen by the gate drivers consists of SiC MOSFETs or IGBTs arranged in a half-bridge, three-phase configuration. Since there are three phases to consider, this means there are three half-bridge arrangements that must be properly isolated and biased. SiC and IGBT switches are favored over Si

MOSFETs because of their superior HV, dynamic switching characteristics, current handling capability and high temperature rating.

This section will consider the impact of the following, from an isolated bias supply point of view: gate drive bias architectures, IGBT vs SiC requirements, determining required bias supply power, input voltage requirements and output voltage regulation requirements.

3.1 Gate Drive Bias Architectures

Within the HS Driver and LS Driver power stage blocks of Figure 2-1 exists one of three unique configurations for distributing the bias supply voltage to each of the isolated gate drivers. Gate drive bias architectures are typically classified into three main types: centralized, distributed and semi-distributed. Hybrid examples also exist and tend to be based on one or more of the three types shown in Figure 3-1.

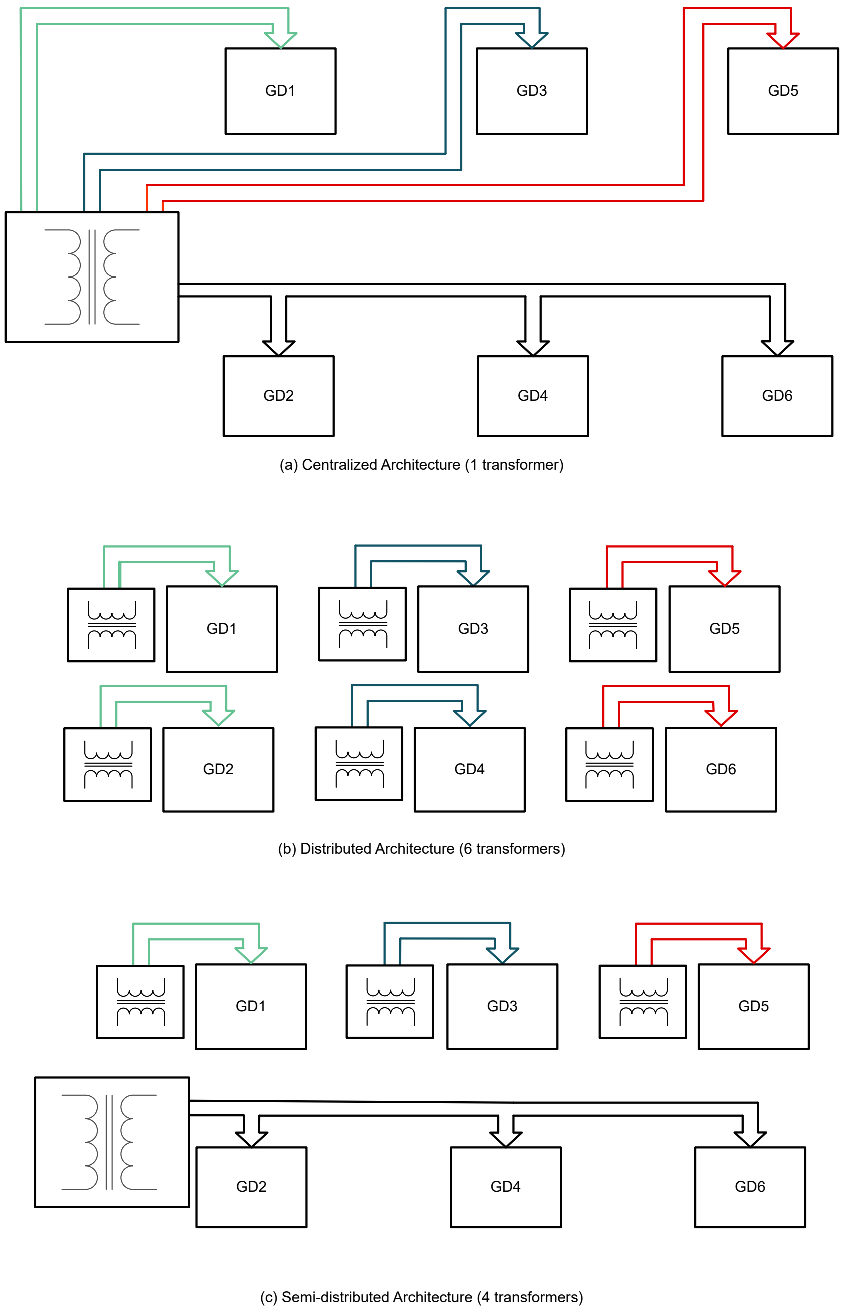

Figure 3-1. Gate Driver Bias Supply Architectures

The centralized architecture achieves isolation through a single transformer used to bias all six drivers. Because the transformer must be rated for the full bias power and achieve primary to secondary isolation between multiple windings, this results in the largest size transformer among the three architectures. Furthermore, if any single winding fails, the transformer fails, losing bias voltage to all three inverter phases. This is the least preferred option from a size, weight, and fault isolation point of view.

At the other end of the spectrum, we see the distributed architecture with six individual bias supplies and six isolation transformers. For fault detection and reliability, distributed architectures are the best approach but are often discounted because of the higher number of components required. The benefit is that a bias failure at any single gate driver can be detected and corrective action assigned, allowing the EV to remain operating with a reduction in traction inverter performance. Here, the total required bias power is divided between each of the six converters. While the power delivered to each gate driver is reduced by six, a proportional reduction in transformer size cannot be fully realized due to the winding spacing and separation required to meet isolation standards. This is a limitation of traditional wire wound transformers the UCC14240-Q1 has overcome. A 3-kV$_{RMS}$ isolation transformer, control and power stage capable of 1.5-W bias power rated to 105°C integrated in a 3.55-mm height, SOIC package make the UCC14240-Q1 perfectly suited for distributed bias architectures.

Semi-distributed architectures can also take advantage of UCC14240-Q1 to bias GD1, GD3 and GD5 when the required power for each is less than 1.5 W. For the low-side bias of GD2, GD4 and GD6, when the total required power exceeds 1.5 W, the *UCC25800-Q1* Ultra-low EMI Transformer Driver is a perfect companion to the 3x UCC14240-Q1 for building a high-performance, semi-distributed, isolated gate drive bias system.

3.2 IGBT vs. SiC

Single IGBT and SiC discrete transistors are available in industry standard packages such as TO-247 and TO-263 and are widely used in automotive, industrial and commercial applications. However, due to the unique, three-phase, half-bridge arrangement needed for inverters and high-power motors, two to six discrete devices built on an aluminum baseplate, encapsulated in plastic are more common. These specialized half-bridge, module packages are designed for high vibration and thermal management and can consist of SiC or IGBT switches.

IGBTs can carry large amounts of current with low saturation voltage, resulting in low conduction losses but are limited by turn-off loss, switching frequency and DC blocking capability. SiC MOSFETs are HV wide-bandgap (WBG) devices, well recognized in the industry for their superior overall advantages compared to Si based IGBT transistors. Reduced HV switching loss, better thermal capability, smaller die size, lower total gate charge, faster switching speeds and lower conduction losses have placed SiC at the forefront for HV, high-power-conversion inverters.

3.3 Determining Required Bias Supply Power

Once a bias architecture is decided, the first step for designing the bias supply is determining the power required according to the IGBT or SiC power module gate charge, Q_G. Table 3-1 highlights some key parameters comparing two 1.2-kV IGBT vs SiC modules.

Table 3-1. IGBT vs SiC Parametric Comparison

	V_{CE}, V_{DS} (V)	I_C, I_D (A)	V_{GE}, V_{GS} (V)	$V_{GE/S(th)}$, (V)	Q_G (µC)
6-pack IGBT	1200	380	-8/15	5.2	**1.75**
6-pack SiC	1200	400	-5/15	3.25	**1.32**

Knowing Q_G, $V_{GE(ON)}$, $V_{GE(OFF)}$ and the switching frequency, F_{SW}, the required power, due to dynamic switching, can be calculated according to Equation 1.

$$P_{SW} = Q_G \times \left(V_{GE/S(ON)} - V_{GE/S(OFF)}\right) \times F_{sw} \tag{1}$$

There is also power required to support the product of the total bias voltage and gate drive quiescent current, I_Q. The quiescent current for a given driver can be obtained from the manufacturers data sheet. Some gate driver IC data sheets specify I_{Q_VDD} and I_{Q_VEE} separately but others can only specify I_{Q_VDD}. For calculating quiescent power, the larger I_Q value should be used and the power can be calculated according to Equation 2.

$$P_{IQ} = \left(V_{GE/S(ON)} - V_{GE/S(OFF)}\right) \times I_Q \tag{2}$$

The total required bias power is then given as:

$$P_{BIAS} = P_{SW} + P_{IQ} \tag{3}$$

For the purpose of comparison, assume a gate driver such as the *UCC21732-Q1* is used for the IGBT and SiC. From the UCC21732-Q1 data sheet, the maximum I_{Q_VDD} is given as 5.9 mA. If both are operating at 20 kHz and switching over their full range of Q_G, the required gate drive bias power for each of the modules listed in Table 3-1, is given by Equation 4 and Equation 5 as:

$$P_{BIAS(IGBT)} = (15\text{ V} - (-8\text{ V})) \times [(1.75\ \mu\text{C} \times 20\text{ kHz}) + 5.9\text{ mA}] = 941\text{ mW} \quad (4)$$

$$P_{BIAS(SiC)} = (15\text{ V} - (-5\text{ V})) \times [(1.32\ \mu\text{C} \times 20\text{ kHz}) + 5.9\text{ mA}] = 646\text{ mW} \quad (5)$$

In addition to the well-known, dynamic switching and thermal benefits gained from SiC modules, their lower gate charge and ΔV_{GS} offers a less recognized, secondary benefit of a 31.4% reduction in required bias power compared to a similar rated IGBT module.

3.4 Input Voltage Requirements

UCC14240-Q1 requires a 24-V nominal, DC input voltage within the range of 21 V<VIN<27 V. The 12-V HEV, EV battery is the primary source for generating 24 V and since both reside on the LV side, a non-isolated, DC-DC converter can be used to provide the 24-V needed. The min/max voltage range for most 12-V, EV batteries is typically between 6 V<VBAT<28 V, but can reach as high as 40 V. General purpose PWM controllers from the *UCC280x-Q1* family are a good choice because of their wide selection of 12-V compatible UVLO options. These PWMs are automotive temperature rated, AEC-Q100 qualified controllers, available in either 50% or 100% max duty cycle and come in standard 8-pin SOIC packages. A flyback converter compatible with UC14240-Q1 would need to source a minimum of 7.5 W (3x UCC14240-Q1) for high-side only, in a semi-distributed architecture or 15 W for a fully distributed bias architecture.

Designing a pre-regulator capable of sourcing enough current to meet the start-up demand of up to six UCC14240-Q1 bias regulators turning on simultaneously is paramount. Depending on the voltage range of the 12-V battery, a suitable pre-regulator topology could be a boost, SEPIC, flyback or pushpull DC-DC converter. The following recommendations should be taken into consideration:

- Boost, SEPIC or flyback topologies are voltage sources interfacing to the UCC14240-Q1 input voltage. Depending on the total bias power and primary start-up current, it is important to assure enough output capacitance is present on the pre-regulator to assure reliable start-up.
- When operating in continuous conduction mode (CCM) the boost, SEPIC and flyback topologies each have a right- half plane zero (RHPZ) as part of their control loop plant. The minimum RHPZ frequency will force a low crossover frequency to assure loop stability. The low crossover frequency will result in poor dynamic response during start-up which can cause the output voltage to undershoot below the UCC14240-Q1 minimum input. This can cause a chattering start-up or even a failed start-up due to insufficient UCC14240-Q1 input voltage, when there is not enough energy storage capacitance on the pre-regulator output. Alternatively, it helps to design these converter topologies to operate as current mode control (CMC) in discontinuous conduction mode (DCM). This will mitigate the effect of the RHPZ and allow higher crossover frequency, better loop stability and improved dynamic response during start-up.
- If the duty cycle of the boost, SEPIC or flyback, operating in CCM, CMC is much higher than 50%, a large amount of slope compensation could be required to prevent subharmonic oscillation. During light-load start-up, the control will appear as voltage mode control (VMC) but the compensation will be for CMC. This problem is eliminated when operating in DCM, CMC, since no slope compensation is required.
- The push-pull, pre-regulator is different compared to the boost, SEPIC or flyback. The push-pull is a buck derived topology that includes an output inductor making it appear as a current source to the UCC14240-Q1 input. The push-pull is well suited for low input voltage operation, such as 12-V and this topology does not have a RHPZ to contend with so the control loop crossover can be much higher comparatively.
- Whichever topology is used, it is recommended to allow the pre-regulator output to reach full regulation before the UCC14240-Q1 (or multiple UCC14240-Q1) tries to start.

3.5 Output Voltage Requirements

Another important differentiation between IGBTs and SiC MOSFETs is their I_D, (I_C) vs V_{DS}, (V_{CE}) output characteristics. The left curve in Figure 3-2 shows the I_D vs V_{DS} for a SiC MOSFET, while the right side depicts the I_C vs V_{CE} for an IGBT. Both are 1.2-kV rated devices.

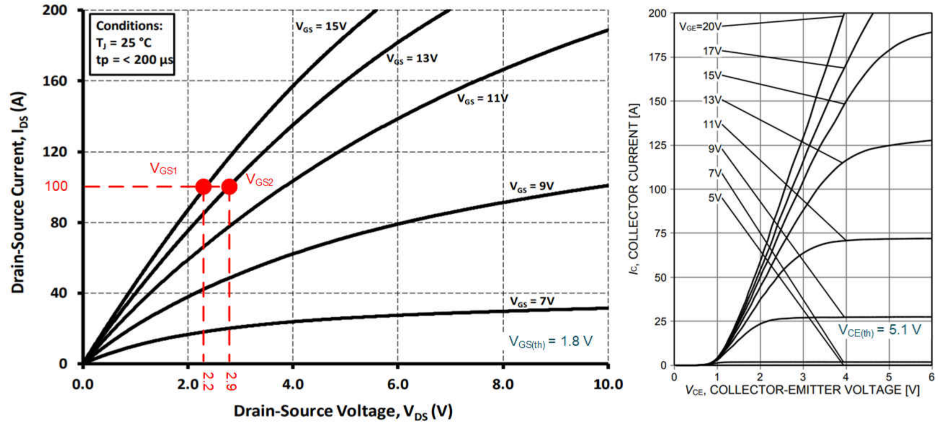

Figure 3-2. 1200 V, 100 A, SiC vs IGBT, VI Characteristics

The IGBT curves show a steep slope in the linear region and a slope of nearly zero in the saturation region. The transition between the linear, ohmic region and saturation region is sharp and distinct so that for any collector-emitter voltage greater than the threshold voltage, $V_{CE(th)}$, the IGBT appears as a voltage controlled current source.

Conversely, the SiC curves show no defined linear or saturation region and a much smaller change in I_D vs V_{GS} compared to the IGBT. As such, SiC MOSFETs are considered low or modest gain devices that are characterized by a continuous decrease in $R_{DS(ON)}$ up to the drain-source breakdown voltage. It is therefore, desirable to turn-on SiC MOSFETs with positive V_{GS} applied as close as possible to their breakdown voltage. For example, consider the two operating points, V_{GS1} and V_{GS2}, highlighted in the SiC IV curves of Figure 3-2.

$$R_{DS1} = \frac{V_{GS1}}{I_D} = \frac{2.2\ \text{V}}{100\ \text{A}} = 22\ \text{m}\Omega, \left(V_{GS1} = 15\ \text{V}\right) \tag{6}$$

$$R_{DS2} = \frac{V_{GS2}}{I_D} = \frac{2.9\ \text{V}}{100\ \text{A}} = 29\ \text{m}\Omega, \left(V_{GS2} = 13\ \text{V}\right) \tag{7}$$

Comparing the two operating points shows a 32% $R_{DS(ON)}$ increase and consequential conduction losses are 1.32 times higher when turning on with V_{GS2}=13 V as opposed to V_{GS1}=15 V. This behavior means the SiC acts more like a voltage-controlled resistor. The VDD turn-on bias supply should be tightly regulated to allow operation as close to 15 V as possible.

Some SiC MOSFET manufacturers recommend 5% accuracy on VDD but designers are often looking for 3% or even 1.5% VDD accuracy for traction inverter applications. Whether using power supply modules or a discrete design such as a distributed flyback converter, achieving such high regulation accuracy can be difficult and often requires additional post-regulation using low dropout (LDO) linear regulators. Better than 1.3% voltage regulation is one of the key features of UCC14240-Q1 making it well suited for enhancing SiC MOSFETs to their lowest $R_{DS(ON)}$ without the need for LDO's or discrete post-regulation circuitry.

Another notable difference between IGBTs and SiC MOSFETs is the $V_{GS(th)}$ ($V_{CE(th)}$) turn-on threshold voltage. For the two devices shown in Figure 3-2, this is noted in the lower right corner of each graph. SiC MOSFETs have low minimum $V_{GS(th)}$ and switch at high dV/dt making them more susceptible to dV/dt induced turn-on in half-bridge configurations. This is a condition where the low-side MOSFET of a half-bridge, such as those used in traction inverters, can inadvertently turn-on while V_{GS} commands it to be in the off-state. One way to circumvent this is to apply a negative voltage during turn-off, providing additional margin against the low $V_{GS(th)}$. The UCC14240-Q1 provides a switched capacitor voltage to generate a regulated, negative VEE voltage for reliable turn-off of SiC and IGBT transistor switches. This is a necessary part of a gate driver bias solution for assuring robustness of the SiC or IGBT module in harsh automotive environments.

4 Single Positive Isolated Output Voltage

For SiC MOSFETs or IGBTs requiring only a single isolated output voltage, the UC14240-Q1 can be configured to regulate between 18 V<VDD-VEE<25 V. Connecting pin 33 to pin 34 allows a single feedback resistor divider,

R_2, R_3 connected between VDD and VEE to set the regulation voltage as shown in Figure 4-1. The feedback pin serves as the inverting input to a hysteretic comparator. The non-inverting input is a precision, trimmed 2.5-V source, internally referenced to VEEA. For highest voltage set point accuracy, consider using 0.1% tolerance resistors, where the lower resistor, R_3, shares the same reference point as the internal voltage reference at VEEA (U1-35). By selecting R_3, then R_2 can be calculated according to Equation 8.

$$R_2 = \frac{R_3 \times (VDD - VEE - 2.5\ V)}{2.5\ V} \tag{8}$$

The circuit shown in Figure 4-1 is an example showing VDD = +20 V with respect to VEE. VEE can be referenced to any secondary-side, low-side ground or the switch-node, midpoint of a half-bridge configuration for high-side bias needs.

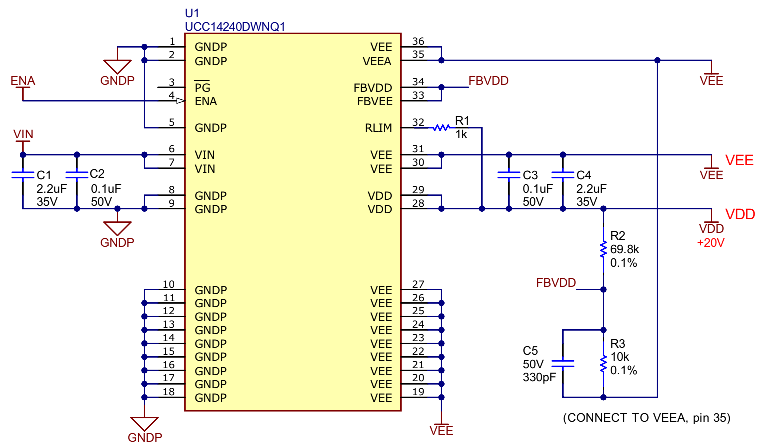

Figure 4-1. Single Isolated Output

5 Dual Positive and Negative Output Voltages

For optimal switching performance and robustness against dV/dt induced turn-on in half-bridge applications, many SiC MOSFETs and IGBTs benefit from a negative VEE voltage during turn-off. The UCC14240-Q1 greatly simplifies the task of establishing dual, positive and negative isolated output voltage rails when configured as shown in Figure 5-1.

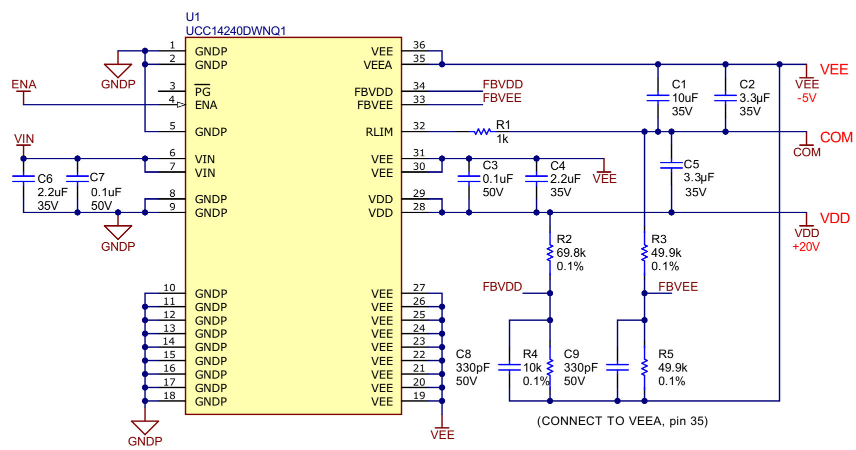

Figure 5-1. Dual Positive, Negative Isolated Outputs

Similar to the single isolated output case of Figure 4-1, the total VDD-VEE is still set to +20 V as determined by the R_2 and R_4 divider with the midpoint connected to FBVDD (pin 34). However, the feedback pins, FBVDD (pin 34) and FBVEE (pin 33) are now separated and a second resistor divider, R_3 and R_5 is introduced with the midpoint connected to FBVEE (pin 33). R_3 and R_5 set the VEE regulation point anywhere within the range of 2.5 V<VEE<VDD-VEE. A capacitive divider between VDD and VEE establishes a virtual reference shown as COM at the midpoint. COM is the positive voltage reference with respect to VEE and the point where the VEE resistor

divider is connected. The selection of the capacitive divider will be detailed in the Capacitor Selection section. The FBVEE resistor divider is determined by selecting R_5, then R_3 can be calculated according to Equation 9.

$$R_3 = \frac{R_5 \times (\mathrm{COM} - \mathrm{VEE} - 2.5\ \mathrm{V})}{2.5\ \mathrm{V}} \tag{9}$$

Referencing the example circuit of Figure 5-1, the total regulated secondary-side voltage is VDD-VEE = +20 V, COM is desired to be +5 V with respect to VEE. Substituting COM = +5 V and VEE = 0 V (secondary-side reference point) into Equation 9 simplifies to R_3=R_5. For highest voltage setpoint accuracy, consider using 0.1% tolerance resistors, where the lower resistor, R_5, shares the same reference point as the UCC14240-Q1 internal voltage reference at VEEA (U1-35). For a dual isolated output configuration, the introduction of the C_1, C_5 capacitive divider redefines the VDD reference point compared to the single output configuration. VDD in the dual output configuration is now given as VDD = +20 V-COM = +20 V-(+5 V) = +15 V and VEE= 0 V-COM = 0 V-(+5 V) = -5 V. The UCC14240-Q1, dual positive and negative voltage rails established for biasing any SiC/IGBT gate driver IC with respect to COM are now defined as: VDD = +15 V, and VEE = -5 V.

NOTE: When probing hardware, do not attach oscilloscope voltage probe ground leads to COM. Connecting probe ground to COM can result in a failed UCC14240-Q1 start-up, since COM is floating and the oscilloscope is referenced to earth ground. All oscilloscope voltage probe measurements made on the UCC14240-Q1 secondary should be referenced to VEE.

6 Dual Positive Output Voltages

For some DC-DC applications, it can be desirable to have a positive VDD1 voltage and a second positive VDD2 voltage. The UCC14240-Q1 configuration shown in Figure 6-1, is an example of VDD1=+20 V and VDD2=+5 V. The settable range for each is 18 V<VDD1<25 V and 2.5 V<VDD2<VDD1. Applications could include driving a SiC between 0 V<V_{GS}<VDD1 (where VDD1 can be 18 V or greater) and using VDD2=5 V or 3.3 V to bias additional secondary-side logic circuits, CAN transceivers, isolated voltage or current sensors or providing secondary-side, digital isolator bias.

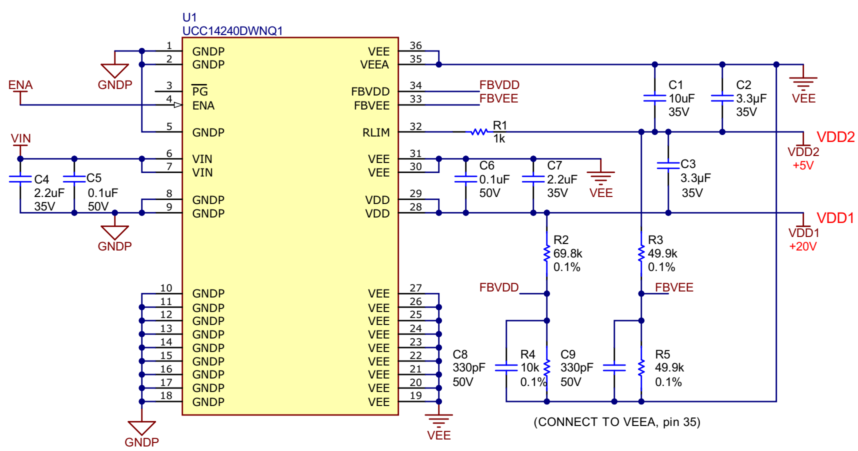

Figure 6-1. Dual Positive Isolated Outputs

7 Capacitor Selection

The UCC14240-Q1 input and output high-frequency decoupling capacitors should consist of a 2.2-µF ceramic capacitor in parallel with a 0.1-µF ceramic capacitor as shown in Figure 7-1 and Figure 7-2. The 0.1-µF capacitor should be placed closest to the IC pins and both capacitors should be rated for at least 1.5 times the applied voltage or a minimum voltage rating of 35 V. The UCC14240-Q1 feedback resistor dividers require a 330-pF ceramic, high-frequency, bypass capacitor in parallel with the lower resistor. The 330-pF bypass capacitors are shown in the schematics of Figure 4-1 through Figure 6-1 and should be placed as close as possible between FBVDD (U1-34) and VEEA (U1-35) and FBVEE (U1-33) and VEEA (U1-35).

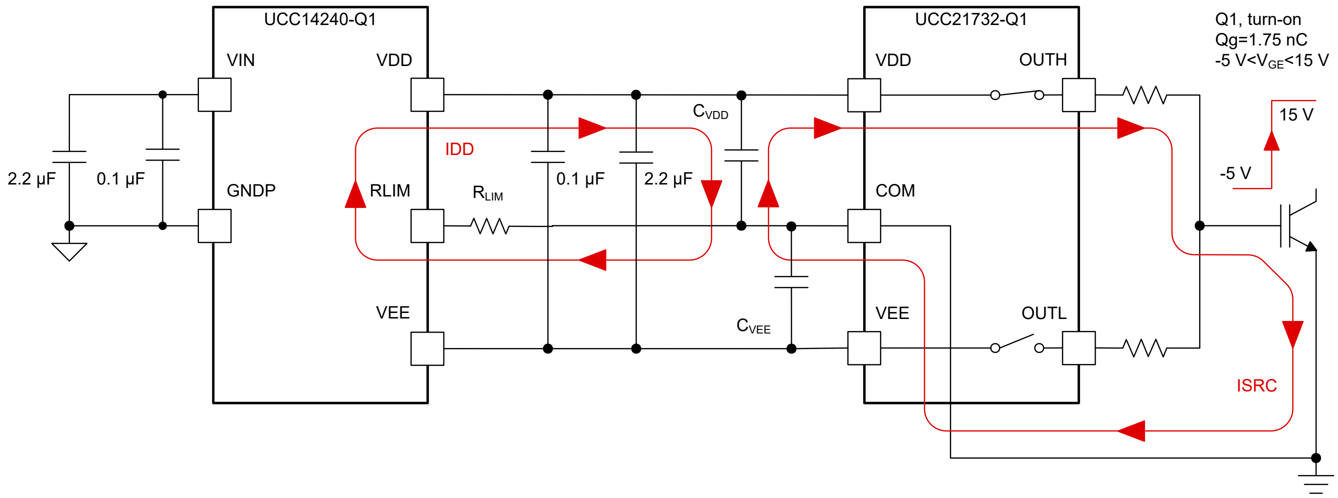

Figure 7-1. Turn-on Current Source

The circuits shown in Figure 7-1 and Figure 7-2 are illustrating source and sink current flow during turn-on and turn-off of an IGBT. The UCC14240-Q1 is providing dual positive and negative bias voltage to the UCC21732-Q1, ±10 A isolated, SiC/IGBT gate driver, driving an IGBT with 1.75 µC total gate charge. The diagrams have been simplified to highlight the functionality and selection of C_{VDD} and C_{VEE}. C_{VDD} and C_{VEE} are capacitors associated with the gate driver but also have a profound impact on the UCC14240-Q1 performance when using the dual, VDD/VEE output voltage configuration shown in Figure 5-1.

C_{VDD} is the UCC21732-Q1, VDD bulk capacitor supplying the required charge to Q_1 during turn-on and should be placed as close as possible to the gate driver pins. The total charge removed from C_{VDD} by ISRC must be replenished by IDD every switching cycle. The removal and replenishing of charge into C_{VDD} occur at the rate of the switching frequency of the IGBT and results in an unavoidable ripple voltage variation across C_{VDD}. Since the total charge is supplied by the series combination of C_{VDD} and C_{VEE}, assuming a desired ripple voltage limit of ΔV=500 mV_{PP}, the total required capacitance can be determined by Equation 10, where lower ripple voltage can be achieved at the cost of higher capacitance.

$$\frac{C_{VDD} \times C_{VEE}}{C_{VDD} + C_{VEE}} \geq \frac{Q_G}{\Delta V} = \frac{1.75\ \mu C}{500\ mV_{PP}} = 3.5\ \mu F \tag{10}$$

The equivalent capacitance, C_G, required according to the IGBT gate charge of 1.75 µC is significantly less compared to the capacitance required by Equation 11. Therefore, the capacitance required to maintain a desired ripple voltage will always dominate over the C_G required by a SiC/IGBT, as verified by 3.5 µF>>87.5 nF.

$$C_G \geq \frac{Q_G}{VDD - VEE} = \frac{1.75\ \mu C}{15\ V - (-5\ V)} = 87.5\ nF \tag{11}$$

During turn-on, the IGBT requires an amount of power from C_{VDD} which results in an equivalent amount of power delivered from the UCC14240-Q1 and is given by Equation 12 as:

$$P_{SRC} = P_{VDD} = Q_G \times (VDD - COM) \times F_{sw} = 1.75\ \mu C \times (15\ V - 0) \times 20\ kHz = 525\ mW \tag{12}$$

During turn-off, the total charge stored in the IGBT gate capacitance is removed by applying C_{VEE} (-5 V) in parallel with the IGBT, V_{GE}. The power removed from C_{VEE} during turn-off must also be replenished and delivered from the UCC14240-Q1 and is given by Equation 13 as:

$$P_{SNK} = P_{VEE} = Q_G \times (COM - VEE) \times F_{sw} = 1.75\ \mu C \times [0\ V - (-5\ V)] \times 20\ kHz = 175\ mW \tag{13}$$

The total dynamic power required, due to switching, is the sum of Equation 12 and Equation 13:

$$P_{SW} = P_{SRC} + P_{SNK} = (VDD - VEE) \times (Q_G \times F_{SW}) = 700\ mW \tag{14}$$

From the UCC21732-Q1 data sheet, the maximum I_{Q_VDD} of 5.9-mA is used to calculate the power required due to quiescent current as:

$$P_{IQ} = (VDD - VEE) \times I_Q = (20\ V - (-5\ V)) \times 5.9\ mA = 147.5\ mW \tag{15}$$

Combining P_{SW} and P_{IQ} gives the total required bias power according to Equation 16:

$$P_{BIAS} = P_{SW} + P_{IQ} = 700\ mW + 147.5\ mW = 847.5\ mW \tag{16}$$

The result of Equation 16 should be used to verify the required power is less than the maximum UCC14240-Q1 power of 1.5 W up to 105°C ambient temperature. For this example, the result is 847.5 mW<1.5 W.

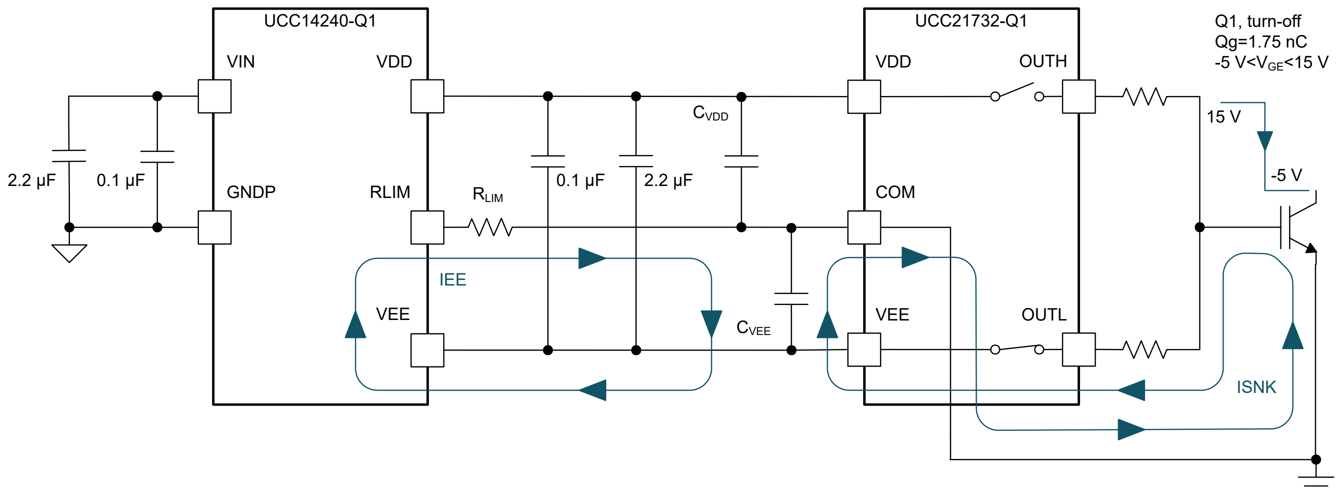

Figure 7-2. Turn-off Current Sink

Equation 10 can be rewritten as:

$$C_{VEE} = \frac{Q_G \times C_{VDD}}{(C_{VDD} \times \Delta V) - Q_G} \tag{17}$$

A second function of the C_{VDD}, C_{VEE} capacitive divider is to balance the midpoint COM voltage according to the desired value of negative VEE voltage relative to positive VDD voltage. The voltage divider formed by C_{VDD} and C_{VEE} results in:

$$C_{VEE} = \frac{C_{VDD} \times (VDD - COM)}{COM - VEE} \tag{18}$$

Setting Equation 17 equal to Equation 18 and solving for C_{VDD} gives:

$$C_{VDD} = \frac{Q_G}{\Delta V} \times \left[\frac{VDD - VEE}{VDD - COM}\right] = \frac{1.75\ \mu C}{500\ mV} \times \left[\frac{15\ V - (-5\ V)}{15\ V - 0\ V}\right] = 4.67\ \mu F \tag{19}$$

C_{VDD}=4.67 µF which can then be used to solve for C_{VEE} in Equation 20.

$$C_{VEE} = \frac{C_{VDD} \times (VDD - COM)}{COM - VEE} = \frac{4.67\ \mu F \times (15\ V - 0\ V)}{0\ V - (-5\ V)} = 14.1\ \mu F \tag{20}$$

It is worth repeating that C_{VDD} and C_{VEE} are the minimum total capacitance values required by VDD and VEE with respect to COM. Add appropriate de-rating and choose standard component values greater than the calculated minimum results shown, then adjust to maintain the correct C_{VDD} to C_{VEE} ratio according to Equation 20. Once the values are chosen, C_{VDD} and C_{VEE} can now be substituted into Equation 10 and Equation 19 to verify the selected capacitor values meet the desired ΔV, ripple voltage as well as setting the correct midpoint voltage established by Equation 19. It might be necessary to use parallel combinations of different capacitor component values to obtain the desired ratio.

Reducing ripple voltage, V_{CE} droop voltage or improving dynamic gate drive performance are a few possible reasons for increasing C_{VDD} capacitor values. In an effort to maintain the correct C_{VDD} to C_{VEE} capacitor divider ratio (3:1 in this example), it important to scale the value of the C_{VEE} capacitors to match any changes introduced to the C_{VDD} capacitor value. C_{VDD} capacitors should be 35-V or higher but C_{VEE} capacitors can be rated at lower voltage, appropriately de-rated to handle ~1.5x VEE. C_{VDD} and C_{VEE} capacitors should be surface mount, ceramic X7R or better dielectric, AEC-Q200 rated for the intended temperature demands of the application. When trying to achieve the minimum required capacitance, careful attention should be paid to the applied DC voltage vs capacitor rated working voltage, temperature, tolerance and dielectric type as shown in Figure 7-3 through Figure 7-5. Achieving optimal bias and gate driver performance requires that minimum calculated capacitance is met under all electrical and environmental operating conditions.

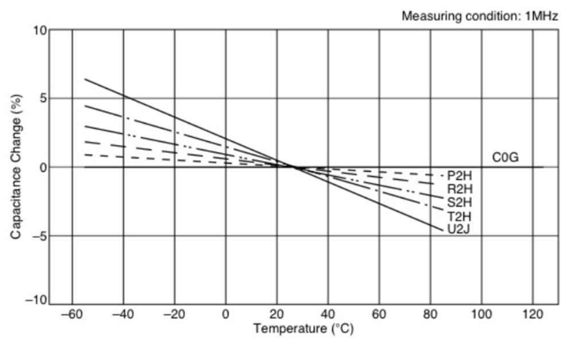

Figure 7-3. Ceramic Capacitor Temperature Characteristics

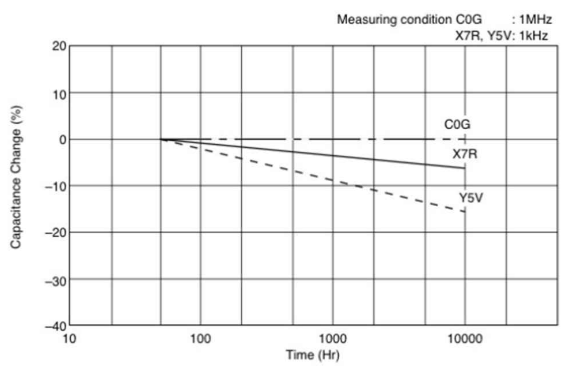

Figure 7-4. Ceramic Capacitor Aging Characteristics

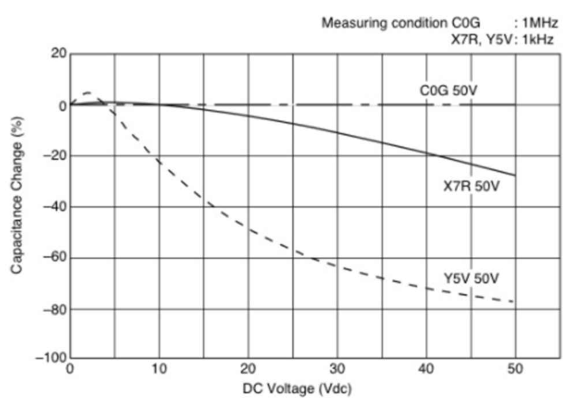

Figure 7-5. Ceramic Capacitor Applied DC Voltage Characteristics

8 R_{LIM} Current Limit Resistor

8.1 R_{LIM} Functional Description

To maintain accurate voltage regulation, charge mismatch between C_{VDD} and C_{VEE}, must be compensated by the UCC14240-Q1. This is accomplished by a simple, totem pole pair of asynchronous, internal switches depicted as S1 and S2 in Figure 8-1 and Figure 8-2. When the UCC14240-Q1 is configured for dual output, the primary purpose of the current limit resistor, R_{LIM}, is to limit the peak current through S1 during VDD current source and S2 during VEE current sink. R_{LIM} also has the secondary function of regulating the current necessary to maintain charge balance between C_{VDD} and C_{VEE}.

If the ideal C_{VDD} to C_{VEE} ratio were obtained, according to the voltage ratio outlined in the Capacitor Selection section, then VDD-VEE is regulated, COM-VEE is indirectly regulated and ILIM=0 A. However, C_{VDD} to C_{VEE} capacitor value mismatch due to temperature, tolerance, aging and applied DC voltage inevitably result in capacitor variation between ideal and actual component values. In addition, the source and sink quiescent current, I_Q, of the gate driver IC results in a small but significant charge imbalance between the C_{VDD} to C_{VEE} capacitor. The UCC14240-Q1 internal RLIM regulator helps to maintain tight voltage regulation better than 1.3% by compensating for errors caused by such instances.

8.2 R_{LIM} Dual Output Configuration

This section describes four cases resulting in C_{VDD} to C_{VEE} capacitor charge imbalance and how the RLIM function is used to compensate for the imbalance to maintain better than 1.3% voltage regulation.

8.2.1 C_{VEE} Above Nominal Value C_{VDD} Below Nominal Value

Consider the ILIM contribution for two cases of C_{VDD} to C_{VEE} capacitor value mismatch, while momentarily disregarding the additional impact of gate driver I_Q. The first case shown in Figure 8-1 illustrates the RLIM regulator sourcing current into the gate driver COM pin to compensate for the nominal values of C_{VEE} being higher and C_{VDD} being lower. In this case the voltage across C_{VEE} (COM-VEE) drifts lower resulting in ILIM sourcing current through R_{LIM} to restore equal capacitor charge balance.

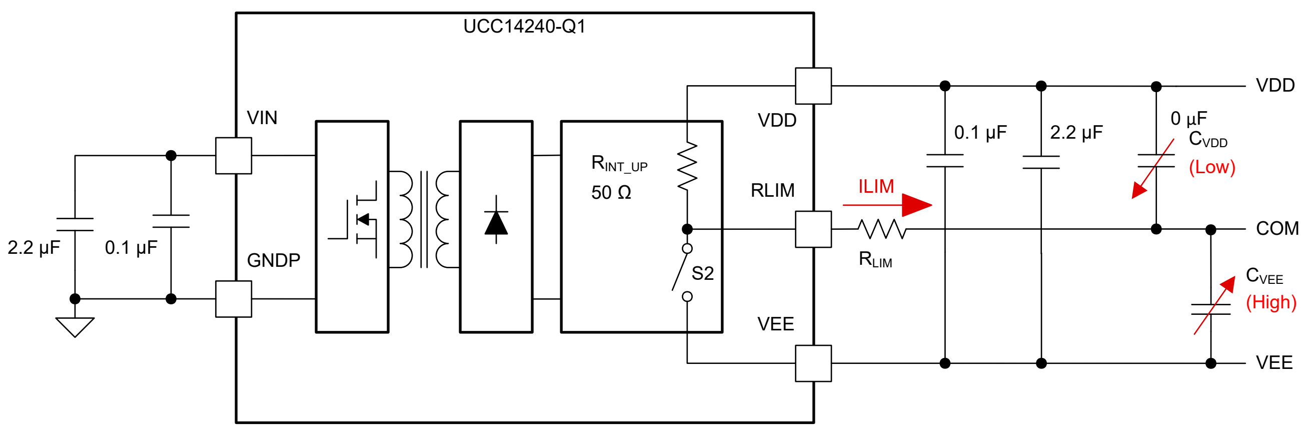

Figure 8-1. Case 1: ILIM Sourcing, C_{VEE} Higher, C_{VDD} Lower

The additional compensated charge, ΔQ_{C_UP}, as a result of the worst case expected capacitor variation ΔC_{VDD} and ΔC_{VEE} is given by Equation 21.

$$\Delta Q_{C\_UP} = Q_G \times \left[\frac{C_{VEE} \times (1 - \Delta C_{VEE})}{C_{VDD} \times (1 - \Delta C_{VDD}) + C_{VEE} \times (1 - \Delta C_{VEE})} - \frac{C_{VEE}}{C_{VDD} + C_{VEE}}\right] \quad (21)$$

The product of ΔQ_{C_UP} and the switching frequency, F_{SW}, can then be used to determine the ILIM source current given by Equation 22.

$$ILIM = \Delta Q_{C\_UP} \times F_{SW} \quad (22)$$

R_{LIM} is then determined by Equation 23 as.

$$R_{LIM} = \frac{VDD - COM}{ILIM} - R_{INT\_UP} \tag{23}$$

8.2.2 C_{VEE} Below Nominal Value C_{VDD} Above Nominal Value

The second case shown in Figure 8-2 illustrates the R_{LIM} regulator sinking current from the gate driver COM pin to compensate for the nominal values of C_{VEE} being lower and C_{VDD} being higher. In this case the voltage across C_{VEE} (COM-VEE) drifts higher resulting in ILIM sinking current through R_{LIM} to restore equal capacitor charge balance.

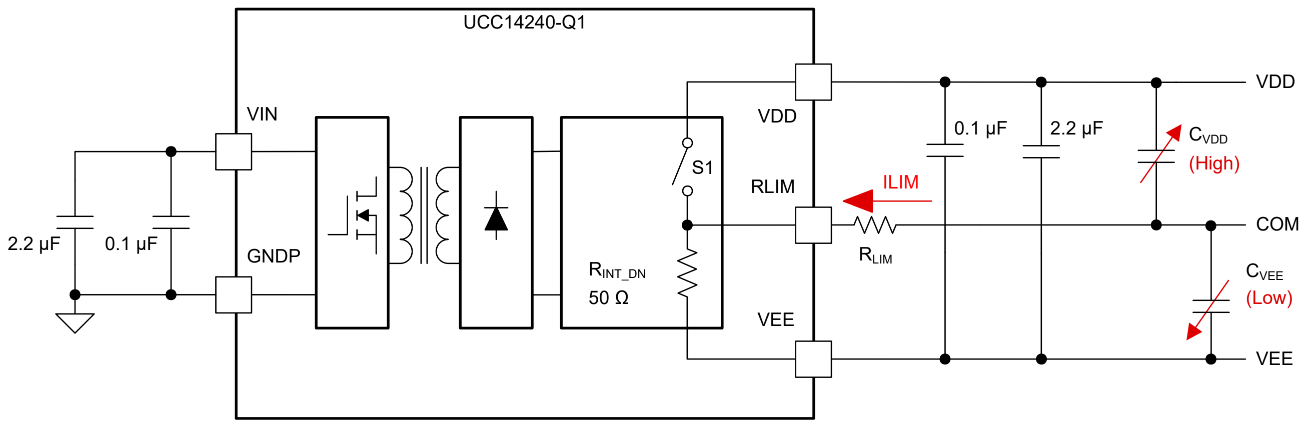

Figure 8-2. Case 2: ILIM Sinking, C_{VEE} Lower, C_{VDD} Higher

The additional compensated charge, ΔQ_{C_DN}, as a result of the worst case expected capacitor variation ΔC_{VDD} and ΔC_{VEE} is given by Equation 24.

$$\Delta Q_{C\_DN} = Q_G \times \left[\frac{C_{VDD} \times (1 - \Delta C_{VDD})}{C_{VDD} \times (1 - \Delta C_{VDD}) + C_{VEE} \times (1 - \Delta C_{VEE})} - \frac{C_{VDD}}{C_{VDD} + C_{VEE}}\right] \tag{24}$$

The product of ΔQ_{C_DN} and F_{SW} can then be used to determine the ILIM source current given by Equation 25.

$$ILIM = \Delta Q_{C\_DN} \times F_{SW} \tag{25}$$

R_{LIM} is then determined by Equation 26 as.

$$R_{LIM} = \frac{VDD - COM}{ILIM} - R_{INT\_DN} \tag{26}$$

8.2.3 Gate Driver Quiescent Current: I_{Q_VEE} > I_{Q_VDD}

Next, consider the ILIM contribution for two cases of imbalanced gate driver I_Q, while momentarily disregarding the impact C_{VDD} to C_{VEE} capacitor value mismatch (ΔC_{VDD} and ΔC_{VEE}). The first case shown in Figure 8-3 illustrates the RLIM regulator sourcing current into the gate driver COM pin to compensate for I_{Q_VEE}>I_{Q_VDD}. In this case the voltage across C_{VEE} (COM-VEE) drifts lower resulting in ILIM sourcing current through R_{LIM} to restore equal capacitor charge balance.

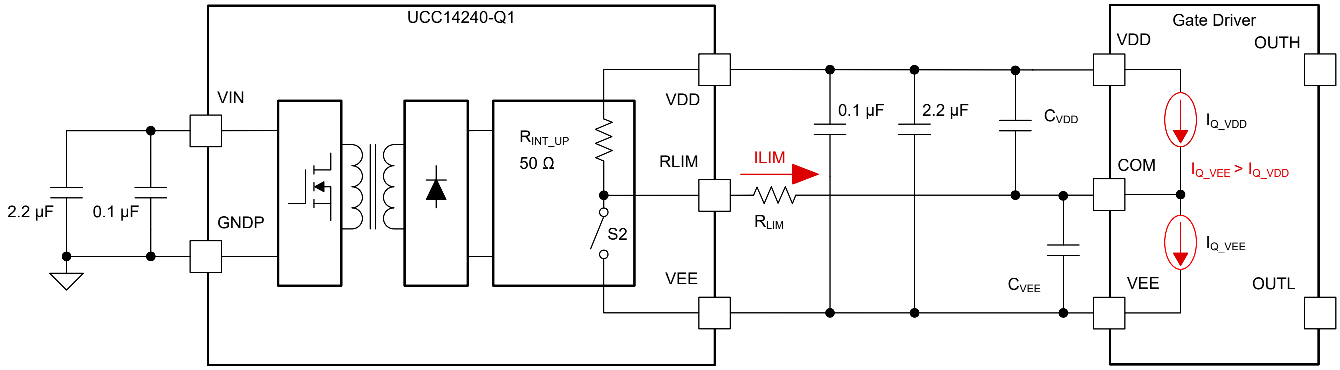

Figure 8-3. Case 3: $I_{Q\_VEE} > I_{Q\_VDD}$

The R_{LIM} resistor for the case that $I_{Q\_VEE} > I_{Q\_VDD}$ is calculated by Equation 27 where $ILIM = I_{Q\_VEE} - I_{Q\_VDD}$.

$$R_{LIM} = \frac{VDD - COM}{ILIM} - R_{INT\_UP} \tag{27}$$

8.2.4 Gate Driver Quiescent Current: $I_{Q\_VEE} < I_{Q\_VDD}$

The fourth case shown in Figure 8-4 illustrates the RLIM regulator sinking current from the gate driver COM pin to compensate for $I_{Q\_VEE} < I_{Q\_VDD}$. In this case, the voltage across C_{VEE} (COM-VEE) drifts higher resulting in ILIM sinking current through R_{LIM} to restore equal capacitor charge balance.

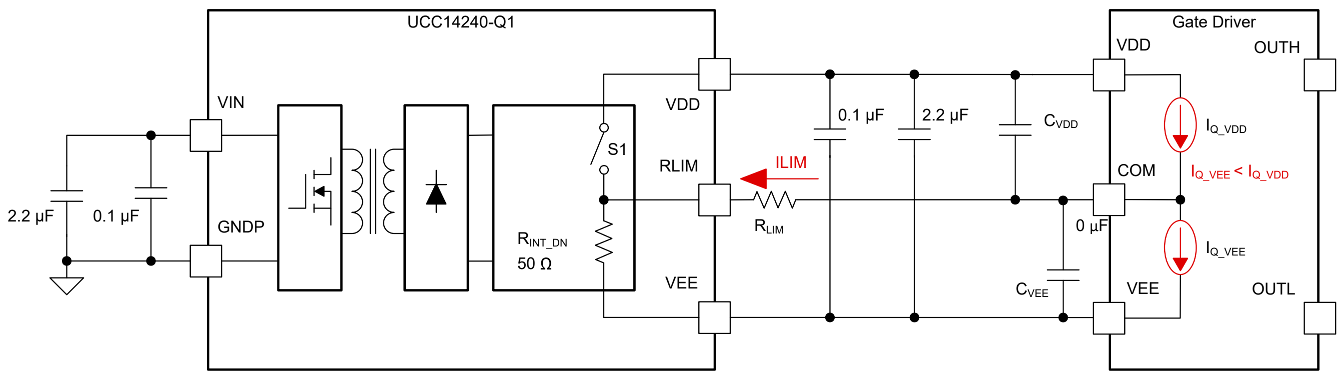

Figure 8-4. Case 4: $I_{Q\_VEE} < I_{Q\_VDD}$

The R_{LIM} resistor for the case that $I_{Q\_VEE} < I_{Q\_VDD}$ is calculated by Equation 28 where $ILIM = I_{Q\_VDD} - I_{Q\_VEE}$.

$$R_{LIM} = \frac{COM - VEE}{ILIM} - R_{INT\_DN} \tag{28}$$

8.2.5 C_{VEE} Above Nominal Value C_{VDD} Below Nominal Value: $I_{Q\_VEE} > I_{Q\_VDD}$

Finally, consider the ILIM contribution for the combined effect of C_{VDD} to C_{VEE} capacitor value mismatch and gate driver I_Q variation. The case shown in Figure 8-5 is the combination of case 1 (Figure 8-1) and case 3 (Figure 8-3) where the RLIM regulator is sourcing current into the gate driver COM pin. This is the worst case where the voltage across C_{VEE} (COM-VEE) drifts lower resulting in ILIM sourcing additional compensating current through R_{LIM} to restore equal capacitor charge balance.

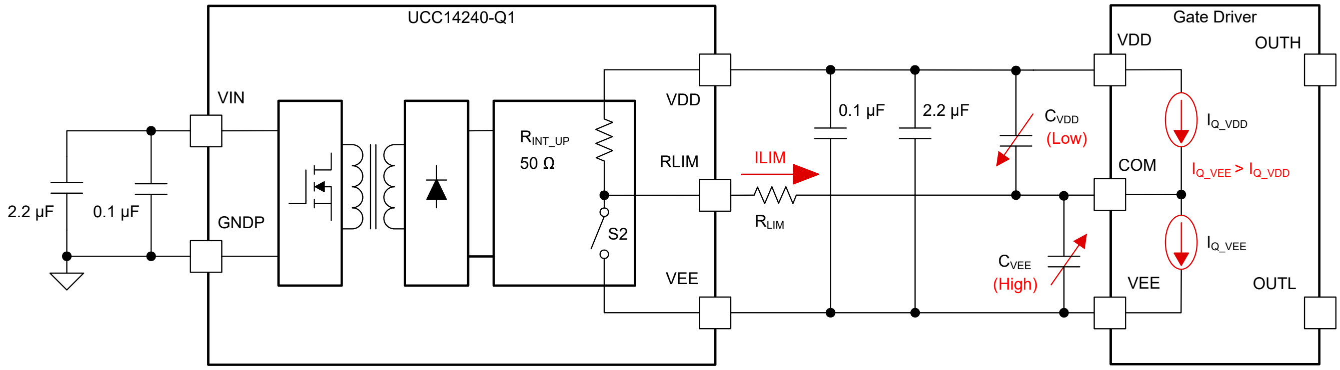

Figure 8-5. Case 1 and Case 3: C_{VEE} Higher, C_{VDD} Lower, $I_{Q\_VEE} > I_{Q\_VDD}$

The additional compensated charge, Δ_{QC_UP}, as a result of the worst case expected capacitor variation ΔC_{VDD} and ΔC_{VEE} is given by Equation 29 which is Equation 21 repeated here for completeness.

$$\Delta Q_{C\_UP} = Q_G \times \left[\frac{C_{VEE} \times (1 - \Delta C_{VEE})}{C_{VDD} \times (1 - \Delta C_{VDD}) + C_{VEE} \times (1 - \Delta C_{VEE})} - \frac{C_{VEE}}{C_{VDD} + C_{VEE}}\right] \tag{29}$$

R_{LIM} is calculated from Equation 30 and the power dissipated is given from Equation 31 where the total ILIM now consists of ΔQ_{C_UP} derived from the total capacitor variation and I_Q variation for the case that $I_{Q\_VEE} > I_{Q\_VDD}$.

$$R_{LIM} = \frac{VDD - COM}{ILIM} - R_{INT\_UP} = \frac{VDD - COM}{\Delta Q_{C\_UP} \times F_{SW} + \left(I_{Q\_VEE} - I_{Q\_VDD}\right)} - R_{INT\_UP} \tag{30}$$

$$P_{RLIM} = ILIM^2 \times R_{LIM} = \left[\Delta Q_{C\_UP} \times F_{SW} + \left(I_{Q\_VEE} - I_{Q\_VDD}\right)\right]^2 \times R_{LIM} \tag{31}$$

8.2.6 C_{VEE} Below Nominal Value C_{VDD} Above Nominal Value: $I_{Q\_VEE} < I_{Q\_VDD}$

The case shown in Figure 8-6 is the combination of case 2 (Figure 8-2) and case 4 (Figure 8-4) where the RLIM regulator is sinking current from the gate driver COM pin. This is the worst case where the voltage across C_{VEE} (COM-VEE) drifts higher resulting in ILIM sinking additional compensating current through R_{LIM} to restore equal capacitor charge balance.

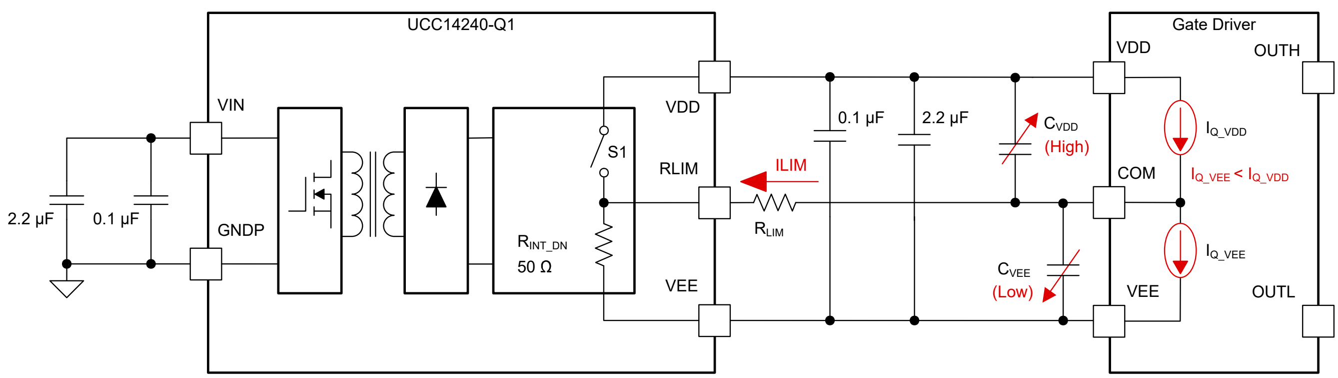

Figure 8-6. Case 2 and Case 4: C_{VEE} Lower, C_{VDD} Higher, $I_{Q\_VEE} < I_{Q\_VDD}$

The additional compensated charge, ΔQ_{C_DN}, as a result of the worst case expected capacitor variation ΔC_{VDD} and ΔC_{VEE} is given by Equation 32 which is Equation 24 repeated here for completeness.

$$\Delta Q_{C\_DN} = Q_G \times \left[\frac{C_{VDD} \times (1 - \Delta C_{VDD})}{C_{VDD} \times (1 - \Delta C_{VDD}) + C_{VEE} \times (1 - \Delta C_{VEE})} - \frac{C_{VDD}}{C_{VDD} + C_{VEE}}\right] \tag{32}$$

R_{LIM} is calculated from Equation 33 and the power dissipated is given from Equation 34 where the total ILIM now consists of ΔQ_{C_DN} derived from the total capacitor variation and I_Q variation for the case that $I_{Q\_VEE} < I_{Q\_VDD}$.

$$R_{LIM} = \frac{COM - VEE}{ILIM} - R_{INT\_DN} = \frac{COM - VEE}{\Delta Q_{C\_DN} \times F_{SW} + \left(I_{Q\_VDD} - I_{Q\_VEE}\right)} - R_{INT\_DN} \tag{33}$$

$$P_{RLIM} = ILIM^2 \times R_{LIM} = \left[\Delta Q_{C\_DN} \times F_{SW} + \left(I_{Q\_VDD} - I_{Q\_VEE}\right)\right]^2 \times R_{LIM} \tag{34}$$

If the selected value of R_{LIM} is too low, the peak IDD current can increase causing oscillations on VDD which can result in the UCC14240-Q1 entering an overload, shut-down condition. Conversely, if the value of R_{LIM} is too high, the charge rate of C_{VDD} and especially C_{VEE} will be slow due to a higher RC time constant. The result will appear as VDD-VEE reaching regulation much sooner compared to COM-VEE, resulting in VDD-COM voltage overshoot during start-up. Selecting C_{VDD} and C_{VEE} excessively larger than the results of Equation 19 and Equation 20 will exasperate the problem of slow COM-VEE response and VDD-COM voltage overshoot. Careful selection of C_{VDD}, C_{VEE} and R_{LIM} is important for optimizing the UCC14240-Q1 start-up and transient performance. Determining UCC14240-Q1 required component values is greatly simplified by using the *Excel UCC14240-Q1 Design Calculator Tool*, described in the UCC14240-Q1 Excel Design Calculator Tool section.

8.3 R_{LIM} Single Output Configuration

When the UCC14240-Q1 is configured for single output VDD operation, there is no C_{VDD}, C_{VEE} capacitive divider, R_{LIM} is applied as shown in Figure 8-7 and takes on a different role. During shutdown or VDD-VEE undervoltage fault, S2 is closed and R_{LIM} provides a controlled discharge path for C_{VDD} (and 2.2 µF // 0.1 µF) as shown by IDSCH. In this case, the minimum recommended R_{LIM} value of 1 kΩ should be used to safely limit IDSCH through the internal lower pull down, R_{INT_DN}.

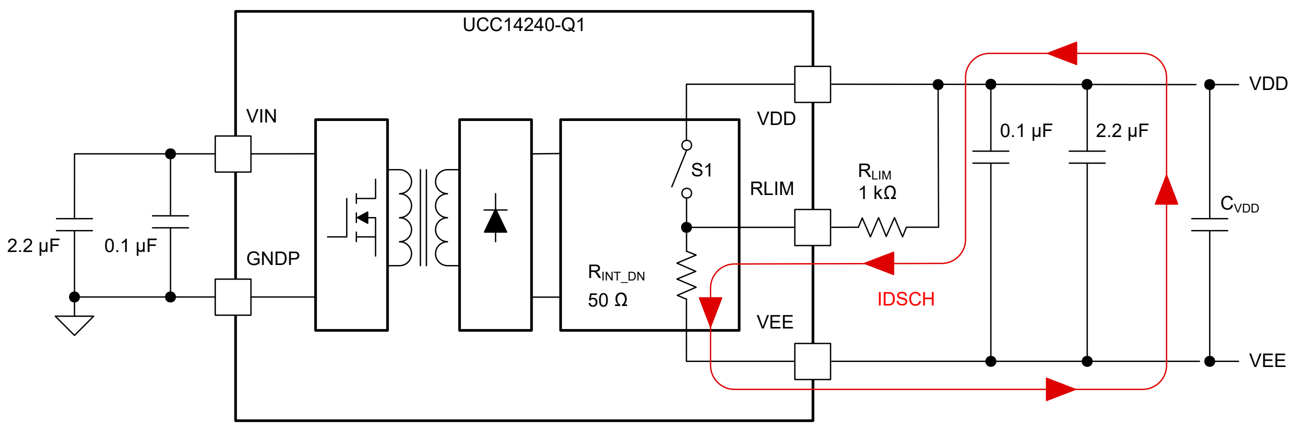

Figure 8-7. R_{LIM}, Single Output Configuration

As an example, using R_{LIM}=1 kΩ, assuming C_{VDD}=22 µF, VDD-VEE=20 V, the time it would take to discharge from the undervoltage fault detection threshold of 0.9x(VDD-VEE) down to 0.5 V would be ~91 ms, assuming there was no load present at VDD-VEE. Removing the charge on C_{VDD} assures the UCC14240-Q1 will not restart into a pre-biased load.

$$t_{DSCH} = -\left(R_{LIM} + R_{INT\_DN}\right) \times \left(C_{VDD} + 2.2\ \mu F\right) \times \ln\left[\frac{V_{C(t)}}{(VDD - VEE) \times 0.9}\right] = -(1\ k\Omega + 50\ \Omega) \times (22\ \mu F + 2.2\ \mu F) \times \ln\left[\frac{0.5\ V}{(20\ V - 0\ V) \times 0.9}\right] \approx 91\ ms \tag{35}$$

9 UCC14240-Q1 Excel Design Calculator Tool

The *UCC14240-Q1 Excel Design Calculator Tool* is available for download from the UCC14240-Q1 product folder on TI.com. The tool allows the user to input their known design parameters into the green boxes shown in Figure 9-1 and Figure 9-2. Based on user feedback and continuous improvement, the tool may be revised as needed, so users are encouraged to check the UCC14240-Q1 product folder for the latest version. The equations presented in this application report are used within the design calculator tool to simplify the task of quickly setting up the UCC14240-Q1.

The requested parameters are intuitive and each of the charge mismatch cases introduced in Section 8.2 are calculated to help select the proper R_{LIM} value covering all cases. The quiescent current, I_Q values will need to be obtained from the gate driver data sheet. Considering the worst-case mismatch, the *UCC21736-Q1 10-A Source and Sink Reinforced Isolated Single Channel Gate Driver for SiC/IGBT with Active Protection and High-CMTI* data sheet gives a maximum value of I_{Q_VDD}=4.7 mA (OUT(L)) and a minimum value of I_{Q_VEE}=830 µA (OUT(H)). Sometimes I_{Q_VEE} may not be specified in the gate driver data sheet. In such cases, only the difference between I_{Q_VDD} and I_{Q_VEE} is used to calculate R_{LIM} and I_{Q_VEE}=0 A can be used as a worst-case.

UCC14240-Q1 DESIGN CALCULATOR TOOL: DUAL OUTPUT (Ver. 4)

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UCC14240-Q1 1.5-W, 24-V VIN, High-Efficiency, > 3 kVRMS, Isolated DC/DC Module

CLEAR ALL USER INPUT CELLS BEFORE STARTING A NEW DESIGN

ALL GREEN CELLS ARE USER INPUTS

WHERE APPLICABLE, A RECOMMENDED VALUE IS GIVEN THAT WILL BE THE BEST CHOICE TO MEET THE GIVEN SPECIFICATION. IT IS IN THE BEST INTEREST OF THE USER TO USE A VALUE AS CLOSE AS POSSIBLE TO THE RECOMMENDED VALUE. FOR ACCURATE RESULTS, THE USER MUST ENTER THE ACTUAL VALUE USED IN THE APPROPRIATE CELL.

DESIGN REQUIREMENTS			
Differential voltage between VDD and VEE, VDD - VEE =	20.0	V	
Differential voltage between COM and VEE, COM - VEE =	5.0	V	
Total gate charge of power switch, Qgtot =	1.75	µC	
Switching frequency of gate driver load, f_{SW} =	20	kHz	
Quiescent current of the gate driver from (VDD – COM), $I_{Q\_DRIVER\_VDD}$	4.7	mA	Includes the operating current of gate driver without switching
Quiescent current of the gate driver from (COM – VEE), $I_{Q\_DRIVER\_VEE}$	0	mA	
Bottom feedback resistor between FBVDD and VEE, R_2	10	kΩ	
Bottom feedback resistor between FBVEE and VEE, R_4	10	kΩ	
Desired AC gate-switching ripple between VDD and VEE, V_{PP_MAX}	0.5	V	Respect to VDD-VEE
Min. energy-storage capacitance between VDD and COM, $C_{OUT2(MIN)}$	4.67	µF	Based on above parameters
Selected energy-storage capacitance between VDD and COM, C_{OUT2}	7.5	µF	Choose ≥ $C_{OUT2(MIN)}$. Note (1)
Max. component tolerance of C_{OUT2}	20	%	
Min. component tolerance of C_{OUT2}	-20	%	
Max. component tolerance of C_{OUT3}	20	%	
Min. component tolerance of C_{OUT3}	-20	%	
Max. RLIM current to overcome capacitance variation, I_{RLM_CAP}	-2.9	mA	Positive means out of RLIM pin Negative means into RLIM pin
Max. RLIM current to overcome capacitance variation & differential I_Q	-7.6	mA	Positive means out of RLIM pin Negative means into RLIM pin
Output power contribution from gate driver switching	0.7	W	
Output power contribution from gate driver quiescent current	0.094	W	
Output power contribution from capacitor mismatch current (I_{RLM_CAP})	0.00	W	
Total output power requirement not RLIM regulator loss, P_O =	0.79	W	1.5W capability for 105°C Ambient

Figure 9-1. UCC14240-Q1 Design Tool: Design Inputs (Green)

As highlighted in Figure 9-2, there are two selectable tabs available at the bottom of the design tool, allowing the user to configure the UCC14240-Q1 for either dual or single output, as shown in Figure 5-1 and Figure 4-1.

RECOMMENDED COMPONENT VALUE FROM DESIGN REQUIREMENTS			
Top feedback resistor between VDD and FBVDD, R_1 =	70	kΩ	
Top feedback resistor between COM and FBVEE, R_3 =	10	kΩ	
Min. decoupling capacitance between COM and VEE, $C_{OUT3(MIN)}$ =	22.5	µF	Note (1)
Max. R_{LIM} resistance, $R_{LIM(MAX)}$ =	606.5	Ω	
Selected R_{LIM} value, R_{LIM} =	511	Ω	Choose slightly lower than $R_{LIM(MAX)}$ Note (2)
Power loss of selected R_{LIM}, P_{RLIM} =	0.030	W	< Max. power limit of R_{LIM}

OTHER RECOMMENDED COMPONENT VALUE		
Filter capacitor between FBVDD and VEE, C_{FBVDD} =	330	pF
Filter capacitor between FBVEE and VEE, C_{FBVEE} =	330	pF
Decoupling capacitor between VDD and VEE, C_{OUT1} =	2.2 // 0.1	µF
Decoupling capacitor between VIN and GNDP, C_{IN} =	2.2 // 0.1	µF

Note (1): Achieve the minimum required capacitance, careful attention should be paid to the applied DC voltage vs. capacitor rated working voltage, temperature, tolerance and dielectric type.
Note (2): RLIM regulator efficiency will be impaired if R_{LIM} is chosen much lower than $R_{LIM(MAX)}$.

Dual Output | Single Output

Figure 9-2. UCC14240-Q1 Design Tool: Dual vs. Single Output

10 Thermal Considerations

10.1 Thermal Resistance

The UCC14240-Q1 data sheet (section 6.4) specifies traditional thermal resistance parameters based on joint electron device engineering council (JEDEC) test standards used to derive $R_{\Theta JA}$ and $R_{\Theta JC}$ for a single die semiconductor package. The junction-to-ambient thermal resistance, $R_{\Theta JA}$, is most often assumed valid for determining the junction temperature, T_J, as:

$$T_J = T_A + \left(R_{\Theta JA} \times P_D\right) \tag{36}$$

Where T_A is the ambient temperature, $R_{\Theta JA}$, is the junction-to-ambient thermal resistance found in the UCC14240-Q1 data sheet and P_D is the power dissipation determined from the UCC14240-Q1 efficiency curves, also published in the data sheet. The problem with this approach is that $R_{\Theta JA}$ is determined based on the JEDEC PCB design standard for a given IC package. The derivation of $R_{\Theta JA}$ carries strong dependence upon chip size, pad size, environmental conditions and PCB design of copper pours, copper thickness, etc. The PCB used in a traction inverter, will most assuredly be nothing like the JEDEC PCB used to characterize $R_{\Theta JA}$.

As a method for determining T_J based on measuring case temperature, T_C, and knowing the total power dissipation, $R_{\Theta JC}$, is commonly used as:

$$T_J = T_C + \left(R_{\Theta JC} \times P_D\right) \tag{37}$$

Using T_C to determine T_J is valid when it can be assumed that the dissipated power converts heat to energy that is mostly radiated off the top surface of a plastic IC package. The T_J measurement technique is useful for legacy or military metallic packages or packages with metal top side cooling. However, inaccuracies are unavoidable when applying $R_{\Theta JC}$ to plastic packages. The UCC14240-Q1 is designed to extract heat through the package lead frame to the PCB introducing further discrepancies to the assumption that heat energy generated from inside the package is accurately represented by measuring the top side surface temperature, T_C.

10.2 Junction-to-Top Thermal Characterization Parameter

A more accurate thermal metric given by Ψ_{JT} can be used to closely predict junction temperature based on measuring T_C. Unlike $R_{\Theta JC}$, Ψ_{JT} is measured using the UCC14240EVM-052 evaluation module (EVM) that more closely represents how the IC is expected to be used in a real-world PCB design. The EVM can therefore be used to estimate IC junction temperature with reasonable accuracy for packages mounted in a non-JEDEC environment. This thermal metric has been adopted by the industry under the JEDEC standard (JESD51-2) and since Ψ_{JT} is not a true thermal resistance, it is measured by the Greek letter psi (Ψ) to differentiate it from theta (Θ). The calculation for determining T_J from Ψ_{JT} gives a more accurate result and is similar in form to $R_{\Theta JA}$ given in Equation 37.

$$T_J = T_C + \left(\Psi_{JT} \times P_D\right) \tag{38}$$

$R_{\Theta JA}$ and Ψ_{JT} are thermal parameters based on test standards defined and developed for a single die IC package. An extension of single die package standards was introduced in JESD51-31 to include thermal test methods covering multi-die packages. However, UCC14240-Q1 is an isolated, DC-DC multi-source package (MSP) containing a primary and secondary die *and* an integrated planar transformer consisting of a primary and secondary transformer winding. Due to the nature of the MSP, a single set of JEDEC standards cannot be used to characterize the UCC14240-Q1. Since T_J for an MSP doesn't carry the same meaning as a single die or even a multi-die IC, the two die and two transformer windings are treated as four separate potential sources of heat generation and a thermal matrix is derived which accurately describes the temperature relationship between each of the four internal elements mentioned.

The thermal matrix is a system of linear equations written into a 4x4 matrix and for the purpose of deriving the UCC14240-Q1 data sheet thermal parameters is given by Equation 39.

$$\begin{bmatrix} T_1 \\ T_2 \\ T_3 \\ T_4 \end{bmatrix} = \begin{bmatrix} R_{11} & R_{12} & R_{13} & R_{14} \\ R_{21} & R_{22} & R_{23} & R_{24} \\ R_{31} & R_{32} & R_{33} & R_{34} \\ R_{41} & R_{42} & R_{43} & R_{44} \end{bmatrix} \cdot \begin{bmatrix} P_1 \\ P_2 \\ P_3 \\ P_4 \end{bmatrix} \tag{39}$$

Where the nomenclature of Equation 39 is defined as:

- 1, 2, 3, 4 denote primary die, secondary die, primary winding and secondary winding, respectively
- T is the die or transformer temperature rise
- P is power dissipation
- R is thermal resistance with subscript as follows:
  - R_{11} is temperature rise per unit power (°C/W) of primary die due to dissipation from primary die
  - R_{12} is temperature rise per unit power (°C/W) of primary die due to dissipation from secondary die
  - R_{13} is temperature rise per unit power (°C/W) of primary die due to dissipation from primary transformer winding
  - R_{14} is temperature rise per unit power (°C/W) of primary die due to dissipation from secondary transformer winding

The model represented by the thermal matrix is simulated using the EVM in 125°C still ambient air. Knowing the predicted temperature and power dissipation values, the thermal resistance numbers are determined by solving the four equations in the thermal matrix. It is not expected that the user would attempt to validate the distributed thermal matrix solution but rather, it is presented here simply to outline the procedure used to establish confidence in the lumped thermal parameters published in the data sheet.

The maximum temperature contribution inside the UCC14240-Q1 is coming from the internal transformer windings. Since T_J is the primary concern, the transformer is allowed to rise to a temperature that can exceed 150°C. The heat generated from the transformer flows through the thermal impedance related to the primary and secondary die as determined by the thermal matrix. The cumulative resulting temperatures at the primary and secondary dies are monitored to shut down the UCC14240-Q1 around 160°C and maintain T_J < 150°C.

Measuring the case temperature with a thermal camera and calculating the IC power dissipation, we can have high confidence for estimating the maximum T_J according to Equation 38.

10.3 Thermal Measurement and T_J Calculation Example

For the UCC14240-Q1 used in an EVM operating at VIN=24 V, VDD-VEE=20 V and POUT=1.62 W with η=57%, the power dissipation is determined as:

$$P_D = P_{OUT} \times \left(\frac{1}{\eta} - 1\right) = 1.62\ \mathrm{W} \times \left(\frac{1}{0.57} - 1\right) = 1.22\ \mathrm{W} \tag{40}$$

The maximum case temperature is measured as T_C=61°C at T_A=26°C ambient and the resulting thermal image is shown in Figure 10-1.

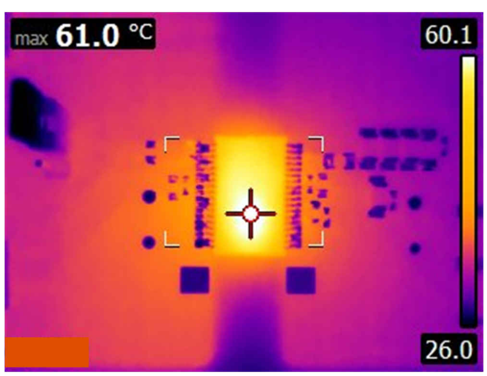

Figure 10-1. UCC14240-Q1 Max Case Temperature, POUT=1.62 W

Using the Ψ_{JT} thermal metric that was derived from the EVM closely representing how the UCC14240-Q1 PCB is expected to be designed, we obtain a T_J of 81.25°C as shown in Equation 41. Applying Ψ_{JT} is therefore considered the most accurate method for estimating T_J.

$$T_J = T_C + (\Psi_{JT} \times P_D) = 61°C + (16.6 ^{°C}/_{W} \times 1.22\ W) = 81.25°C \tag{41}$$

Compare to applying the $R_{\Theta JC}$ thermal resistance extracted from the JEDEC PCB which has less copper *heat sink*, no vias and thin copper traces extending from each IC pin, we obtain a T_J of 95.7°C as shown in Equation 42. The error in this result is mostly attributed to the PCB mismatch between the JEDEC PCB and the EVM as well as the thermal interface between the measured case temperature and die temperature.

$$T_J = T_C + (R_{\Theta JC} \times P_D) = 61°C + (28.5 ^{°C}/_{W} \times 1.22\ W) = 95.7°C \tag{42}$$

Finally, applying the $R_{\Theta JA}$ thermal resistance, also extracted from the JEDEC PCB, which has less copper *heat sink*, no vias and copper *fingers* extending from each IC pin, we obtain a T_J of 89.8°C as shown in Equation 43. This result also assumes the error between the JEDEC PCB and the EVM but does not rely on measured case temperature and more closely agrees with Equation 43.

$$T_J = T_A + (R_{\Theta JA} \times P_D) = 26°C + (52.3 ^{°C}/_{W} \times 1.22\ W) = 89.8°C \tag{43}$$

11 Enable (ENA) and Power Good (/PG)

The UCC14240-Q1 includes a primary referenced, 5-V TTL and 3.3-V LVTTL logic compatible, active-high enable function. Forcing ENA low disables the device, and places it in a non-switching standby mode where current consumption is reduced to less than 500 µA. Pulling the ENA pin high, above the 2-V threshold, activates normal device functionality. The ENA pin has a weak internal pull-down resistor, so the ENA pin floats to the disable state if the pin is left open. If ENA is not used it should be pulled high a voltage between 2.5 V<V_{ENA}<5.5 V. Care should be taken to assure V_{ENA} does not exceed 5.5 V_{MAX}.

The active-low, power good (/PG) pin is an open-drain output that indicates when the UCC14240-Q1 has no faults present and the output voltages are within ±10% of their regulation setpoints. Connect a pull-up resistor (>1 kΩ) from the /PG pin to either a 5-V or 3.3-V logic rail. For applications not using the /PG signal, /PG can be connected directly to GNDP.

The start-up waveforms in Figure 11-1 show the expected behavior of /PG relative to ENA. The input voltage (VIN=24 V, not shown) is already present and the UCC14240-Q1 is activated by ENA going high. The measured time between ENA high and /PG low is ~3.75 ms but can vary according to the time required for the isolated output voltages to be within ±10% of the set regulation value. The longer time required for COM-VEE to reach regulation relative to VDD-VEE results in the slight VDD-COM overshoot but this is happening before /PG reaches its active-low state. This emphasizes the importance of not switching the gate driver until /PG is in the active-low state. Note that the waveforms introduced here, were captured from the UCC14240EVM-052 EVM. *Using the UCC14240EVM-052 for Biasing Traction Inverter Gate Driver ICs Requiring Single, Positive or Dual, Positive/Negative Bias Power* is the EVM User's Guide containing the schematic, PCB details and measured performance data.

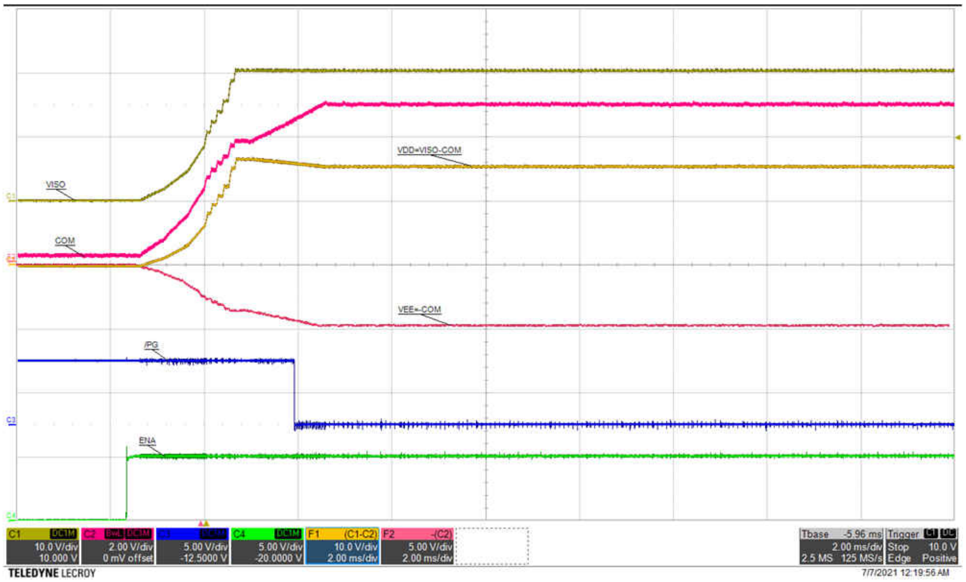

Figure 11-1. Start-up: VIN=24 V, IDD=80 mA, (top: VISO (VDD-VEE), 10V/div, mid-1: COM, 2V/div, mid-2: VDD=VISO-COM, 10V/div, mid-3: VEE=-COM, 5V/div, mid-4: /PG, 5V/div, bot: ENA, 5V/div), time = 2ms/div unless otherwise noted.

Conversely, the shut-down waveforms in Figure 11-2 show that as soon as ENA is pulled low, the UCC14240-Q1 output voltage are discharged in a controlled manner and /PG transitions high with almost no delay relative to ENA.

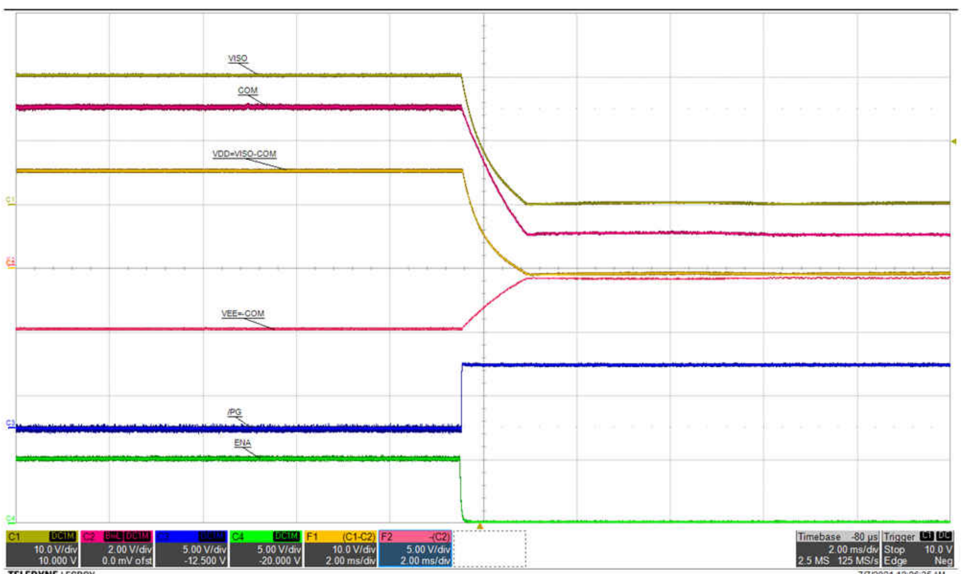

Figure 11-2. Shutdown: VIN=24 V, IVDD=80 mA, (top: VISO (VDD-VEE), 10V/div, mid-1: COM, 2V/div, mid-2: VDD=VISO-COM, 10V/div, mid-3: VEE=-COM, 5V/div, mid-4: /PG, 5V/div, bot: ENA, 5V/div), time = 2ms/div unless otherwise noted.

12 PCB Layout Considerations

Minimal external components mean easier, more direct PCB routing occupying less PCB area. Proper PCB layout is important to achieve optimum electrical and thermal performance. Automotive systems taking advantage of the high-performance features offered by the UCC14240-Q1 are likely to use multi-layer PCB designs. It is recommended to plan for at least a four-layer PCB design with 2-ounce copper preferred. The following thought given in terms of component placement and routing priority should also be applied as best as possible.

1. Place the 2.2-µF and 0.1-µF decoupling capacitors as close as possible to the input and output device pins with the 0.1-µF bypass capacitors closest to the IC pins. For the input, place the capacitor between pins 6, 7 (VIN) and pins 1, 2, 5, 8-18 (GNDP). For the isolated output, place the capacitor(s) between pin 28, 29 (VDD) and pins 19-27, 30-31, 35-36 (VEE). This location is of particular importance to the input decoupling capacitor, because this capacitor supplies the transient current associated with the fast switching waveforms of the power drive circuits.
2. Because the device does not have a thermal pad for heat-sinking, heat is extracted through the respective GND pins. Ensure that enough copper – preferably a connection to the ground plane – is present on GNDP and VEE pins for best heat-sinking.
3. If space and layer count allow, it is also recommended to connect the VIN, GNDP, VDD, RLIM, and VEE pins to internal ground or power planes through multiple vias of adequate size. Alternatively, make traces for these nets as wide as possible to minimize losses.
4. TI also recommends grounding the no-connect pins (NC) to their respective ground planes. For single output option pins 32 and 34, connect to VEE. This will allow more continuous ground planes and larger thermal mass for heat-sinking.
5. A minimum of four layers is recommended to allow sufficient internal layer GND shielding and low thermal impedance vias connecting the top and bottom layers for heat sinking the UCC14240-Q1. Inner layers can be used to create a high-frequency, common-mode stitch capacitor between GNDP and VEE, which in turn mitigates radiated emissions. An example showing the design of an internal PCB stitch capacitor can be found in the *UCC12050EVM-022 EVM User's Guide*.
6. Pay close attention to the spacing between primary ground plane (GNDP) and secondary ground plane (VEE) on the PCB's outer layers. The effective creep-age and or clearance of the system will be reduced if the two ground planes have a lower spacing than that of the UCC14240-Q1 package.
7. To ensure isolation performance between the primary and secondary side, avoid placing any PCB traces or copper below the UCC14240-Q1 device.

Additional PCB guidance can be found within the *UCC14240EVM-052 User's Guide*.

13 Reference Design Example

The *PMP22817A* reference design solution operates from a nominal 12-V input and includes a SEPIC pre-regulator, UCC14240-Q1 isolated bias converter and *UCC5870-Q1 30-A Isolated IGBT/SiC MOSFET Gate Driver with Advanced Protection Features for Automotive Applications* .

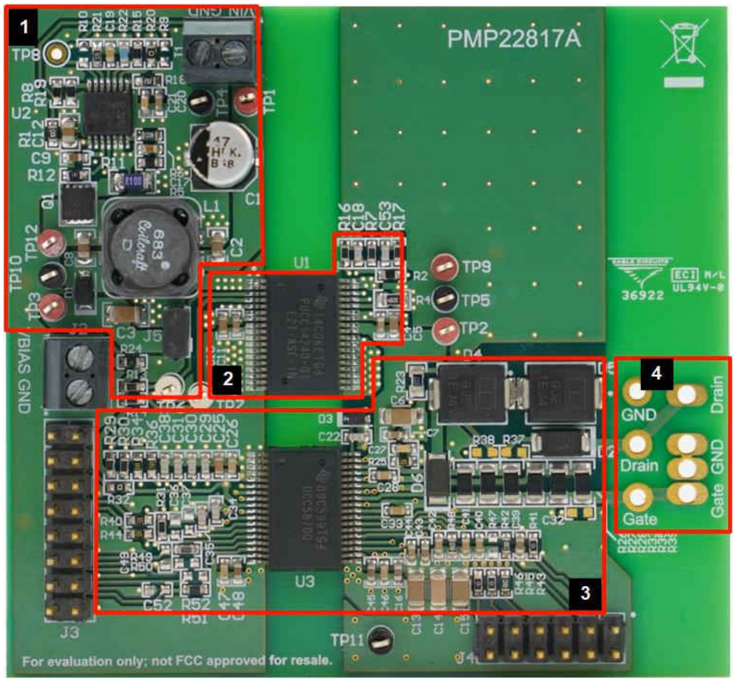

Figure 13-1. Single Channel SiC/IGBT Gate Drive Solution

The partitions outlined in Figure 13-1 are defined as:

1. *LM5156-Q1*: 12-V (6 V<12 V<42 V) to 24-V SEPIC pre-regulator
2. *UCC14240-Q1*: 24-V to +15-V, -5 V isolated bias supply
3. *UCC5870-Q1*: 30-A isolated gate driver for IGBT/SiC (plus digital interface)
4. Plated through-holes can accommodate 3-pin, TO-220 or 4-pin kelvin discrete IGBT/SiC packages or attached flying leads to drive IGBT/SiC modules

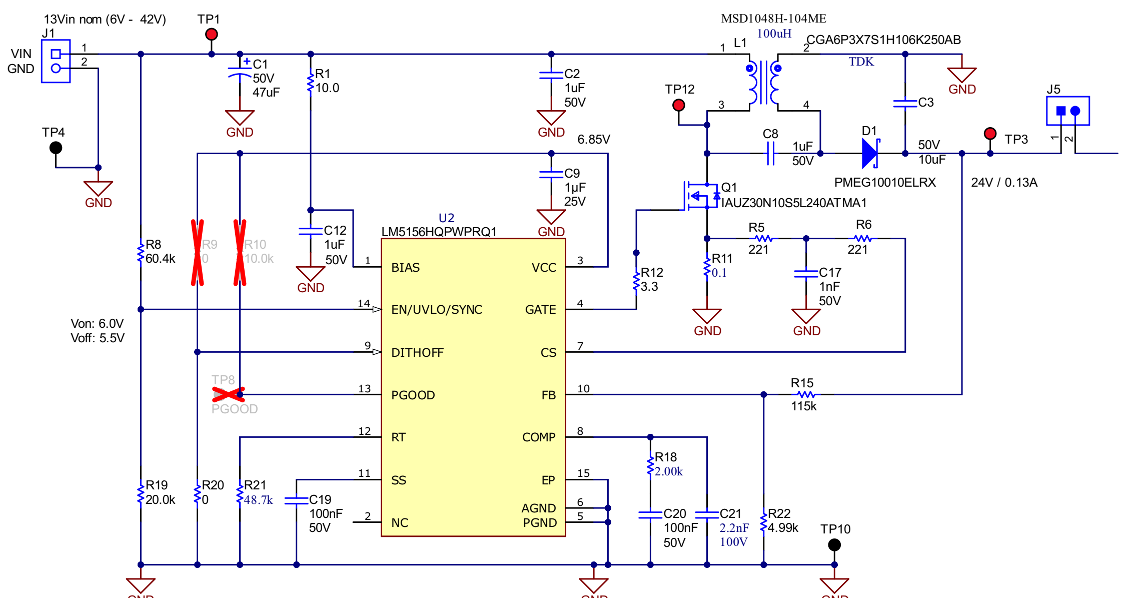

Figure 13-2. LM5156-Q1, 12-V to 24-V SEPIC Pre-regulator

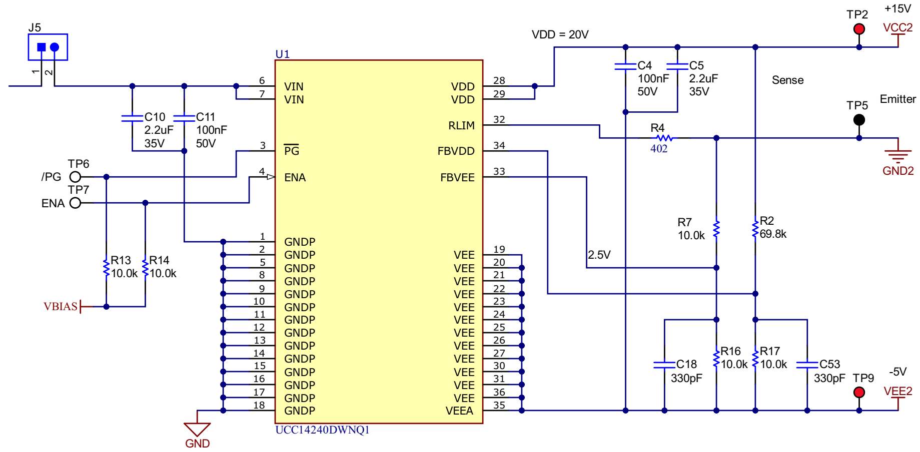

Figure 13-3. UCC14240-Q1, 24-V to +15-V, -5-V Isolated Bias Supply

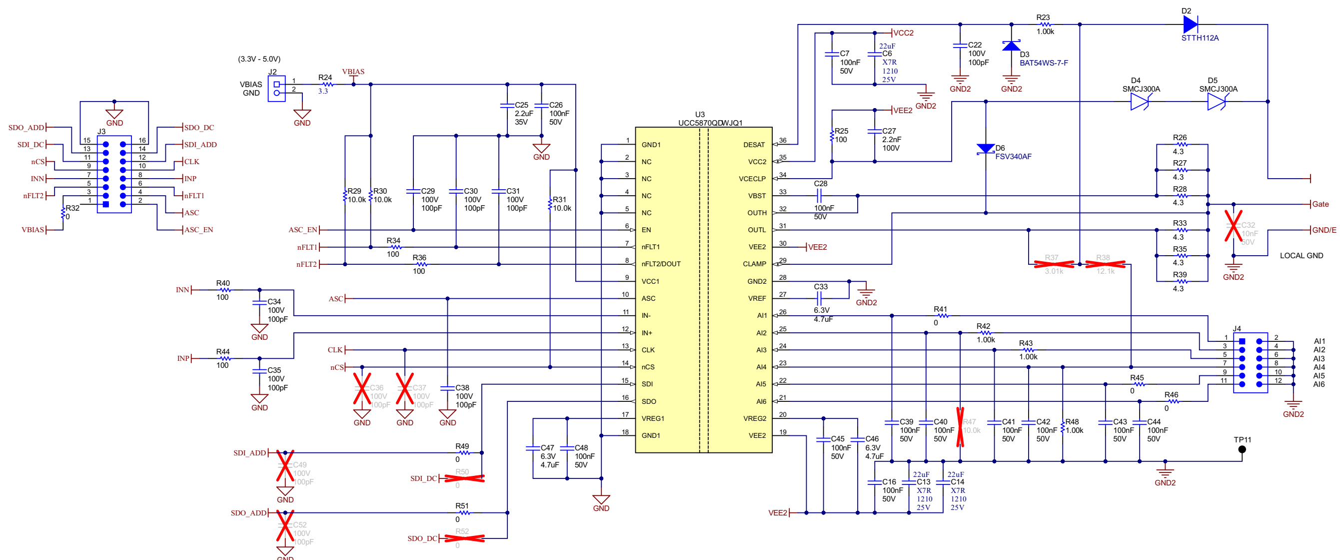

Figure 13-4. UCC5870-Q1, 30-A, Isolated IGBT/SiC Gate Driver

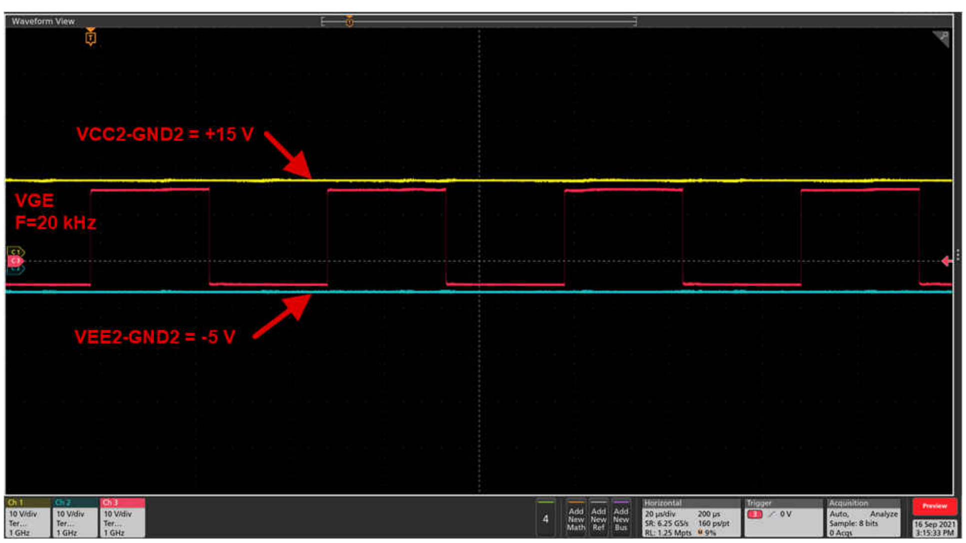

Figure 13-5. PMP22817A Steady-state Switching

14 Summary

Distributed gate drive bias architectures offer the highest level of performance, reliability and fault detection required by EV, HEV automotive propulsion and battery management systems. By integrating the transformer and control functions into a low-profile SOIC package, the *UCC14240-Q1 1.5-W, 24-V VIN, High-Efficiency, > 3 kVRMS, Isolated DC-DC Module* eases the challenge of providing dedicated bias power to each IGBT/SiC gate driver location. The UCC14240-Q1 provides isolated, positive and negative voltage rails and is easily configurable to meet the needs of different IGBT/SiC power and voltage requirements. Ease of use, low component count, high reliability, high power density, compatibility with TI Isolated Gate Drivers and scalability make UCC14240-Q1 the smart choice for EV, HEV HV bias supply applications.

15 References

1. Texas Instruments, *UCC14240-Q1 1.5-W, 24-V VIN, High-Efficiency, > 3 kVRMS, Isolated DC-DC Module* data sheet.
2. Texas Instruments, *UCC25800-Q1 Ultra-low EMI Transformer Driver for Isolated Bias Supplies* data sheet.
3. Texas Instruments, *UCC21732-Q1 10-A Source/Sink Reinforced Isolated Single Channel Gate Driver for SiC/IGBT with Active Protection, Isolated Analog Sensing and High-CMTI* data sheet.
4. Texas Instruments, *UCC280x-Q1 Low-Power BiCMOS Current-Mode PWM Controllers* data sheet.
5. Texas Instruments, *UCC14240-Q1 Excel Design Calculator Tool*, 2022, UCC14240-Q1 design tool.
6. Texas Instruments, *UCC21736-Q1 10-A Source and Sink Reinforced Isolated Single Channel Gate Driver for SiC/IGBT with Active Protection and High-CMTI* data sheet.
7. Texas Instruments, *Using the UCC14240EVM-052 for Biasing Traction Inverter Gate Driver ICs Requiring Single, Positive or Dual, Positive/Negative Bias Power* user's guide.
8. Texas Instruments, UCC14240EVM-052, UCC14240-Q1 Evaluation Module for 1.5-W Dual Output Isolated DC-DC Converter Gate Driver Bias.
9. Texas Instruments, Darvin Edwards, Hiep Nguyen, *Semiconductor and IC Package Thermal Metrics* application report.
10. Texas Instruments, UCC12050EVM-022, UCC12050DVE Isolated DC-DC Converter Evaluation Module.
11. Texas Instruments, *UCC12050EVM-052 User's Guide* user's guide.
12. Texas Instruments, *UCC12050 High-Density, Low-EMI, 5-kVRMS Reinforced Isolation DC/DC Module* data sheet.
13. Texas Instruments, *PMP22817A Reference Design*.
14. Texas Instruments, *LM5156x-Q1 2.2-MHz Wide VIN 65-V Non-synchronous Boost/SEPIC/Flyback Controller with Dual Random Spread Spectrum* data sheet.
15. Texas Instruments, *UCC5870-Q1 30-A Isolated IGBT/SiC MOSFET Gate Driver with Advanced Protection Features for Automotive Applications* data sheet.