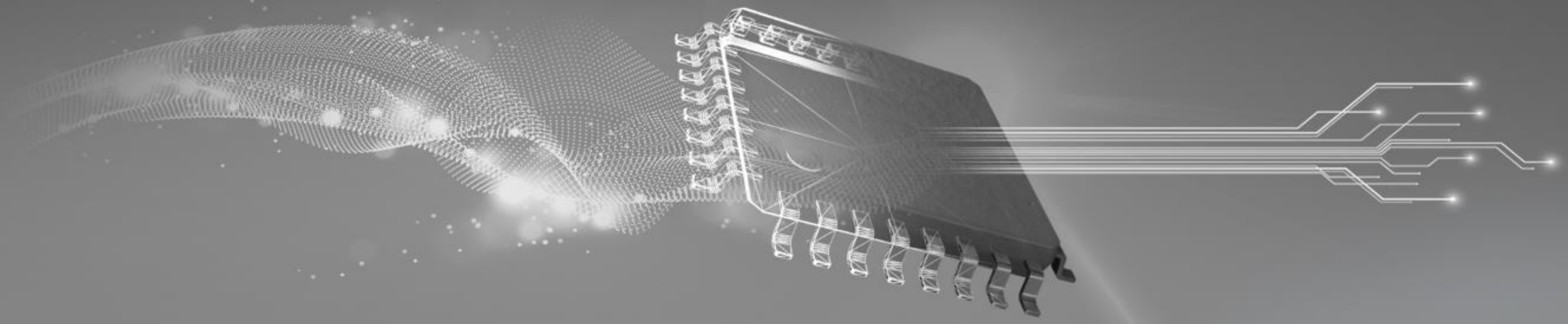
TI TECH DAYS



Jacinto™ 7 SoC and PMIC functional safety

Mahmut Ciftci, Pauline Wang

Agenda

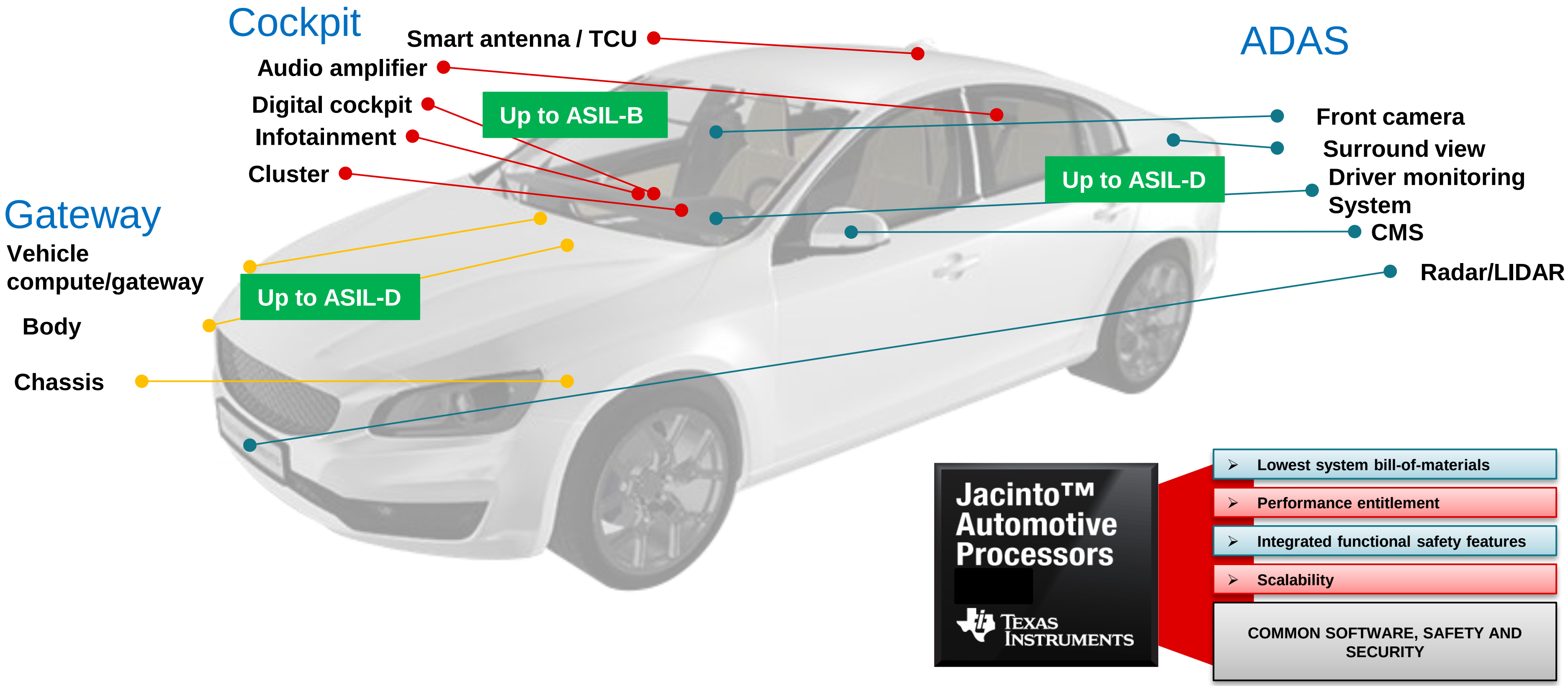
- Jacinto™ 7 platform overview
- Jacinto 7 SoC safety architecture and hardware diagnostics capabilities
- Jacinto 7 SoC safety software
- PMIC safety mechanisms
- Q&A

Jacinto 7 Functional Safety

Mahmut Ciftci

Systems Architect,
Jacinto Processors

Jacinto 7 SoC platform for functional safety applications



Cockpit

Up to ASIL-B

- Smart antenna / TCU
- Audio amplifier
- Digital cockpit
- Infotainment
- Cluster

ADAS

Up to ASIL-D

- Front camera
- Surround view
- Driver monitoring System
- CMS
- Radar/LIDAR

Gateway

Up to ASIL-D

- Vehicle compute/gateway
- Body
- Chassis

Jacinto™ Automotive Processors

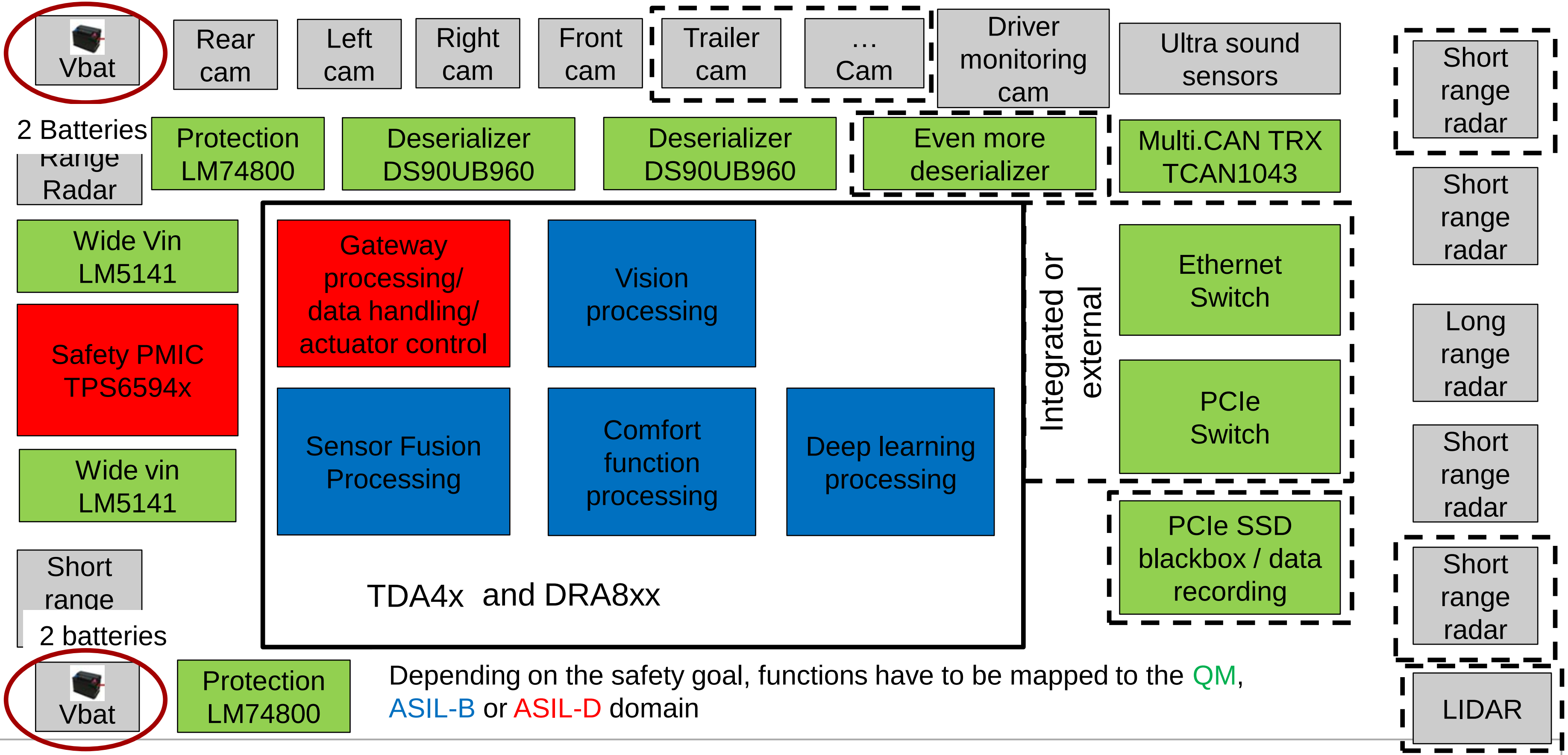
[redacted]

Texas Instruments

- Lowest system bill-of-materials
- Performance entitlement
- Integrated functional safety features
- Scalability

COMMON SOFTWARE, SAFETY AND SECURITY

ADAS system block diagram up to level 3



Vbat

Rear cam

Left cam

Right cam

Front cam

Trailer cam

… Cam

Driver monitoring cam

Ultra sound sensors

Short range radar

2 Batteries

Range Radar

Protection LM74800

Deserializer DS90UB960

Deserializer DS90UB960

Even more deserializer

Multi.CAN TRX TCAN1043

Wide Vin LM5141

Safety PMIC TPS6594x

Wide vin LM5141

Gateway processing/ data handling/ actuator control

Vision processing

Sensor Fusion Processing

Comfort function processing

Deep learning processing

TDA4x and DRA8xx

Integrated or external

Ethernet Switch

PCIe Switch

PCIe SSD blackbox / data recording

Short range radar

Long range radar

Short range radar

Short range radar

LIDAR

Short range

2 batteries

Vbat

Protection LM74800

Depending on the safety goal, functions have to be mapped to the QM, ASIL-B or ASIL-D domain

Jacinto 7 platform: heterogeneous compute

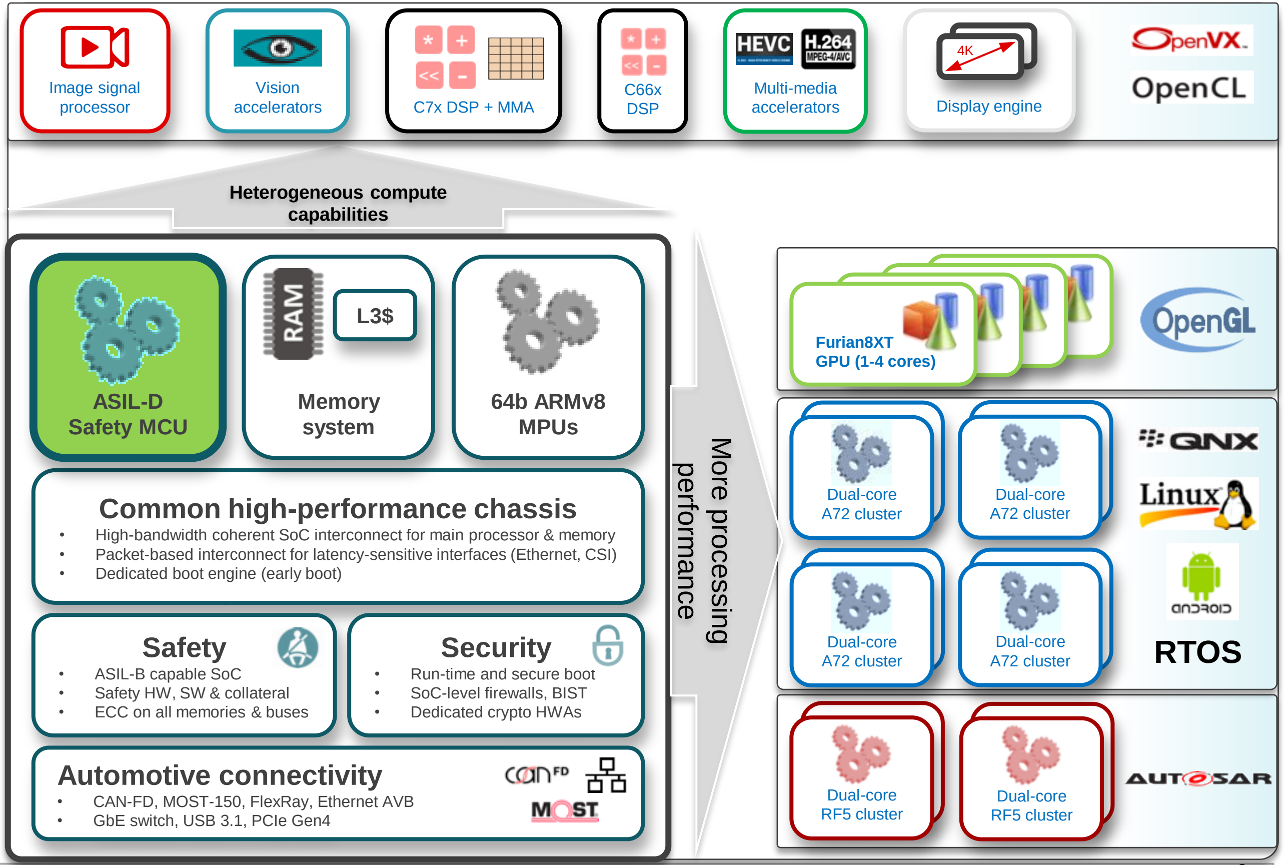
TDA4x / DRA8xx SoCs

Designed for automotive safety and robustness

Choose the right core for the right job

Optimize entire platform around programmer productivity on the MPUs

Offload the majority of "work" to specialized processors. Provide tools & software to manage complexity



Common high-performance chassis

- High-bandwidth coherent SoC interconnect for main processor & memory
- Packet-based interconnect for latency-sensitive interfaces (Ethernet, CSI)
- Dedicated boot engine (early boot)

Safety

- ASIL-B capable SoC
- Safety HW, SW & collateral
- ECC on all memories & buses

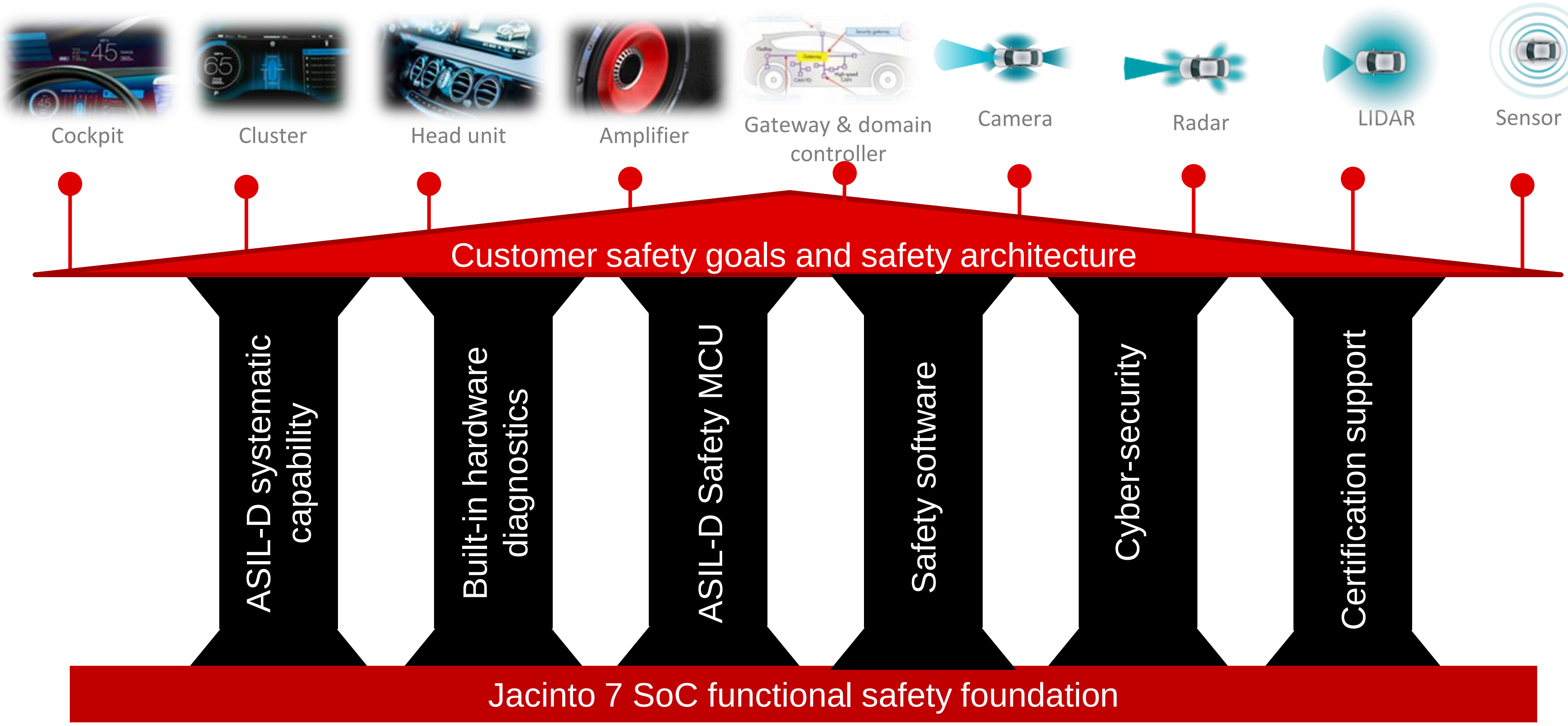
Security

- Run-time and secure boot
- SoC-level firewalls, BIST
- Dedicated crypto HWAs

Automotive connectivity

- CAN-FD, MOST-150, FlexRay, Ethernet AVB
- GbE switch, USB 3.1, PCIe Gen4

Jacinto 7 platform | common safety architecture



Cockpit

Cluster

Head unit

Amplifier

Gateway & domain controller

Camera

Radar

LIDAR

Sensor fusion

Customer safety goals and safety architecture

ASIL-D systematic capability

Built-in hardware diagnostics

ASIL-D Safety MCU

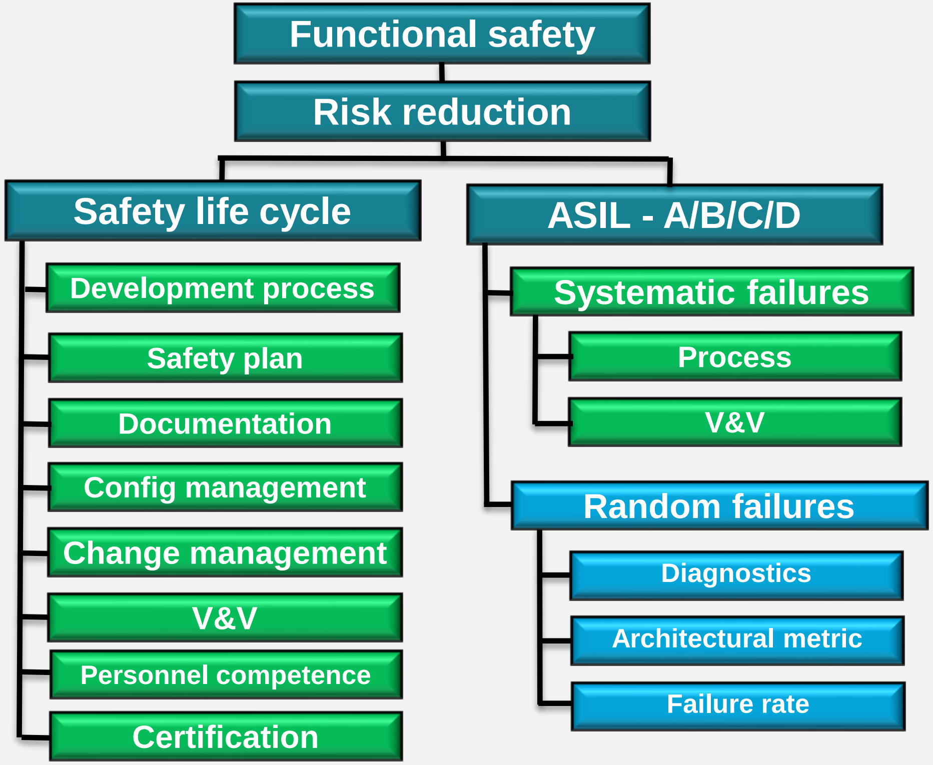
Safety software

Cyber-security

Certification support

Jacinto 7 SoC functional safety foundation

Jacinto 7 functional safety design for ISO-26262 / IEC-61508


Functional safety

Risk reduction

Safety life cycle

- Development process
- Safety plan
- Documentation
- Config management
- Change management
- V&V
- Personnel competence
- Certification

ASIL - A/B/C/D

- Systematic failures
  - Process
  - V&V
- Random failures
  - Diagnostics
  - Architectural metric
  - Failure rate

CSP = Compliance support package

Functional safety design packages help meet functional safety requirements while managing both systematic and random failures.

- TI HW development process is TUV SUD certified
- TI SW development process is TUV SUD certified
- All Jacinto 7 SoCs will be certified

CERTIFICATE

- TI delivers safety manual documentation
- TI delivers safety analysis report (FMEDA)

DRA8xx safety manual

PDF

Jacinto 7 SoC (DRA8xx/TDA4x) functional safety support

Systematic capability

Up to ASIL-D / SIL-3

- Integrated Safety MCU
- Independently certified hardware and software development processes
- Requirements tracking
- Documentation
- Validation

Built-in diagnostics, low FIT

Up to ASIL-D / SIL-3

- Asymmetric multi-processing
- Lockstep CPUs
- Memory SECDED ECC
- Interconnect protection
- MPU/MMU/firewalls
- Voltage/clock/reset monitors
- Voltage temperature monitors
- Logic/memory BIST
- Built-in tests for diagnostics

…and more.

Certification support

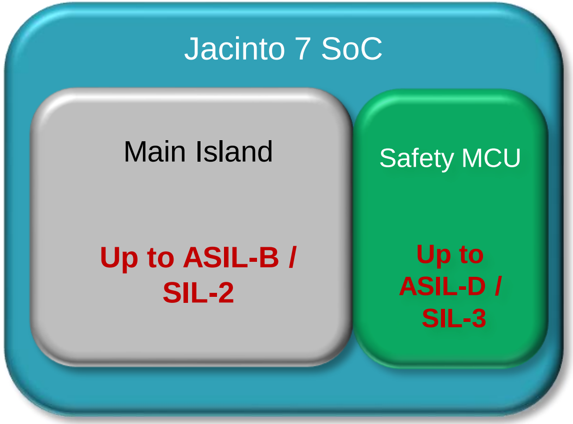
Functional Safety Design Package

- Safety manual
- Safety analysis report
- Configurable FMEDA
- Software compliance support Packages (CSPs)
- 3rd party safety element out of context (SEooC) assessment

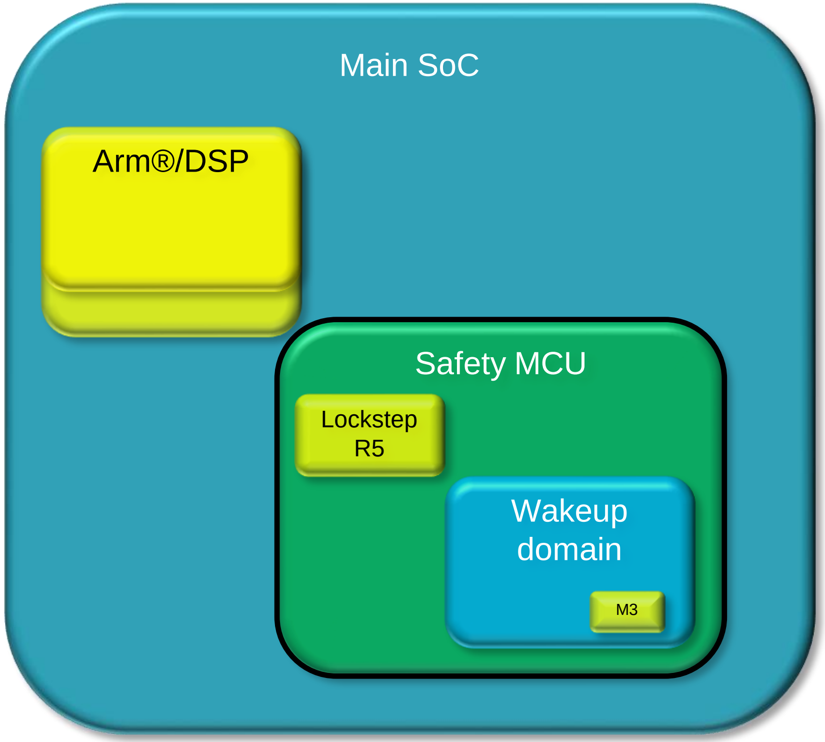
Note: These are platform capabilities. See ‘functional safety’ design package for individual device capabilities.

Jacinto 7 SoC safety architecture highlights

- **Targeted for mixed criticality**
  - Safety MCU up to ASIL-D / SIL-3
  - Main SoC minimum ASIL-B / SIL-2 with many functions up to ASIL-D depending on device
  - Some Jacinto 7 SoCs target ASIL-D / SIL-3 through the DDR
  - Main SoC may crash while MCU stays alive and on the CAN bus
    - MCU system is boot, safety, security, power management master and needs to be ON
  - Whitelist firewalls on all slaves to support FFI
- **Each SoC has 1 or more lockstep R5F cores**
- **Each SoC has 1 or more MPUs (A53, A72, C7x)**
  - Intentionally arranged in no more than dual clusters with separate voltage and clocks for FFI
  - Interconnect, coherence and inter-processor communication is natively ASIL-B / SIL-2 or up enabling reciprocal comparison by software, software lockstep, program flow monitoring and other system level safety mechanisms for high powered compute

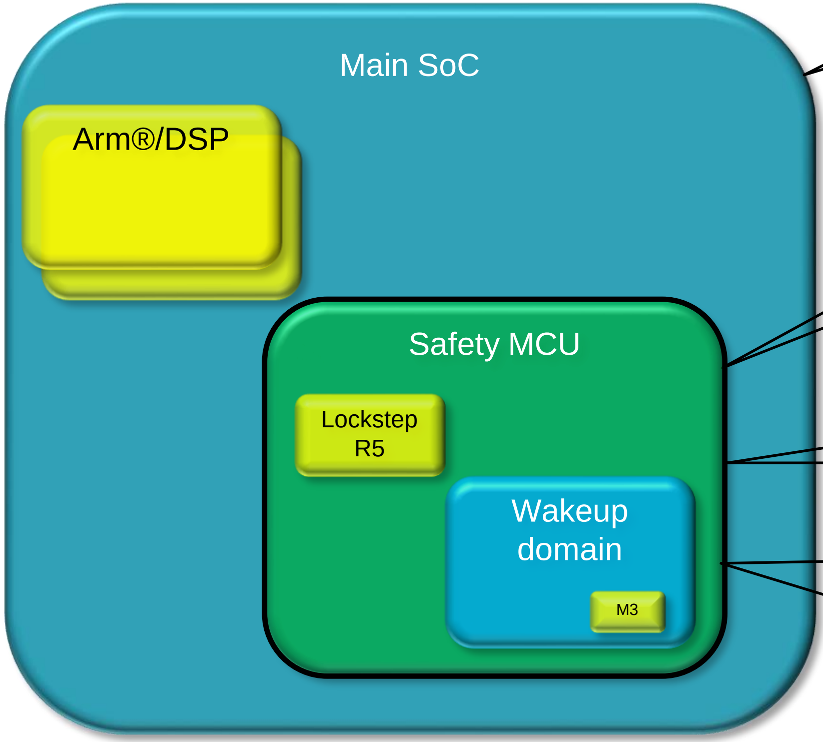


Jacinto 7 SoC safety architecture concept



- "Safety MCU" concept
  - Region of component is heavily protected by hardware diagnostic measures
    - Power
    - Clock
    - Reset
    - CPUs
    - Memories
    - Interconnect
  - Once the correct operation of a Safety MCU is established, logic in this region can be used to provide diagnostic coverage on other regions
  - This partition provides a basis for effective functional safety metrics while providing benefits to minimize overall system BOM overhead cost
- MCU integration concept
  - Separate voltage supplies
  - Separate clocks and resets
  - Chip inside a chip
  - Main SoC can crash and MCU remains alive, can reboot main SoC

Safety isolation architecture



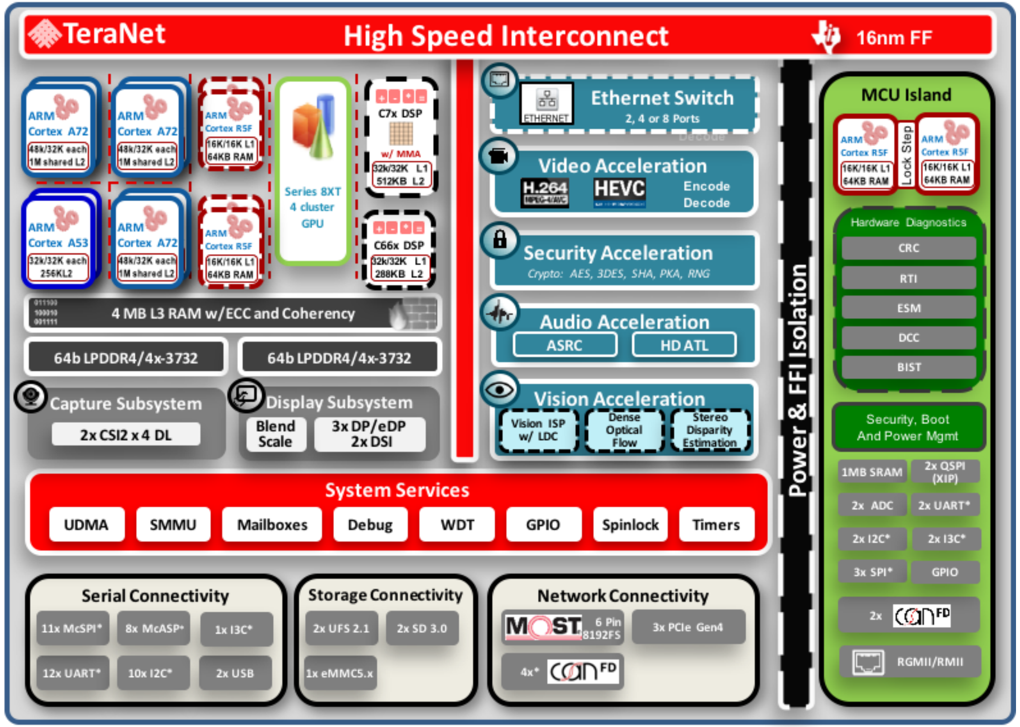
High-power processing
- High power processing (Cortex® A/DSP)
- Graphics
- High speed communication (USB/PCIe/etc..)
- Industrial communication

Safe processing and monitoring
- Lockstep R5
- Flash
- Serial communications
- ADCs

Secure device services
- Power control
- Reset control
- Isolation control
- Authentication requests

Freedom from interference
- Separate voltage
- Separate clocks
- Firewalls
- Internal SPI communication

Safety mechanisms



- Hardware lockstep R5F

- CPU coverage
  - Reciprocal comparison by software
  - Program flow monitoring
  - Asymmetric multi-processing

- Interconnect,
  - Redundant req/ready
  - Parity on control and attributes
  - SECDED ECC on data
  - Parity protection of critical Flops/MMRs

- Memory ECC

- Memory self test (PBIST)
- Logic self test (LBIST)
- SW BIST across IP
- IO loopback on interfaces

- Safety diagnostics
  - Voltage and temperature monitors
  - Power good detectors
  - Dual clock comparators
  - Watchdog timers
  - Error signaling modules

- Communication, sensors, flash interfaces
  - Freeze/hang detection
  - Protocol
  - Built-in diagnostics
  - Redundancy
  - End-to-end Safing
  - Data hash, CRC, authentication

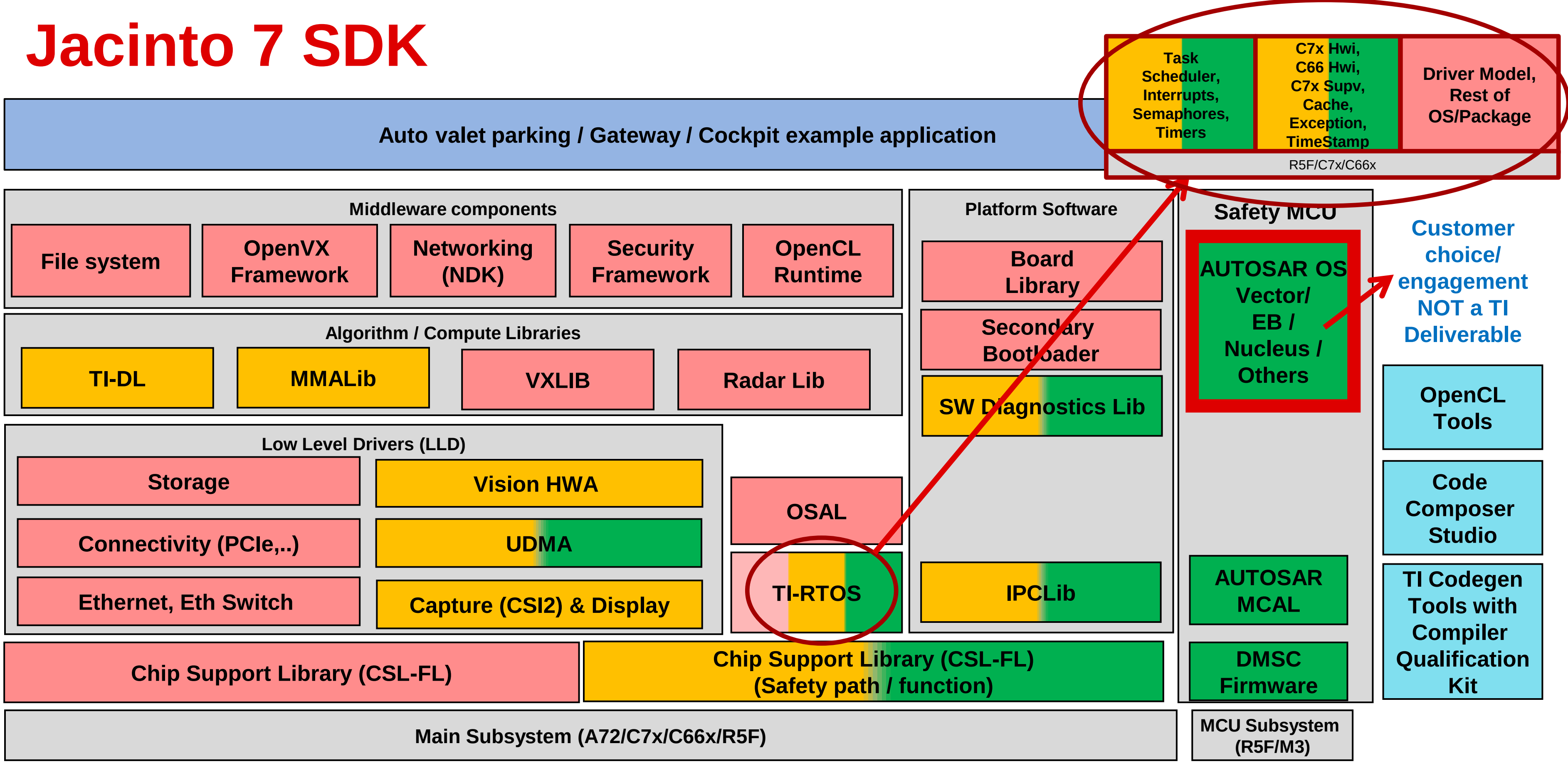
- Device configuration and control
  - Redundant programming
  - MMR monitoring

Jacinto 7 SoC functional safety deliverables

- TI deliverables
  - Functional safety manual
  - Safety analysis report
    - Including customizable FMEDA
  - Software
    - Certification support packages
    - Diagnostic library
  - External assessment as safety element out of context (including certificate)
    - This is not end-product system-level certification which is system integrator’s responsibility

Jacinto 7 SoC Functional Safety Software

Jacinto 7 SDK



Task Scheduler, Interrupts, Semaphores, Timers

C7x Hwi, C66 Hwi, C7x Supv, Cache, Exception, TimeStamp

Driver Model, Rest of OS/Package

R5F/C7x/C66x

Auto valet parking / Gateway / Cockpit example application

Middleware components

File system

OpenVX Framework

Networking (NDK)

Security Framework

OpenCL Runtime

Algorithm / Compute Libraries

TI-DL

MMALib

VXLIB

Radar Lib

Low Level Drivers (LLD)

Storage

Vision HWA

Connectivity (PCIe,..)

UDMA

Ethernet, Eth Switch

Capture (CSI2) & Display

OSAL

TI-RTOS

Platform Software

Board Library

Secondary Bootloader

SW Diagnostics Lib

IPCLib

Safety MCU

AUTOSAR OS Vector/ EB / Nucleus / Others

AUTOSAR MCAL

DMSC Firmware

Customer choice/ engagement NOT a TI Deliverable

OpenCL Tools

Code Composer Studio

TI Codegen Tools with Compiler Qualification Kit

Chip Support Library (CSL-FL)

Chip Support Library (CSL-FL) (Safety path / function)

Main Subsystem (A72/C7x/C66x/R5F)

MCU Subsystem (R5F/M3)

Legend

Demo

TI Baseline

ASIL-C/D Safety Compliant

ASIL-B Safety Compliant

Tools

Functional safety software components

Diagnostics

Software Diagnostic Library (SDL)

LBIST / PBIST

- Power on self test on MCU R5F, M3
- SW controlled on R5F, A72, C7x
- SW controlled PBIST of MSMC RAM

Loopback: CAN, SPI, ...

- Functionality check: CRC, ECC, ...
- Monitors: RTI, DCC, ESM, Frame freeze detect, …
- Error Injection

Software Test Library(STL)

- C66x, MMA, C7x: **TBD**
- A72, R5F: **ARM STL release**

Functional Software

ASIL-C/D

- AUTOSAR MCAL on Safety Island (CAN, DIO, SPI, ETH, IPC, ADC, PWM, WDG, GPT)
- CSL-FLs for Safety IPs (ECC, CRC, DCC, ESM, BIST, VTM, PGD, POK, ADC)
- SCI Client, UDMA, Resource Manager
- DMSC Firmware
- TI-RTOS

ASIL-B

- CSL-FLs for all IPs in safety path
- MMA, TIDL Library
- LLDs for CSI2, DSS, VHWA, IPC
- Compiler Qual Kit

Reference Software

- Reference SW for Safety IP usage
- Reference SW for safety manual items allocated to SW
- Example code for FFI, Main / MCU island isolation and other safety features

Software certification support package

Compliance Support Package (CSP):

- Software safety manual
- TI internal audit report
- Requirements, test plan and reports
- Traceability data
- Dynamic code coverage analysis
- Static code analysis/MISRA-C
- Safety diagnostics library and manual
- Compiler qualification kit
- Software FMEA report

Jacinto 7 PMIC functional safety

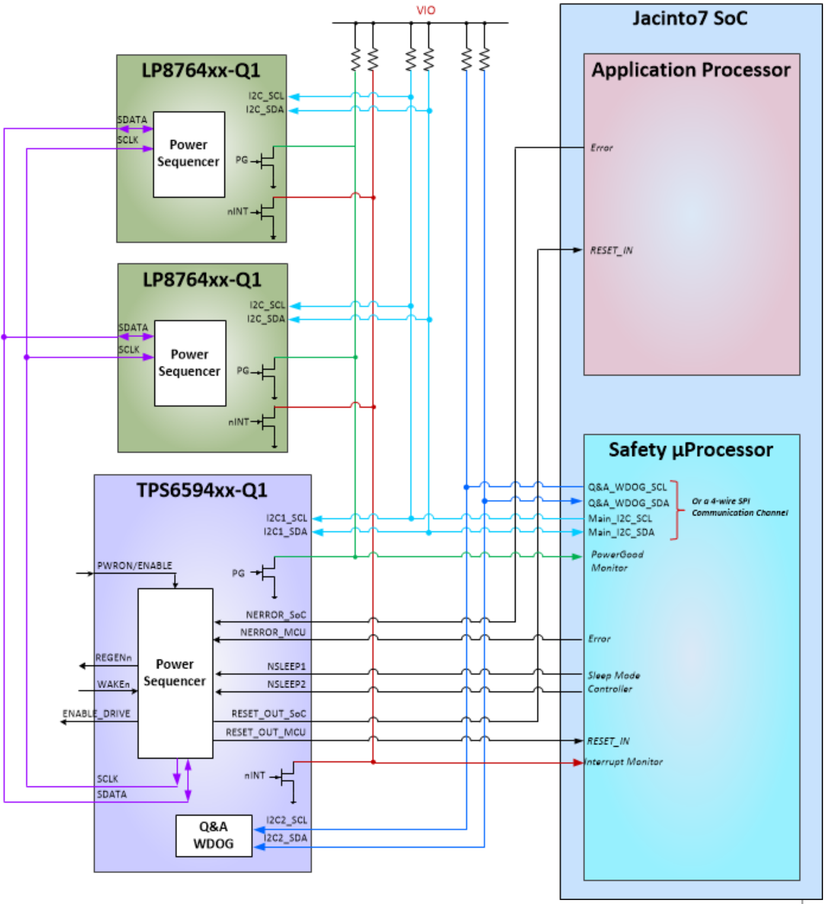
Pauline Wang

TPS6594x-Q1 and LP8764x-Q1 Multi-PMIC Connection – Our Solution

- The multi-PMIC connection module in TPS6594x provides a method to synchronize multiple integrated PMICs and make them look like a ***virtual single PMIC*** to each variant of the **Jacinto 7 platform.**

  This is done by ***sharing power state information between the devices*.**

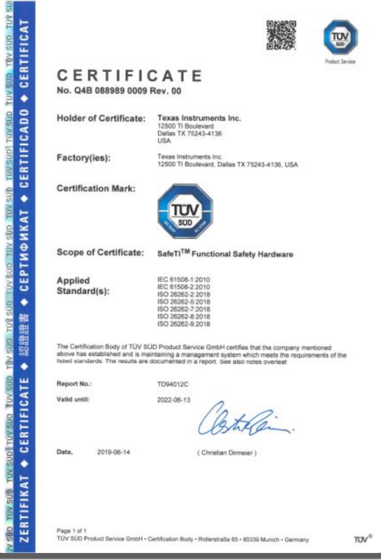
- The advantages of this control scheme:
  - Enables a **scalable power solution** that can be optimized for high/mid/low end variants of the **Jacinto 7 platform**
  - **Preserves system interface towards Jacinto 7 SoC same as with a single PMIC. So no additional software overhead needed on Jacinto 7 SoC when multiple PMICs are used**
  - **Partitioning of the power management functions into any desired number of smaller PMICs, transparent to the Jacinto 7 SoC**
  - Enables fully synchronous operation of all PMICs without the need for external sequencer or glue logic. **So no software overhead needed on Jacinto 7 SoC**
  - Supports diagnostics and **functional safety monitoring of the Jacinto 7 SoC** inside the fault-tolerant time of the system



TPS6594-Q1 and LP8764-Q1 Functional Safety Capability

Systematic

- Developed according SafeTI™ Development Process with TÜV SÜD certification for ISO26262 ASIL-D target



ZERTIFIKAT ◆ CERTIFICATE ◆ 認證證書 ◆ СЕРТИФИКАТ ◆ CERTIFICADO ◆ CERTIFICAT

Product Service

CERTIFICATE

No. Q4B 088989 0009 Rev. 00

Holder of Certificate:	**Texas Instruments Inc.** 12500 TI Boulevard Dallas TX 75243-4136 USA
Factory(ies):	Texas Instruments Inc. 12500 TI Boulevard, Dallas TX 75243-4136, USA
Certification Mark:	TÜV SÜD
Scope of Certificate:	SafeTI^{TM} Functional Safety Hardware
Applied Standard(s):	IEC 61508-1:2010 IEC 61508-2:2010 ISO 26262-2:2018 ISO 26262-5:2018 ISO 26262-7:2018 ISO 26262-8:2018 ISO 26262-9:2018

The Certification Body of TÜV SÜD Product Service GmbH certifies that the company mentioned above has established and is maintaining a management system which meets the requirements of the listed standards. The results are documented in a report. See also notes overleaf.

Report No.:	TD94012C
Valid until:	2022-06-13

Date, 2019-06-14

(Christian Dirmeier)

Page 1 of 1

TÜV SÜD Product Service GmbH • Certification Body • Ridlerstraße 65 • 80339 Munich • Germany

TÜV®

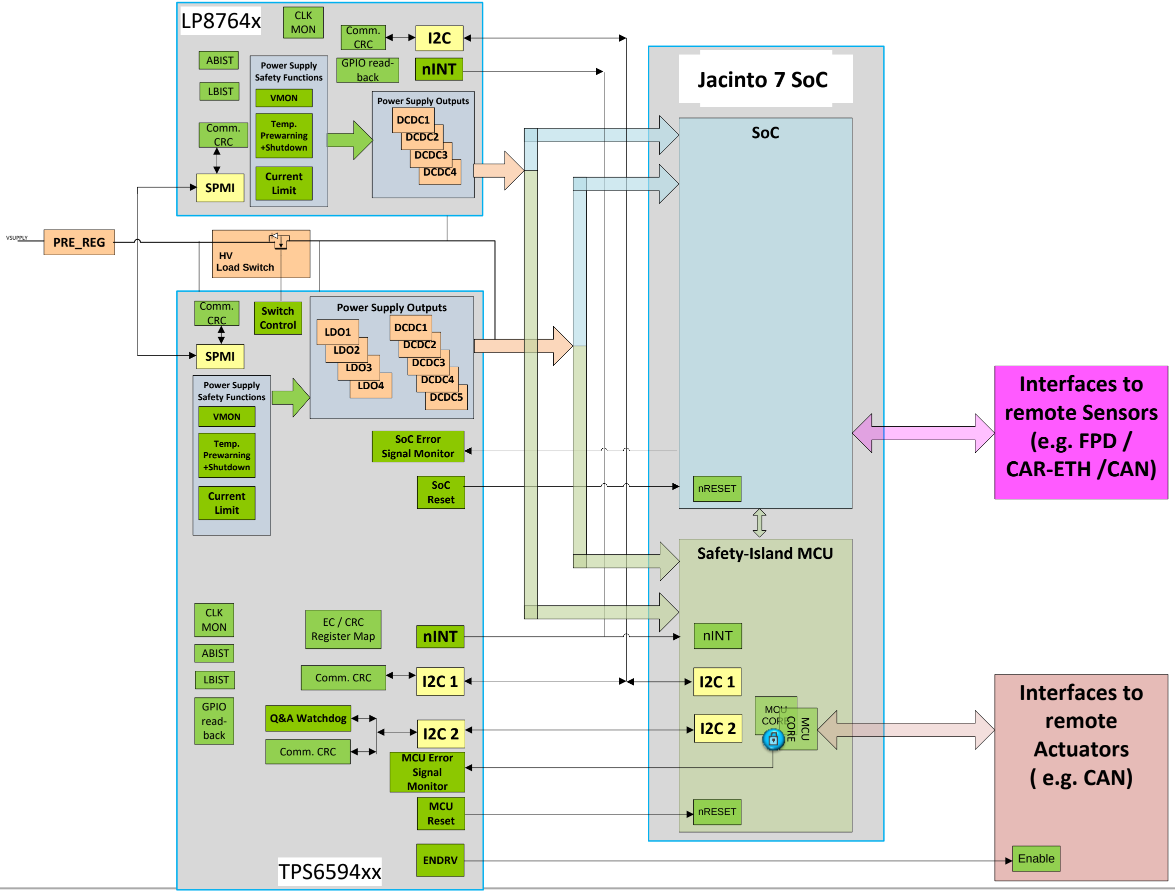
Hardware Metrics

- **> 99% Single-Point Metric** and **>90% Latent-Fault Metrics**
- Accurate and fast Output Voltage Monitoring
- Accurate and fast Input Voltage Monitoring
- Fast Over-Voltage Protection
- Q&A Watchdog
- Error Signal Monitors
- CRC on Communication Interfaces and SPMI bus
- CRC on Configuration Registers
- CRC on internal memory
- Built-In Self-Tests on Voltage Monitors, State Machine, SPMI Bus, Watchdog and Error Signal Monitors

Supporting tools and documents

- FMEDA
- Safety Manual
- Functional Safety Analysis Report:
  - DFMEA
  - pin-FMEA
  - FTA & DFA
- Technical Reference Manual(s) for powering **Jacinto 7 SoC** with TPS6594x / LP8764x PMICs
- **SDK for Jacinto 7 SoCs**

Safety Concept for supplying Processor

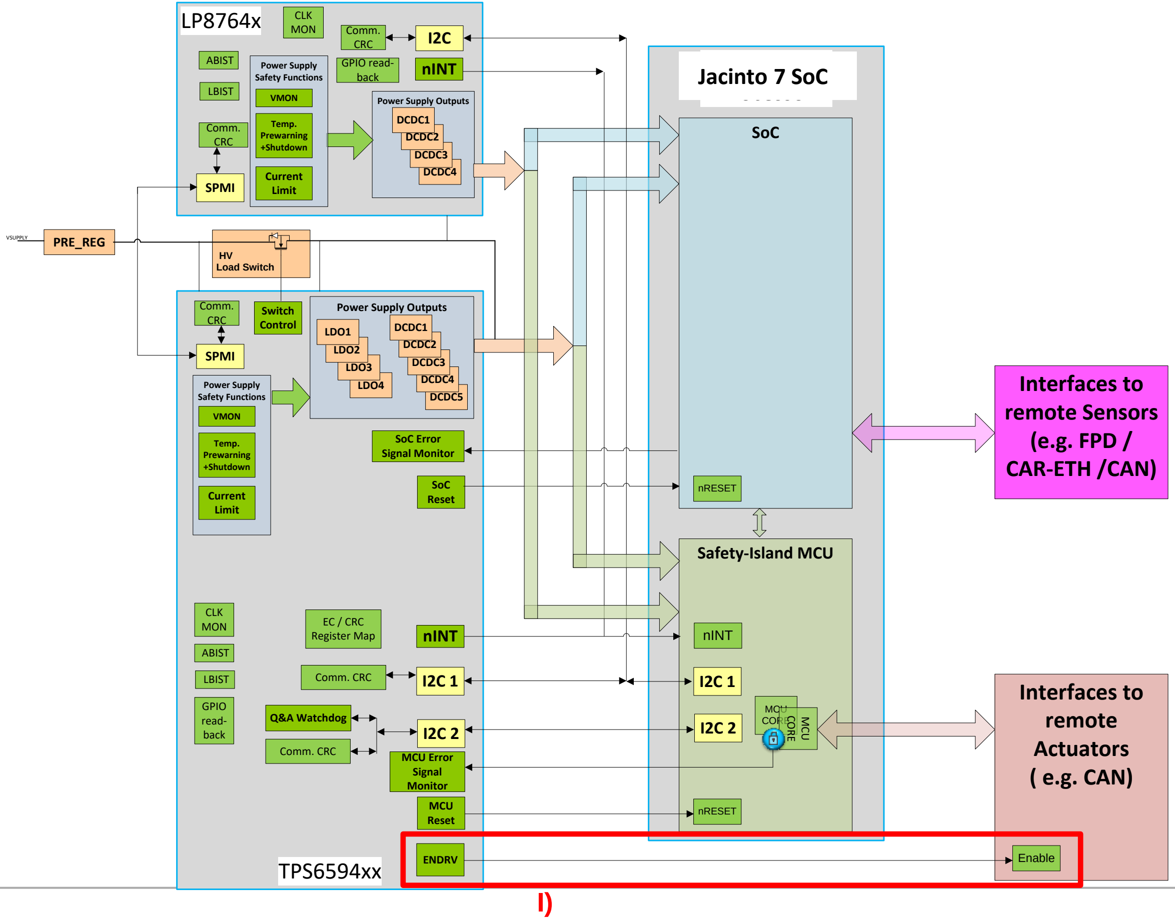


Fail-Silent Safety Concept

As long as SoC and Safety MCU in **Jacinto 7 SoC** work properly:

- SoC checks sensor data
- Safety MCU:
  - Checks the SoC operation
  - Controls the actuators
  - Checks whether the actuators react on the control in the expected way

Safety Concept for supplying Processor



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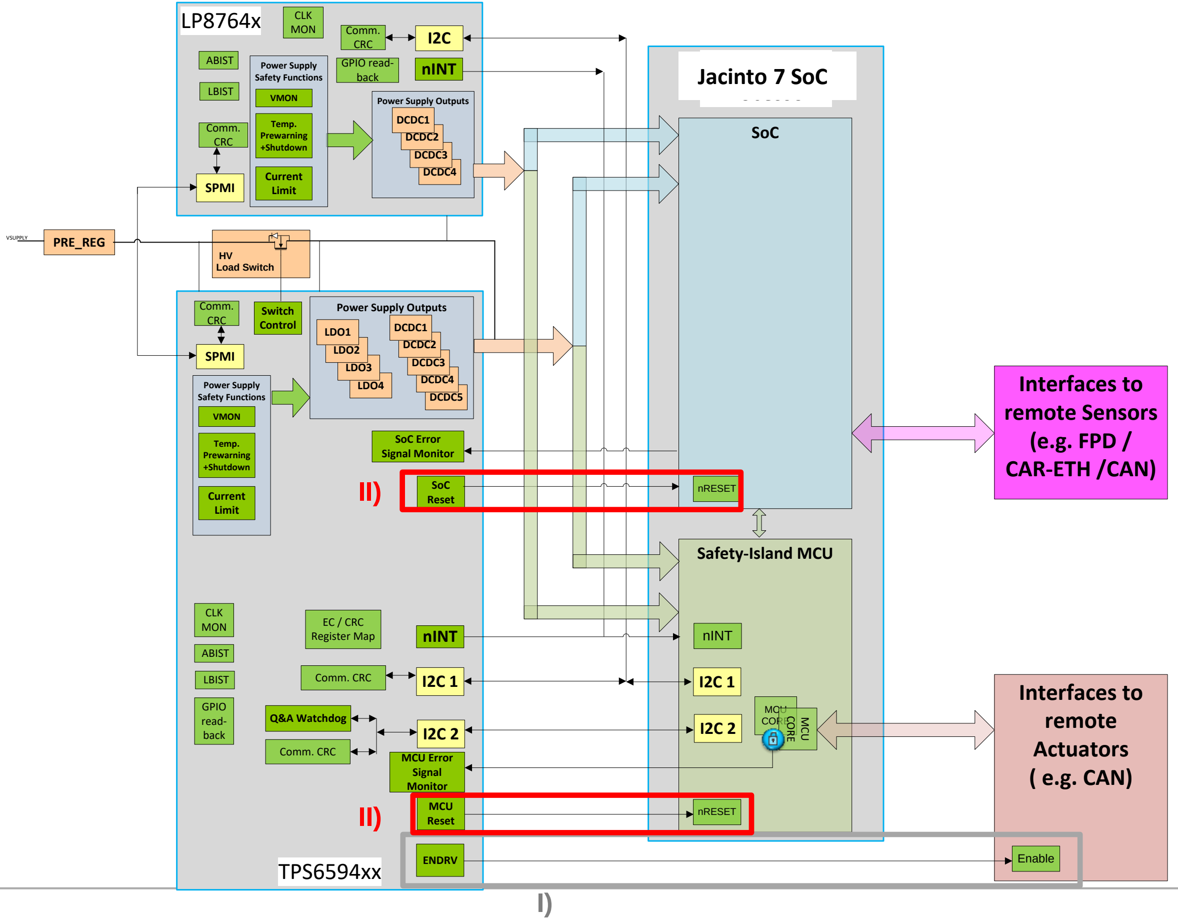
For failures which would cause improper operation of the Safety MCU or SoC:

I. PMIC puts system in safe state through EN_DRV pin

Safety Concept for supplying Processor



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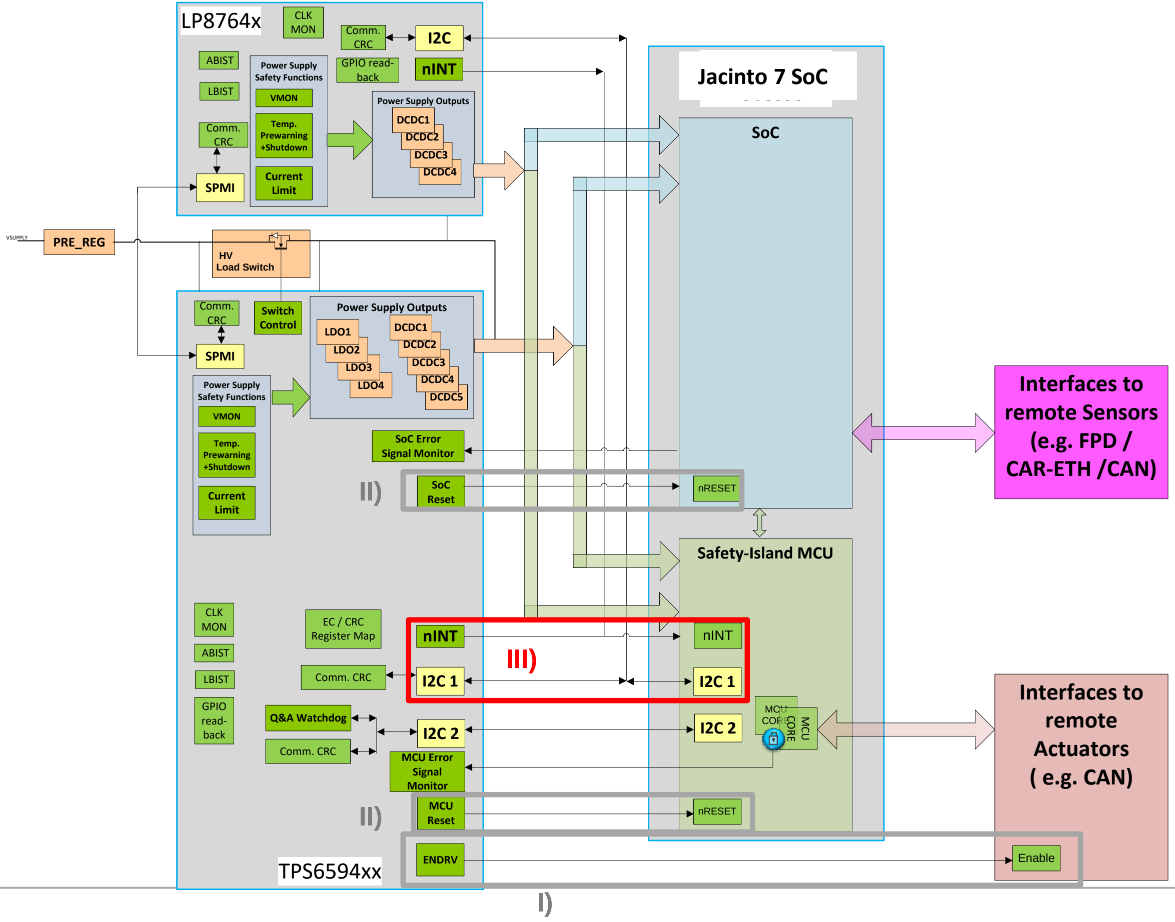
For failures which would cause improper operation of the Safety MCU or SoC:

I. PMIC puts system in safe state through EN_DRV pin

II. PMIC resets SoC and/or Safety MCU if necessary

Safety Concept for supplying Processor



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  - Controls the actuators
  - Checks whether the actuators react on the control in the expected way

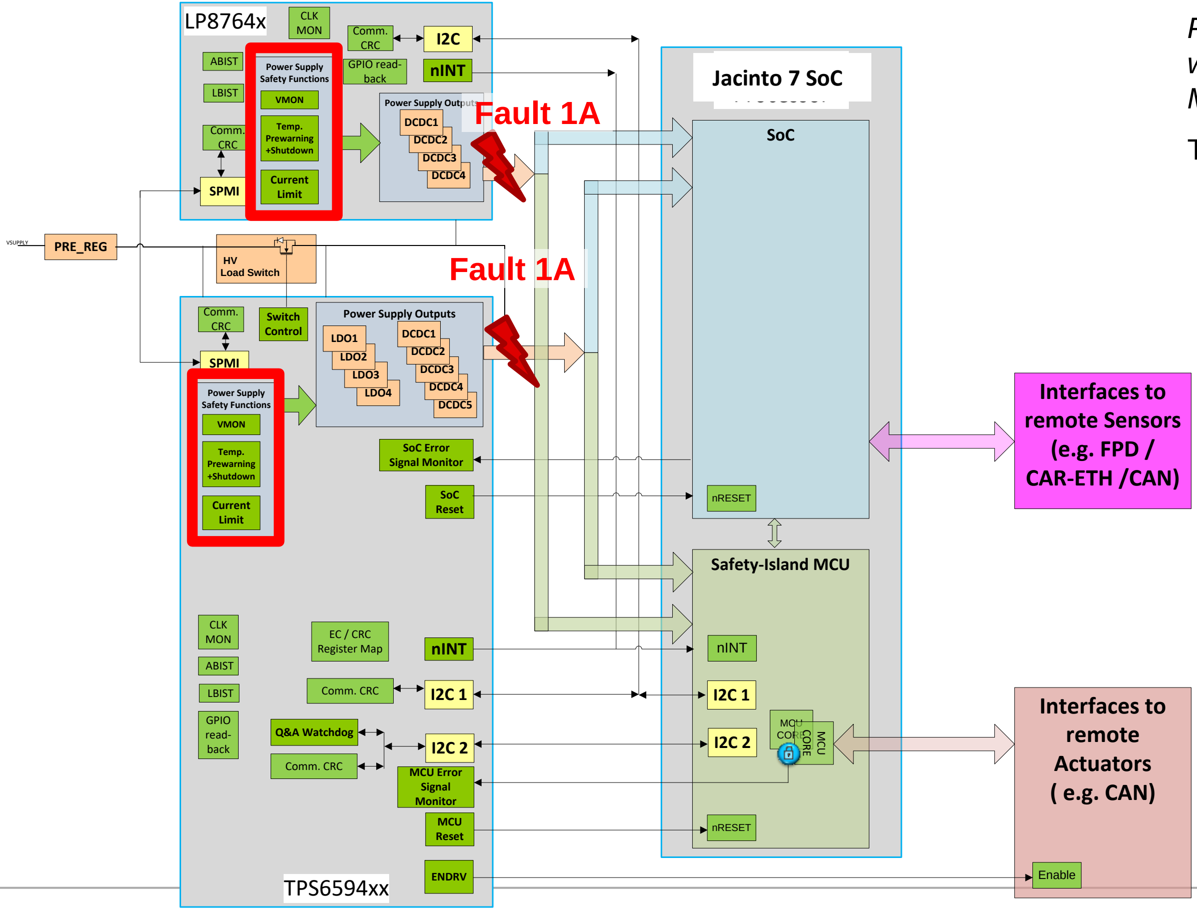
For failures which would cause improper operation of the Safety MCU or SoC:

I. PMIC puts system in safe state through EN_DRV pin

II. PMIC resets SoC and/or Safety MCU if necessary

III. PMIC reports all previously occurred errors during a drive-cycle to **Jacinto 7 SoC**

Safety Concept for supplying MCU + SoC domains in Jacinto 7 SoC



PMIC puts system in assumed safe state for failures which would cause improper operation of the Safety MCU or SoC.

These failures include:

1. **A) Failures in supply voltages to Safety MCU or SoC**

1. B) Failure in input supply voltage to PMIC

2. A) SoC hardware error

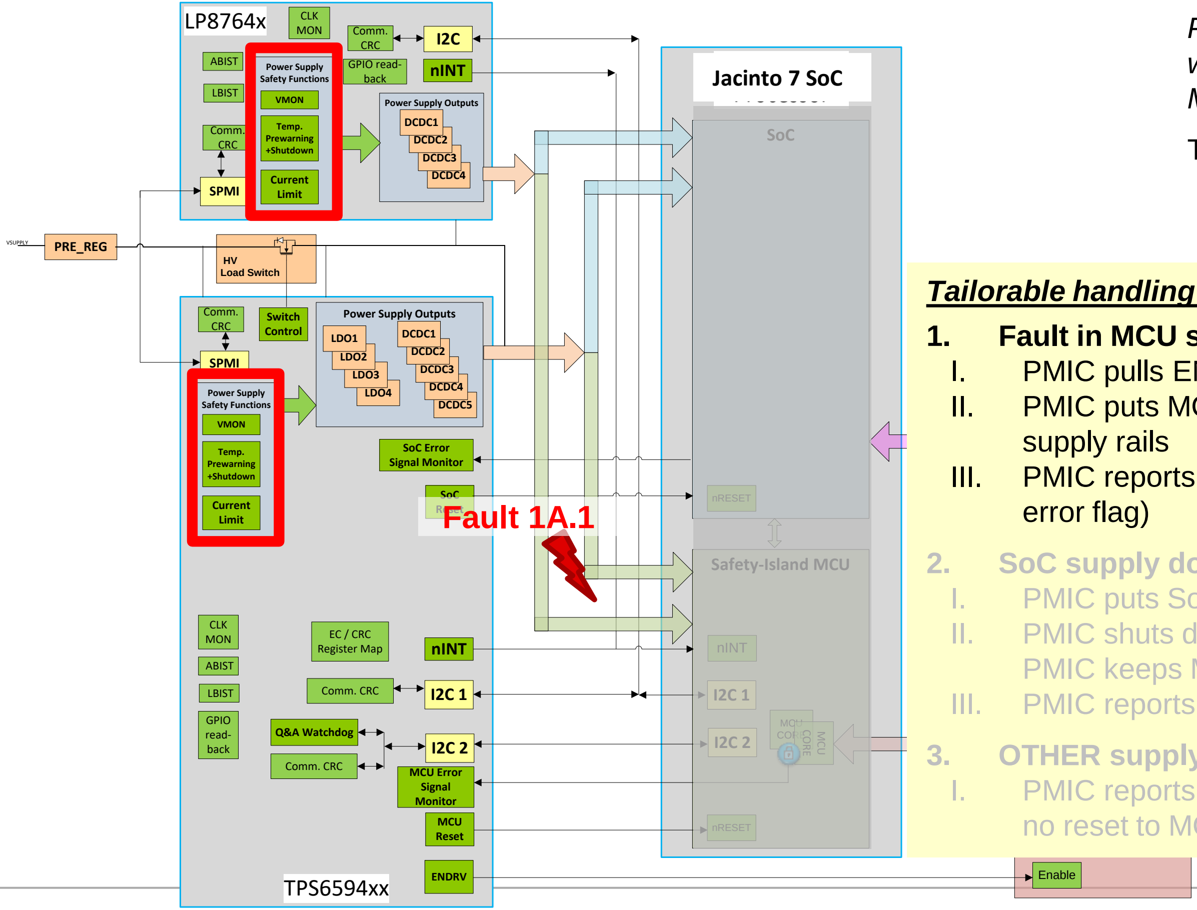
2. B) Safety Island MCU hardware error

3. Safety Island MCU software error

Safety functions for detecting fault 1A in TPS6594-Q1 & LP8764-Q1:

- **Output voltage monitoring (VMON) with independent bandgap reference**
- **Junction temperature monitoring (Tj MON)**
- **Current limit**

Safety Concept for supplying MCU + SoC domains in Jacinto 7 SoC



PMIC puts system in assumed safe state for failures which would cause improper operation of the Safety MCU or SoC.

These failures include:

1. **A) Failures in supply voltages to Safety MCU or SoC**

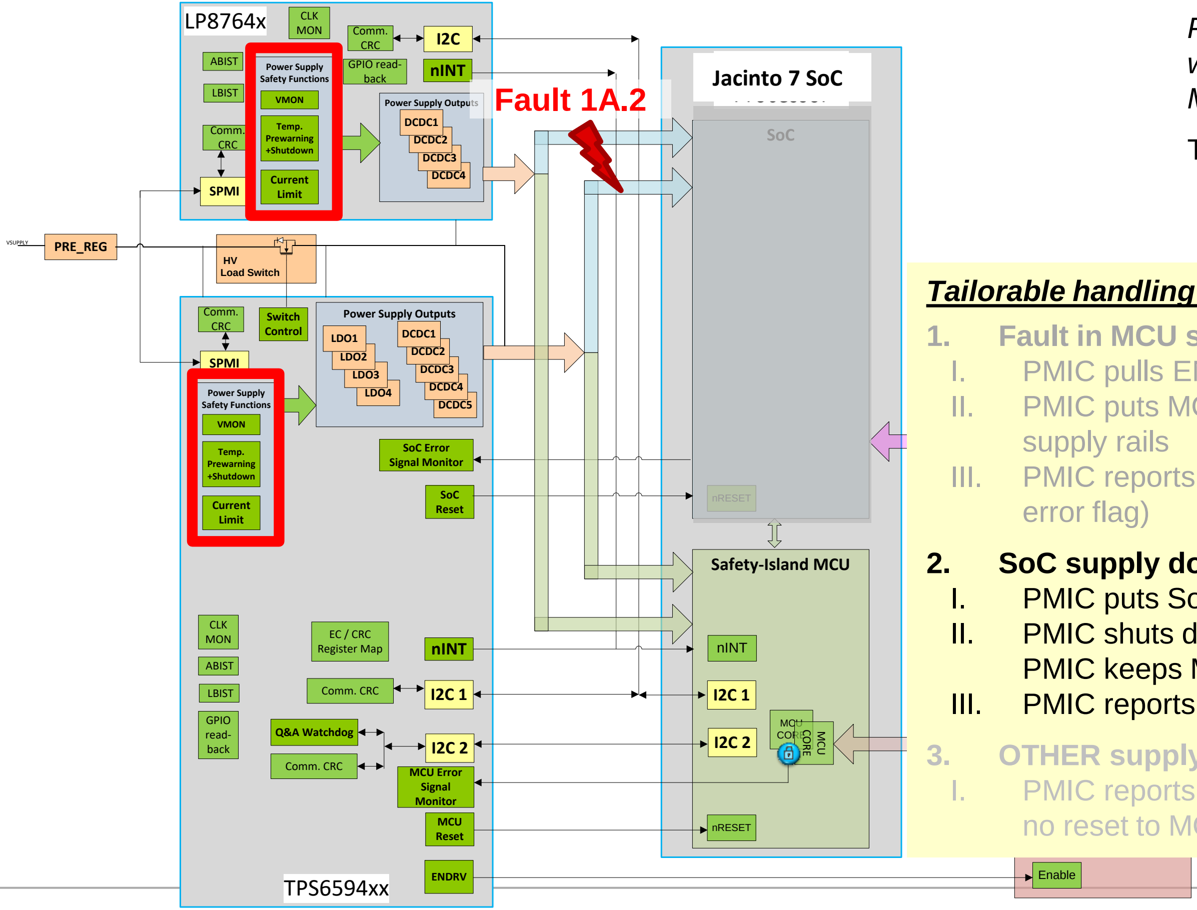
Tailorable handling of output voltage faults:

1. **Fault in MCU supply domain:**
   I. PMIC pulls ENDRV low
   II. PMIC puts MCU and SoC in reset and shuts down all power-supply rails
   III. PMIC reports the error to the MCU on re-start (nINT pin low + error flag)

2. **SoC supply domain**:
   I. PMIC puts SoC in reset. MCU not put in reset
   II. PMIC shuts down the power-supply rails mapped to the SoC. PMIC keeps MCU supply rails on. ENDRV can stay high
   III. PMIC reports the error to the MCU (nINT pin low + error flag)

3. **OTHER supply domain**:
   I. PMIC reports the error to the MCU. PMIC keeps all rails on, and no reset to MCU and SoC (nINT pin low + error flag)

Safety Concept for supplying MCU + SoC domains in Jacinto 7 SoC



PMIC puts system in assumed safe state for failures which would cause improper operation of the Safety MCU or SoC.

These failures include:

1. **A) Failures in supply voltages to Safety MCU or SoC**

Tailorable handling of output voltage faults:

1. Fault in MCU supply domain:

- I. PMIC pulls ENDRV low
- II. PMIC puts MCU and SoC in reset and shuts down all power-supply rails
- III. PMIC reports the error to the MCU on re-start (nINT pin low + error flag)

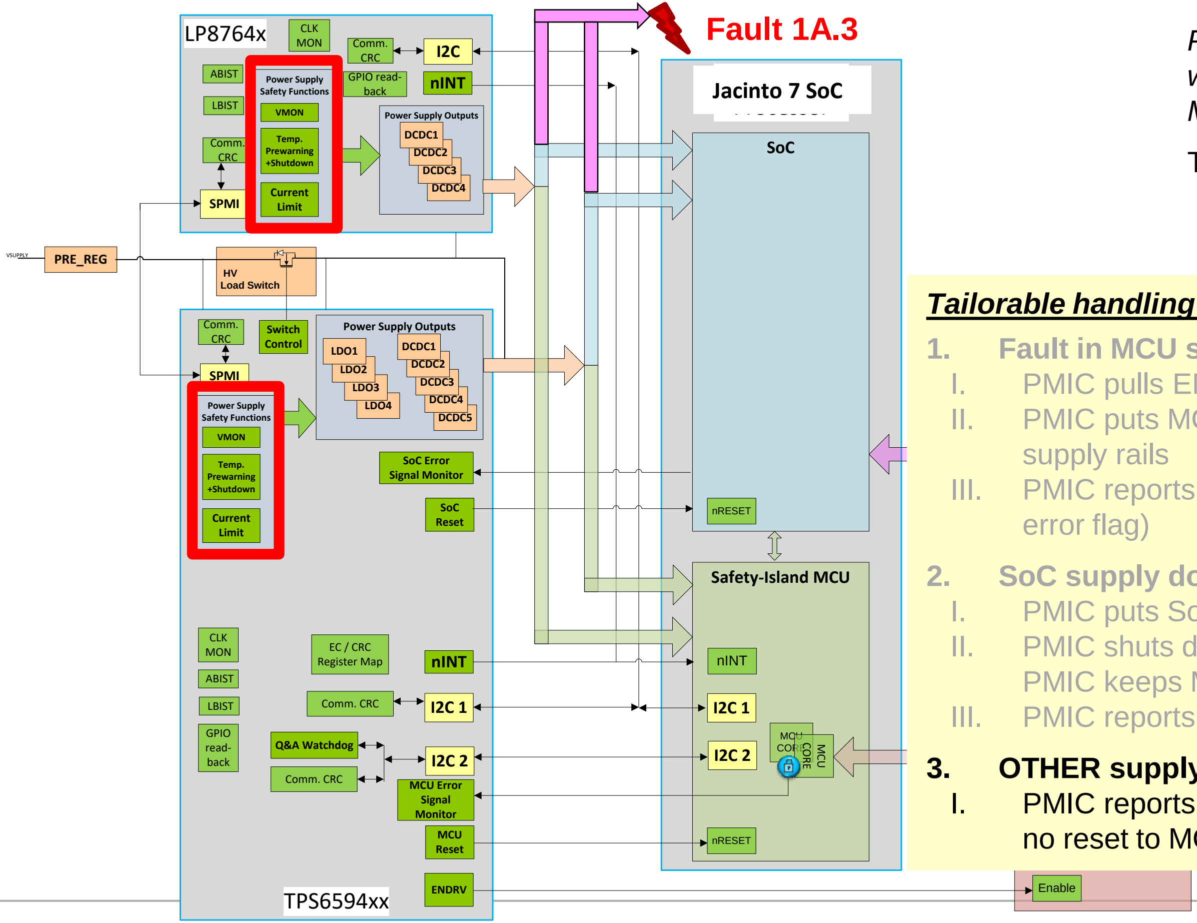
2. SoC supply domain:

- I. PMIC puts SoC in reset. MCU not put in reset
- II. PMIC shuts down the power-supply rails mapped to the SoC. PMIC keeps MCU supply rails on. ENDRV can stay high
- III. PMIC reports the error to the MCU (nINT pin low + error flag)

3. OTHER supply domain:

- I. PMIC reports the error to the MCU. PMIC keeps all rails on, and no reset to MCU and SoC (nINT pin low + error flag)

Safety Concept for supplying MCU + SoC domains in Jacinto^{TM} 7



PMIC puts system in assumed safe state for failures which would cause improper operation of the Safety MCU or SoC.

These failures include:

1. **A) Failures in supply voltages to Safety MCU or SoC**

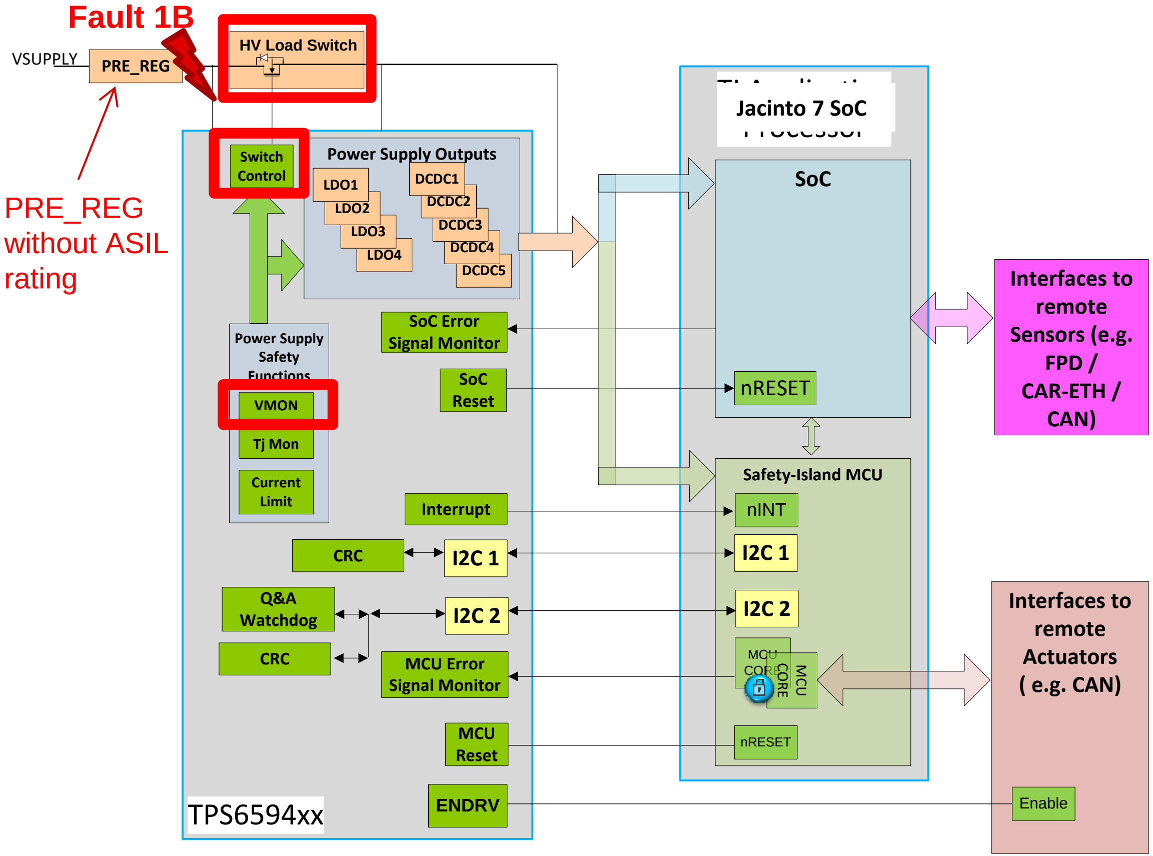
Tailorable handling of output voltage faults:

1. **Fault in MCU supply domain:**
   I. PMIC pulls ENDRV low
   II. PMIC puts MCU and SoC in reset and shuts down all power-supply rails
   III. PMIC reports the error to the MCU on re-start (nINT pin low + error flag)

2. **SoC supply domain**:
   I. PMIC puts SoC in reset. MCU not put in reset
   II. PMIC shuts down the power-supply rails mapped to the SoC. PMIC keeps MCU supply rails on. ENDRV can stay high
   III. PMIC reports the error to the MCU (nINT pin low + error flag)

3. **OTHER supply domain**:
   I. PMIC reports the error to the MCU. PMIC keeps all rails on, and no reset to MCU and SoC (nINT pin low + error flag)

TPS6594x-Q1/LP8764x-Q1 Safety Concept



PMIC puts system in assumed safe state for failures which would cause improper operation of the Safety MCU or SoC.

These failures include:

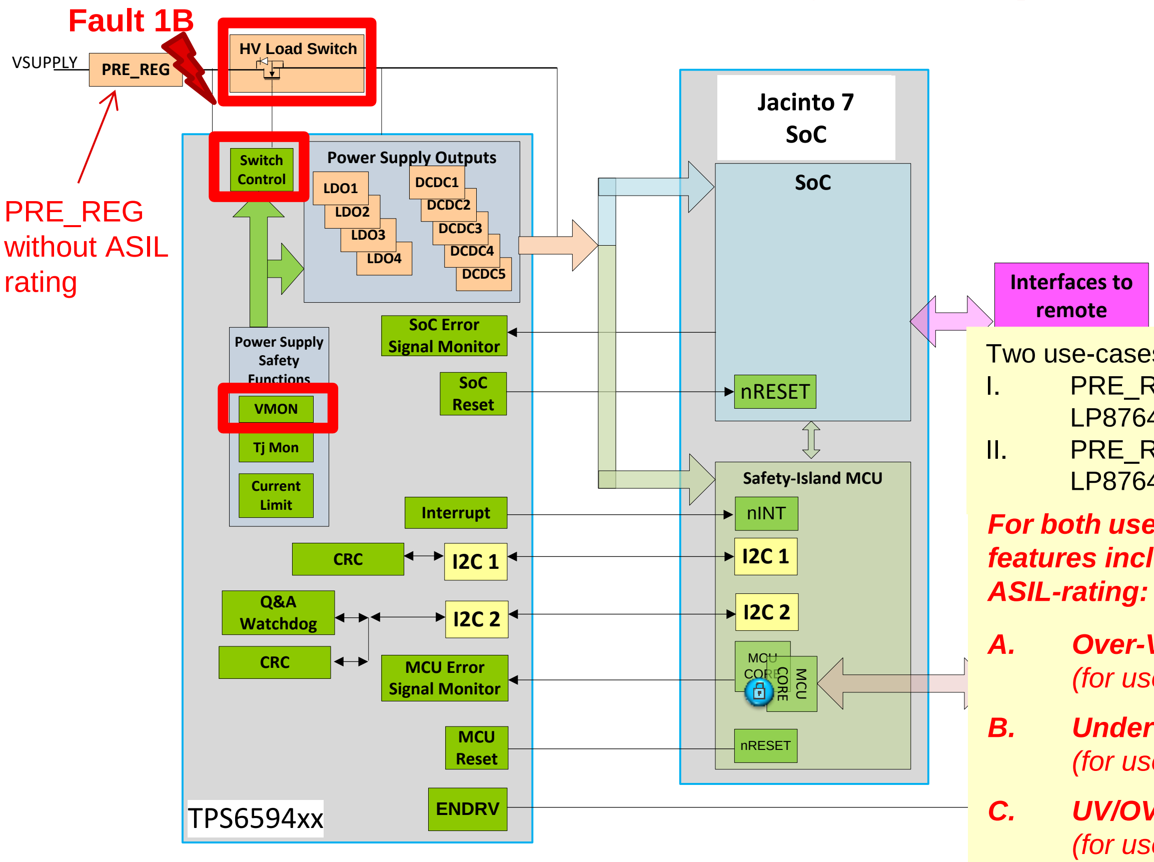
1. A) Failures in supply voltages to Safety MCU or SoC
1. **B) Failure in input supply voltage to PMIC**
2. A) SoC hardware error
2. B) Safety MCU hardware error
3. Safety MCU software error

Safety functions for detecting fault 1B:

- **Input voltage monitoring (VMON) =>** independent /isolated function inside PMIC
- **Switch control**
- **External FET (HV load switch)**

Note: LP8764 does not have the switch control. Use supply line behind external FET to supply the LP8764

TPS6594x-Q1/LP8764x-Q1 Safety Concept



Fault 1B

PRE_REG without ASIL rating

PMIC puts system in assumed safe state for failures which would cause improper operation of the Safety MCU or SoC.

These failures include:

1. A) Failures in supply voltages to Safety MCU or SoC

1. **B) Failure in input supply voltage to PMIC**

Two use-cases:

I. PRE_REG only used as input supply for TPS6594x-Q1 and LP8764x-Q1

II. PRE_REG uses as as input supply for TPS6594x-Q1, LP8764x-Q1 **and Jacinto™ 7**

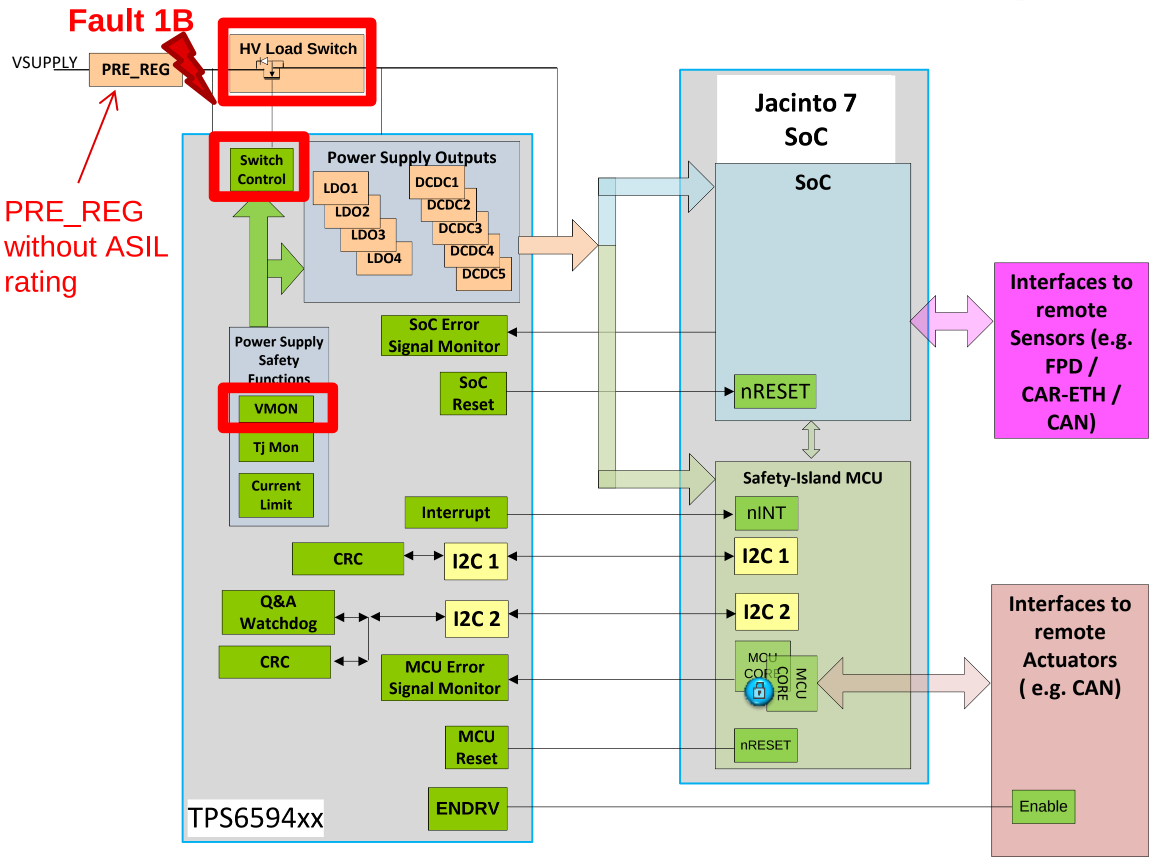
For both uses-cases, TPS6594x-Q1 has following safety features included which allow usage of a PRE_REG without ASIL-rating:

A. Over-Voltage Protection
(for use-case I & II)

B. Under-Voltage Lock-out
(for use-case I & II)

C. UV/OV PGOOD monitoring
(for use-case II only, same error-handling as for Fault 1A)

TPS6594x-Q1/LP8764x-Q1 Safety Concept



Fault 1B

PRE_REG without ASIL rating

PMIC puts system in assumed safe state for failures which would cause improper operation of the Safety MCU or SoC.

These failures include:

1. A) Failures in supply voltages to Safety MCU or SoC

1. **B) Failure in input supply voltage to PMIC**

Objective of TPS6594x-Q1 input over-voltage protection:

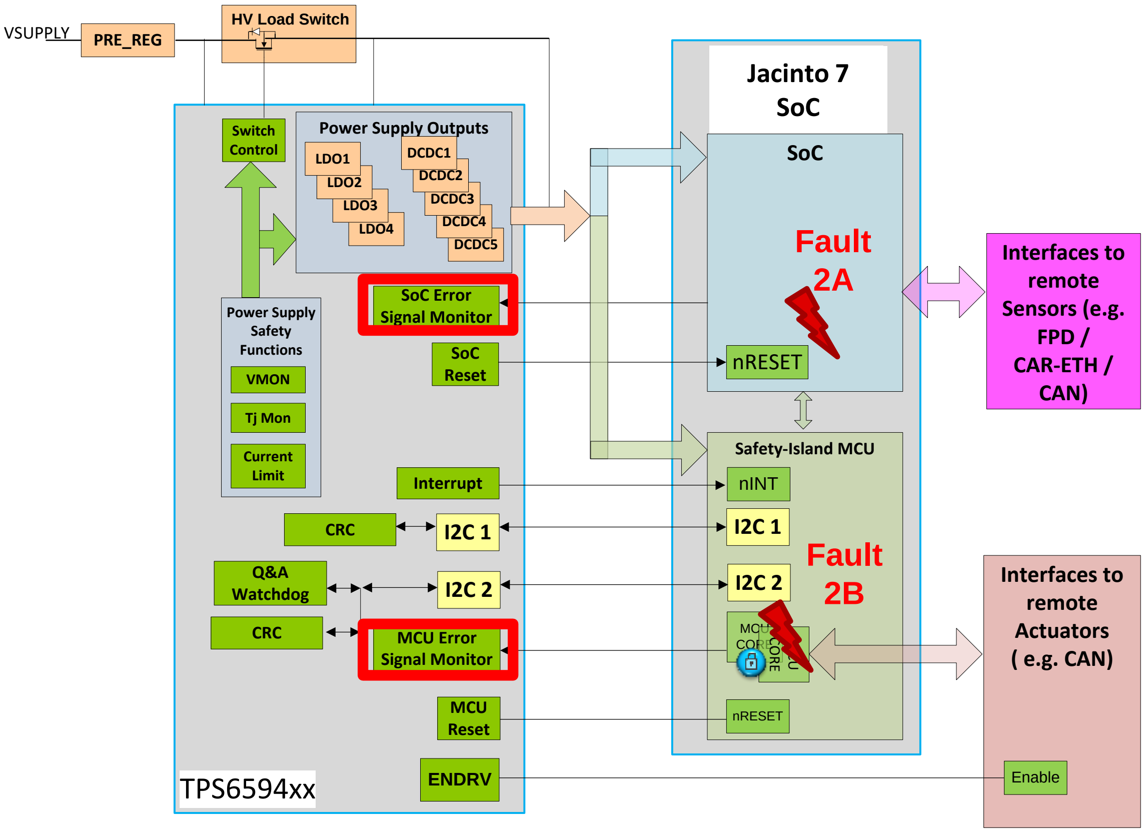
KEEP VCCA voltage < EOS voltage level of TPS6594x-Q1 to allow TPS6594x-Q1 keeping system in safe state

How?

In case of PRE_REG overvoltage, TPS6594x-Q1 opens external FET fast enough

⇒ Complete system will reach a powered-down state, which is a safe state from Functional Safety point-of-view

TPS6594x-Q1/LP8764x-Q1 Safety Concept



PMIC puts system in assumed safe state for failures which would cause improper operation of the Safety MCU or SoC.

These failures include:

1. A) Failures in supply voltages to Safety MCU or SoC

1. B) Failure in input supply voltage to PMIC

2. **A) SoC hardware error**

2. B) Safety MCU hardware error

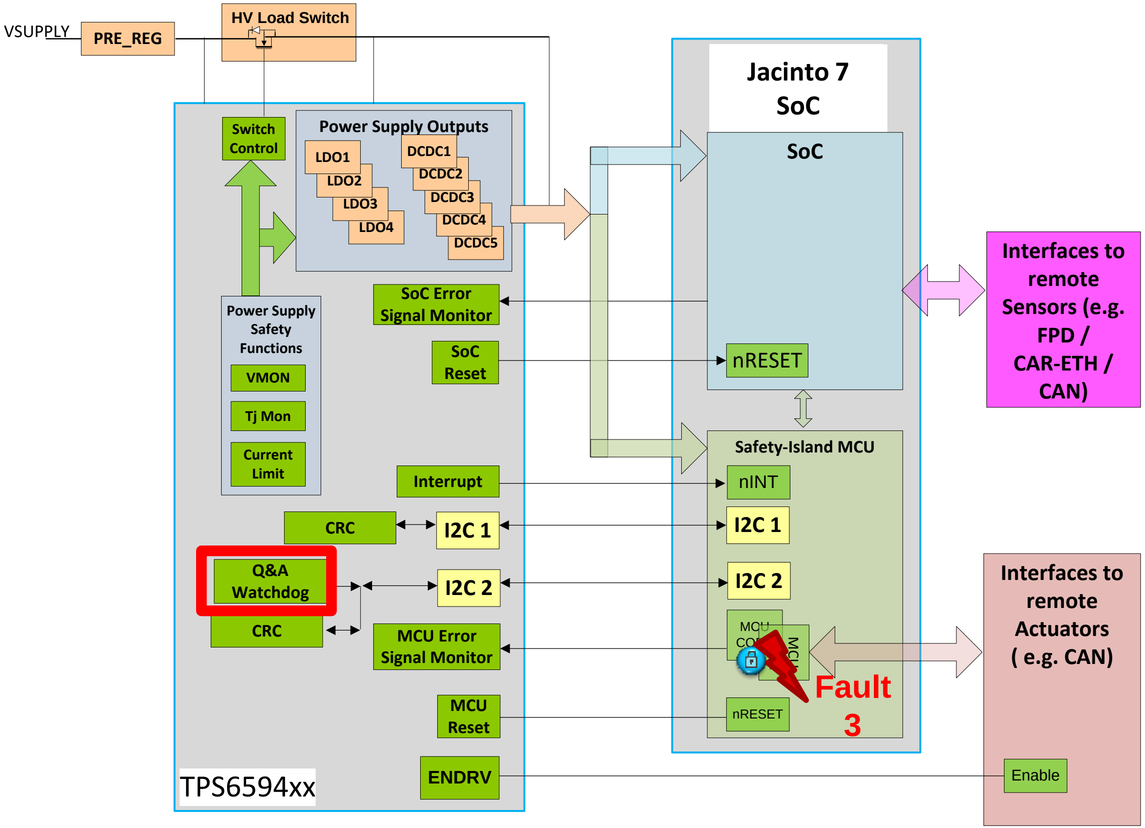
3. Safety MCU software error

Safety function in TPS6594-Q1 for detecting:

- **Fault 2A: SoC error signal monitor**
- **Fault 2B: MCU error signal monitor**

Customer support: PMIC SDK for **Jacinto 7 SoC** *for setting up the ESMs will be available at RTM (Q1 2021)*

TPS6594x-Q1/LP8764x-Q1 Safety Concept



PMIC puts system in assumed safe state for failures which would cause improper operation of the Safety MCU or SoC.

These failures include:

1. A) Failures in supply voltages to Safety MCU or SoC

1. B) Failure in input supply voltage to PMIC

2. A) SoC hardware error

2. B) Safety MCU hardware error

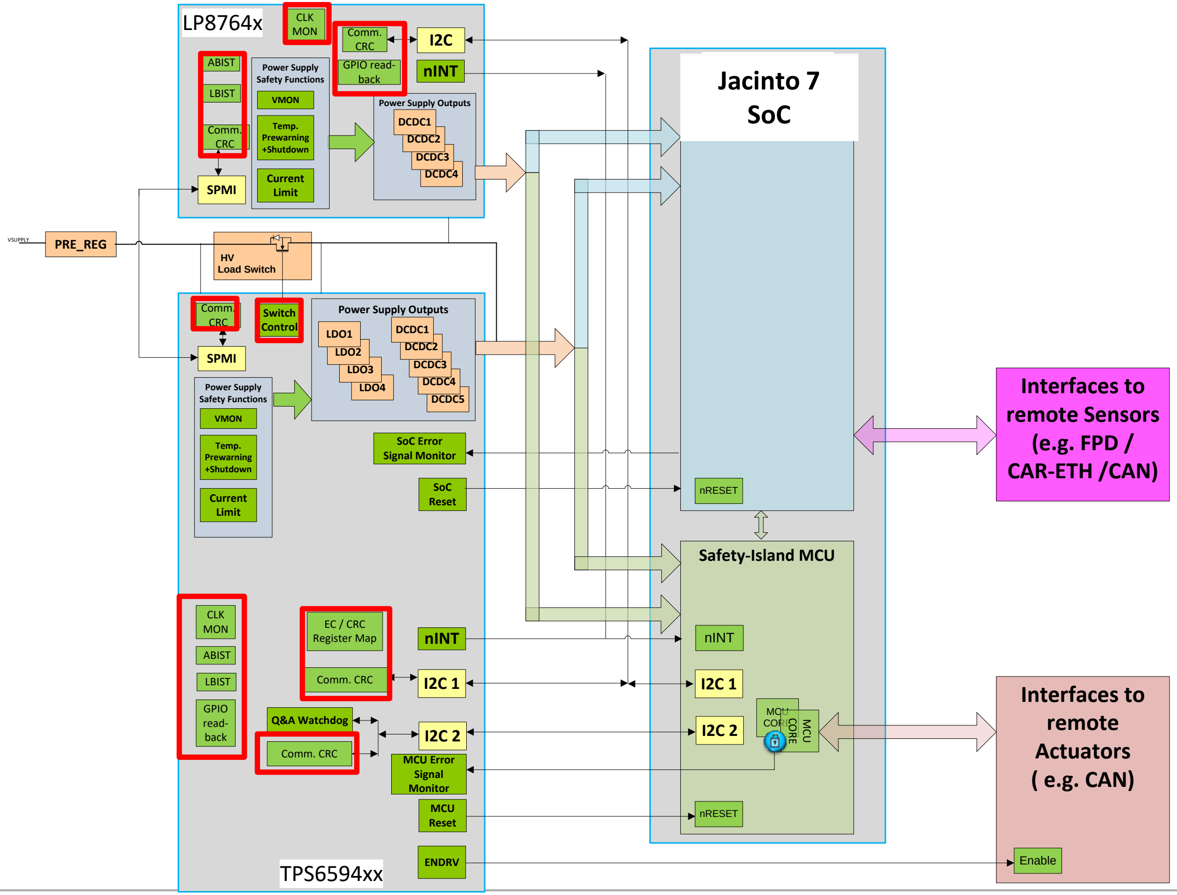
3. **Safety MCU software error**

Safety function in TPS6594-Q1 for detecting fault 3:

- **Q&A watchdog**

Customer support: PMIC SDK for **Jacinto 7 SoC** *for setting up the watchdog will be available at RTM (Q1 2021)*

Safety Concept for supplying Processor



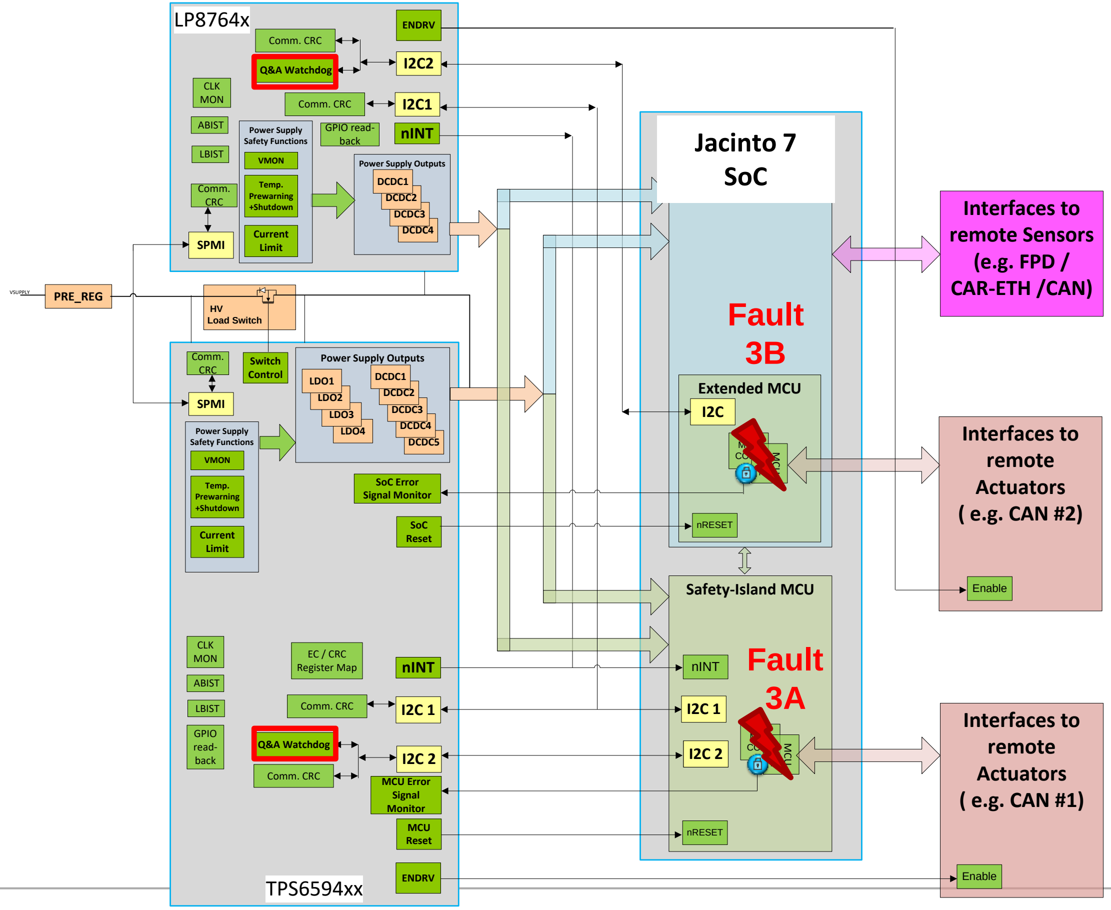
Safety mechanisms inside each PMIC for internal faults :

- Clock monitor
- Internal bias voltage monitor

Safety mechanisms inside each PMIC for latent-faults:

- ABIST (for VMON and temp monitor)
- LBIST (for watchdog, error signal monitors, Error handling logic, I2C interfaces, clock monitor)
- CRC on volatile and non-volatile memory
- Read-back on EN_DRV, nRSTOUT, nRSTOUT_SoC, nINT
- Watchdog + CRC on PMIC interconnect bus
- CRC on I2C interfaces
- Fail-short test on VSYS-OVP FET

Alternative Safety Concept with Extended MCU: 2nd Watchdog



PMIC puts system in assumed safe state for failures which would cause improper operation of the Safety MCU or SoC.

These failures include:

1. A) Failures in supply voltages to Safety MCU or SoC
1. B) Failure in input supply voltage to PMIC
2. A) SoC hardware error
2. B) Safety MCU hardware error
3. **A) Safety MCU software error**
3. **B) Extended MCU sofware error**

Safety function for detecting fault 3A:
- **Q&A watchdog in TPS6594xx**

Safety function for detecting fault 3B:
- **Q&A watchdog in LP8764x**

Thank you for joining.

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