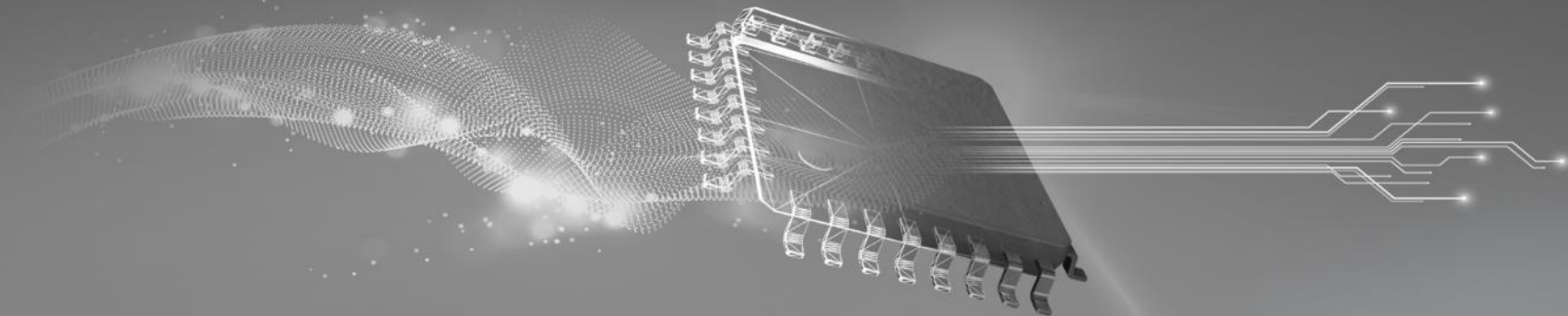


# TI TECH DAYS



## Optimizing your automotive system with Jacinto™ 7 SoCs and MCU integration

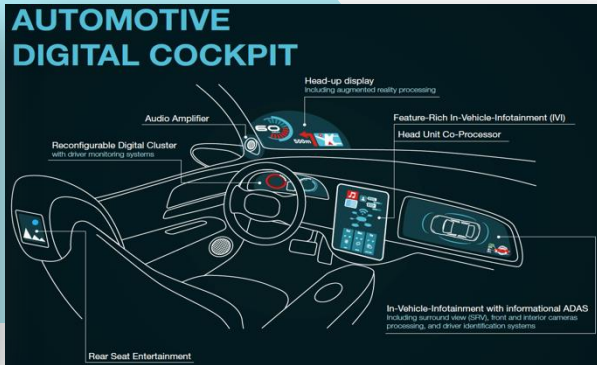
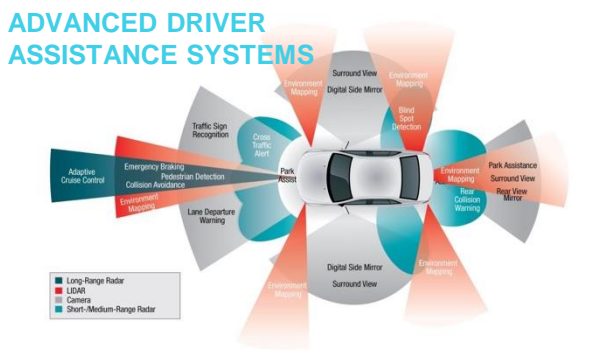
Eric Best

Texas Instruments

# Jacinto™ 7 SoCs



Common IP, software & Tools  
Safety & Security



Front Camera	Driver Monitoring
Surround View	CMS / Mirror Replacement
Sensor Fusion / Domain	Lidar / Time of Flight
Radar	Rear Camera

Integrated Cockpit	Digital Cluster
Center Stack HMI	Heads-Up Display
Silverbox	V2V / V2X
Rear-seat	Vehicle compute, Gateway

**2** **150+ million**  
Auto Processor SoCs on the road in more than 35 OEM brands

2010 Launch of first processor with dedicated ADAS analytics accelerator.

2012 TI announces "Jacinto" family of infotainment processors.

2014 TI builds on strong list of ADAS accomplishments by producing award-winning CHRYSLER Lane 2 with up to 10 TDA ADAS SoCs in one vehicle.

2015 Continued recognition for ADAS processors  
 CES | Texas Instruments infotainment processor drives Ford Sync 3  
 BMW | Texas Instruments infotainment processor drives BMW Connected Drive Platforms

Texas Instruments infotainment processor "Jacinto" family powers VW MIB II  
 IEEF | TI receives 4 awards for white papers  
 Collaborating with SWC and Altaba to develop the internet car

2016 **15+ Million** ADAS SoCs on the road (in more than 25 OEM brands)

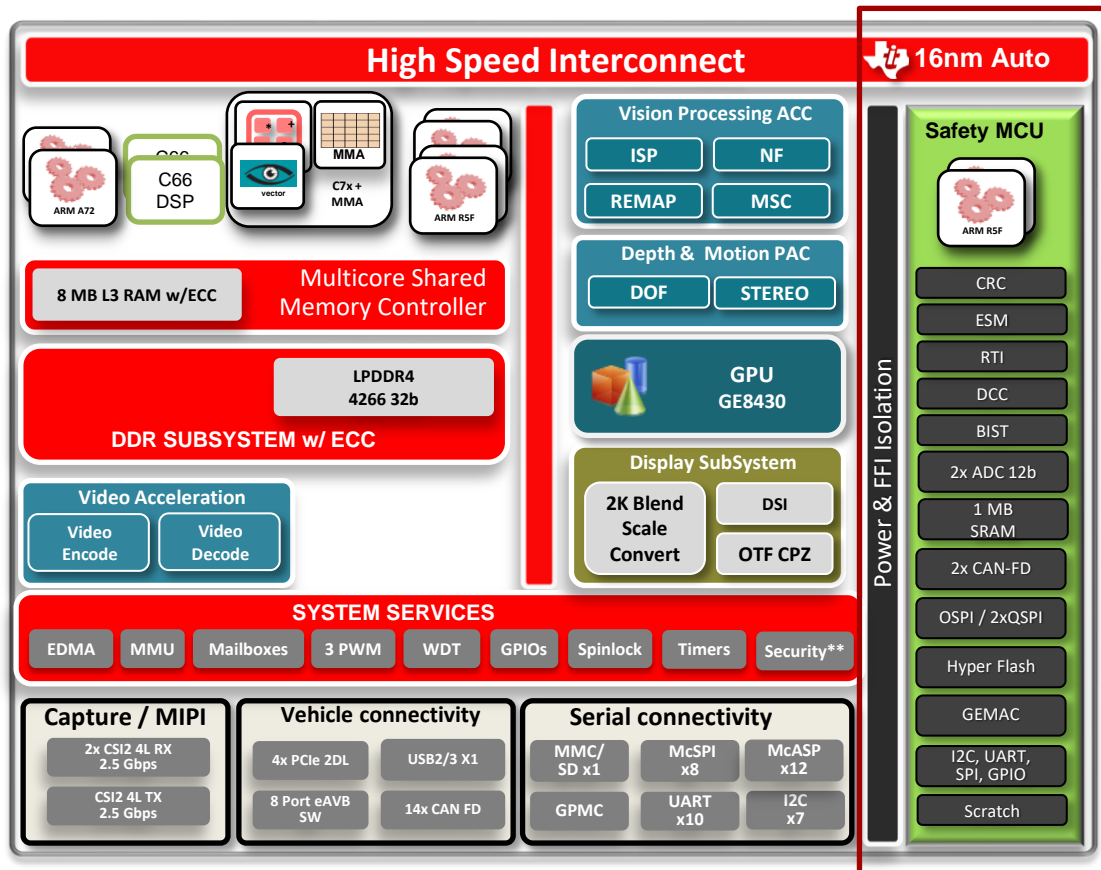
2017

Texas Instruments strong history with signal processing has produced strong results in the automotive industry, and will continue to enable the leading integrated digital cockpit and autonomous driving solutions of the future.

# TDA4V-MID

## Integrated Safety MCU

# Available Now



### Processing Cores

- 2x ARM Cortex A72 @ 2GHz
- 1x C71x DSP + MMA @ 1GHz
- 2x C66 DSP @ 1GHz
- Up to 8 MB Shared on-chip memory w/ECC
- 3x ARM Dual Cortex R5F dual/lock-step
- Vision Acceleration – VISP, VPAC, DOF, SDE
- 1x GE8430 GPU (100 GFLOPS)

### Video / Vision

- 2x CSI-2 (4 lane) x 2.5Gbps Camera interface
- 1x CSI-2 TX Output interface
- Multiformat encode/decode (H.264 Encode up to 180 MP/s for 1080P)
- DSS: Scale, Blend, Convert
- 1x 2.5K, 1x 4K Display OTF composition, increased number of layers/flexibility
- 4L DSI interfaces

### Memory IO

- 1x 32b LP-DDR4X-4266
- 1x MMC/SD/SDIO: 1x UHSI 4b, 1x eMMC v5.1
- 1x SDIO 4b SD s4.0, SATA: 1 lane
- 1x OSPI (166 MHz SDR / 80MHz DDR) / 1x HyperBus™

### High-Speed IO

- 4x PCIe Gen 3, USB3.1, USB2.0

### Automotive IO

- 16x CAN Controllers supporting CAN A&B, FD
- 8 Port Ethernet Switch

### Safety

- Up to ASIL D safety MCU
- High Security\*\* Version

**Package:** 24x24mm BGA, 0.8mm pitch

**Power Dissipation** Typical Range: 12 to 20W @ 125CTj

# History of TI's Integrated Safety MCU

## Mature IP

- The MCU island leverages mature core and peripheral IP blocks (R5F, UART, SPI, RAM, ECC, DCC, etc), which are all well proven on many devices within TI's broad family of SoC's.

## ASIL D Heritage

- The MCU island is technology based on TI's [Hercules™ TMS570](http://www.ti.com/microcontrollers/hercules-safety-mcus/overview.html) stand-alone Safety MCU family, which has shipped millions of automotive units over 15+ years. These devices are TÜV SÜD certified IEC61508 SIL3 and ISO26262 ASIL D microcontrollers for automotive and industrial applications. TI is leveraging the same safety concept and ISO26262 design methodology in TDA4. See: <http://www.ti.com/microcontrollers/hercules-safety-mcus/overview.html>

## Robust Safety Case

- The MCU Island is already available on several 28nm processor derivatives addressing applications with heavy functional safety requirements. The IP is validated, robust and delivering performance to spec.
  - Safety documentation, MCAL, and AUTOSAR availability.
  - AUTOSAR (R5F) and Adaptive AUTOSAR (A53) demo first shown on DRA804M at CES19.

## Family Approach

- The [Jacinto DRA82XX/TDA4x family of devices](#) leverages the same IP in the 16FF process node, enabling software re-use and scalability for functional safety with superset device first sampled in May 2019.

# Vehicle MCU requirements increasing over time

- Increased **compute power**, to satisfy higher compute needs of complex software
- Increased embedded flash **memory size** to handle more complex software.
- Increased high speed memories to accommodate **large software** (both data and instructions)
- Increased **shared data** with the system application processor
- Multiple Ethernet ports to support **multiple networks**
- Greater number of **I/O interfaces** (such as CAN, LIN, ADC, etc...)
- Up to **ASIL-D safety support** to meet the system safety goals
- **Autosar** for integrated MCU

**TI's solution is to integrate the vehicle MCU**

*Lower Cost*

*Smaller Board Area*

*Higher Performance/Watt*

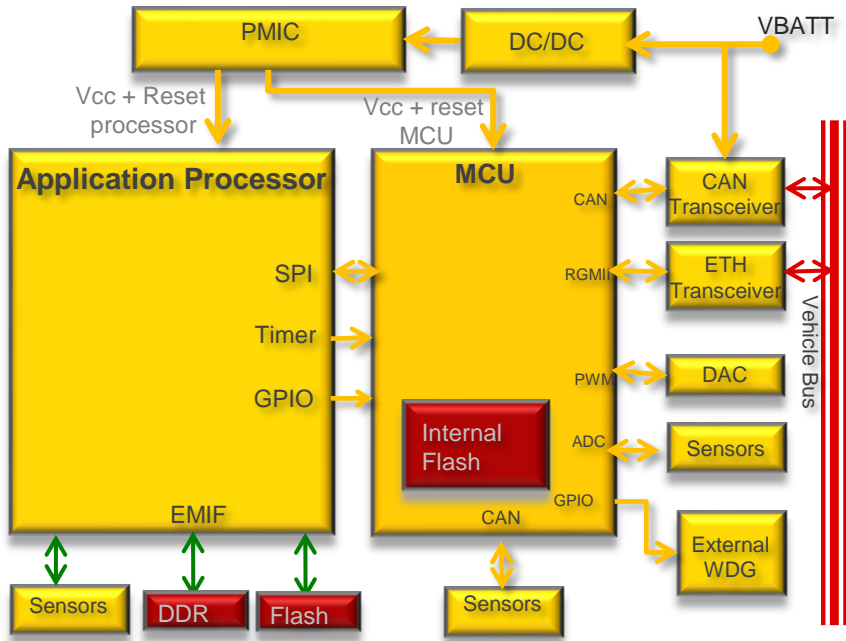
*Higher CPU and Memory Capacity*

# Summary – External MCU vs TDA4 MCU integration

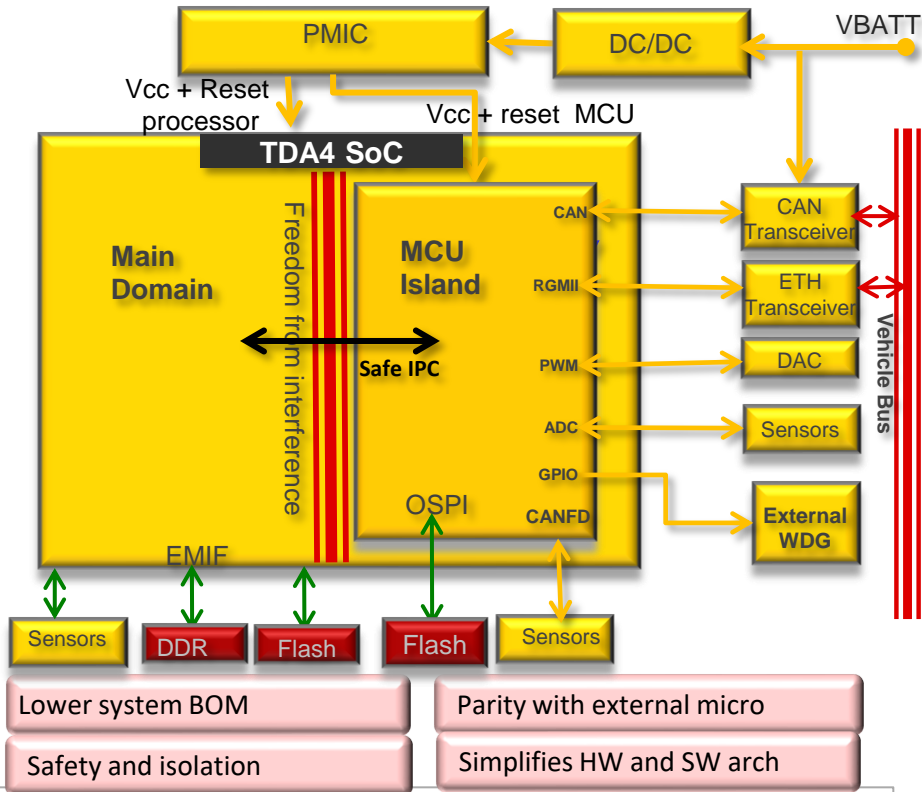
Features	External MCU	TDA4x MCU Integration
Processing cores	Microcontroller cores limited by embedded FLASH access time. Typically 300MHz max with proper wait states	Higher performance cores executing from RAM Multiple R5F cores @1GHz
IO support	CAN, ADC, SPI, GPIO, PMW, Ethernet, I2C	CAN, ADC, SPI, GPIO, PMW, Ethernet, I2C
Power	Meets low-standby current	Meets system level low power requirements. Companion PMIC includes functionality to manage standby current.
Wake-ups	Large number of wakeup sources	Multiple options to support wakeup sources
System BOM	Cost related to flash size, functional safety requirement etc.	Provides significant system BOM saving due to integration of external MCU and decreased PCB area
Boot	Can meet 50-100ms boot time for CAN response	Can meet 50-100ms boot time for CAN response. <ul style="list-style-type: none"> <li>• 30mS general purpose</li> <li>• 42mS secure</li> </ul>
Software development	Separate software development kits	Unified software development with application processor
Flash	Internal flash	External flash (QSPI, OSPI, Hyperflash) XIP Supported. Can support cost effective larger external flash
Apps processor communication	Serial port (i.e. SPI, I2C etc.)	128 bit wide internal bus interface with end to end ECC
Functional safety	Up to ASIL-D	Up to ASIL-D, simplifies safety case for mixed criticality applications.

# Integration in TDA4

## Typical ECU architecture



## Integrated micro with TDA4 - ECU architecture



# TDA4 MCU Island

Peripherals for vehicle and other ECU component connectivity – SPI, CAN, ETH, UART

External flash with on-the-fly security and ECC

12 bit ADC for monitoring

ROM and Efuse Timers/RTI for monitoring

Internal memory for code and data

12 MHz RC OSC for fail safe mode

Temperature monitor and internal

Voltage and Power monitor

**DMSC**  
Separate power, security and resource manager. With Cortex M3, internal memory, AES accelerator

Primary OSC for external crystal

DMA engine for peripherals

Resilient interconnect

MCU safety DTK clock monitoring  
Error Signaling Module  
On chip PBIST and LBIST

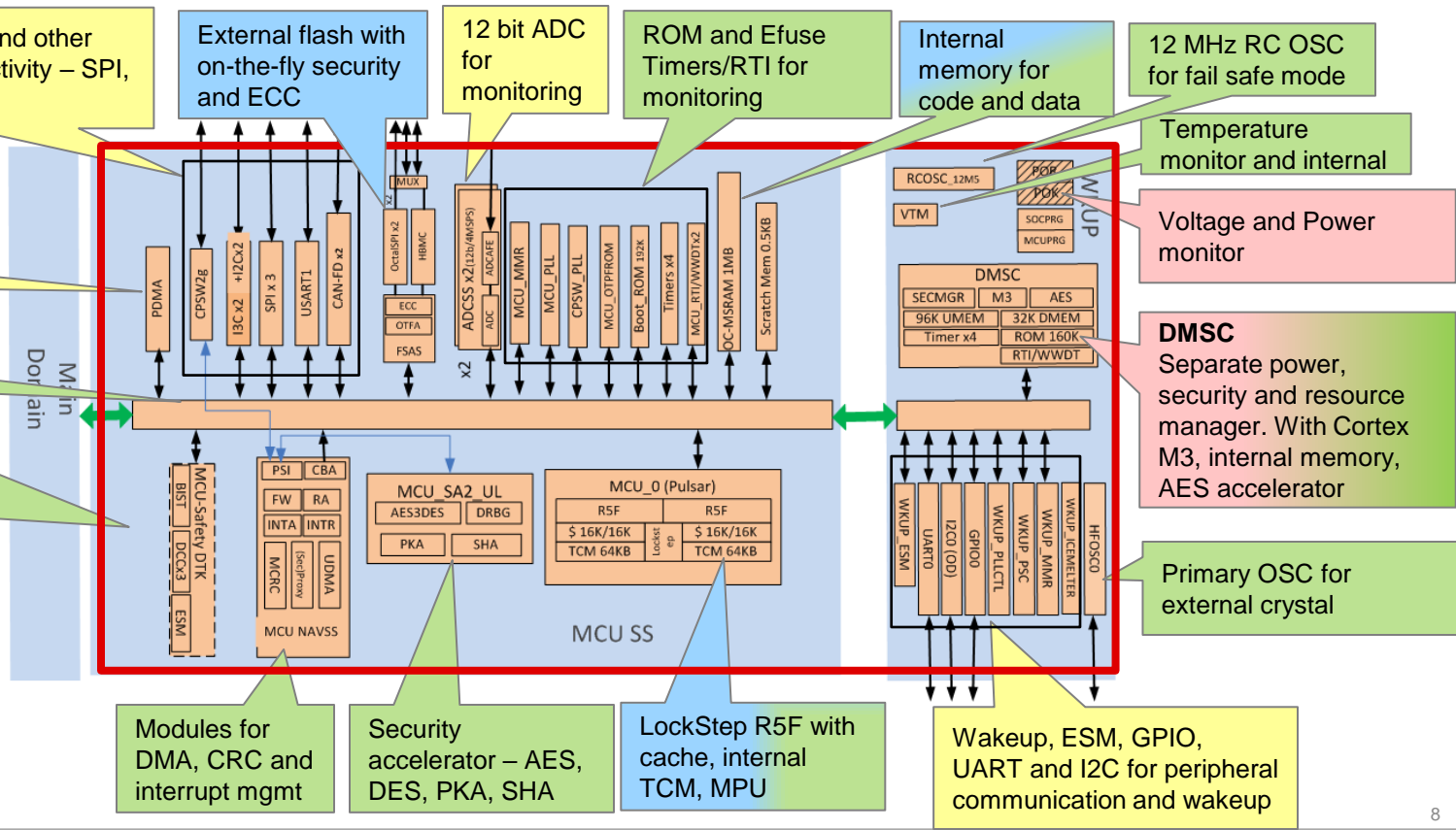
Logical boundary of MCU Island

Modules for DMA, CRC and interrupt mgmt

Security accelerator – AES, DES, PKA, SHA

LockStep R5F with cache, internal TCM, MPU

Wakeup, ESM, GPIO, UART and I2C for peripheral communication and wakeup





# AUTOSAR highlights

AUTOSAR available now from multiple suppliers

- Vector and KPIT official releases in Q1'20

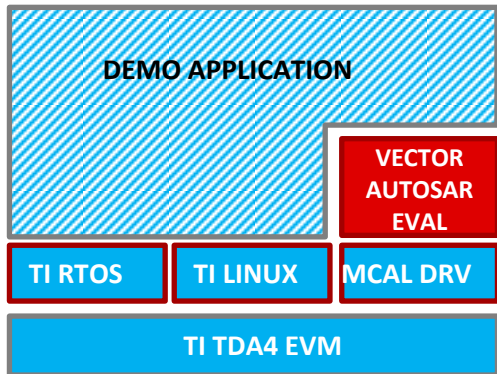
Multiple R5F subsystems allow for flexible architecture

- AUTOSAR on one pair, or across multiple pairs with core partitions

High capacity cores for large headroom

- 2-3x capacity of typical external MCU
- Up to 6GHz of R5F processing

# Vector AUTOSAR pre-integration on TDA4x



AUTOSAR evaluation on TI EVM

## Vector TDA4 AUTOSAR eval package in definition today

- Subset of available AUTOSAR features to enable basic application
- Includes AUTOSAR OS for R5F, limited set of integrated MCAL drivers
- MCAL drivers from Vector or from TI SDK

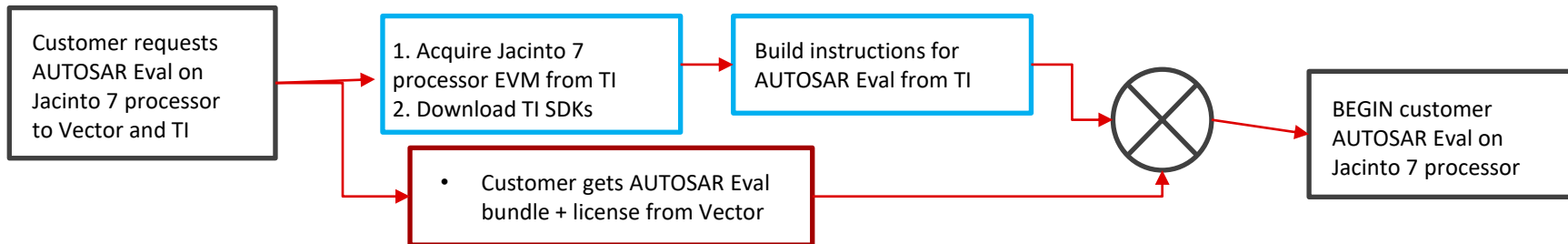
## TI Linux and TI RTOS on processing cores

- Enables quick path to Vector AUTOSAR evaluation

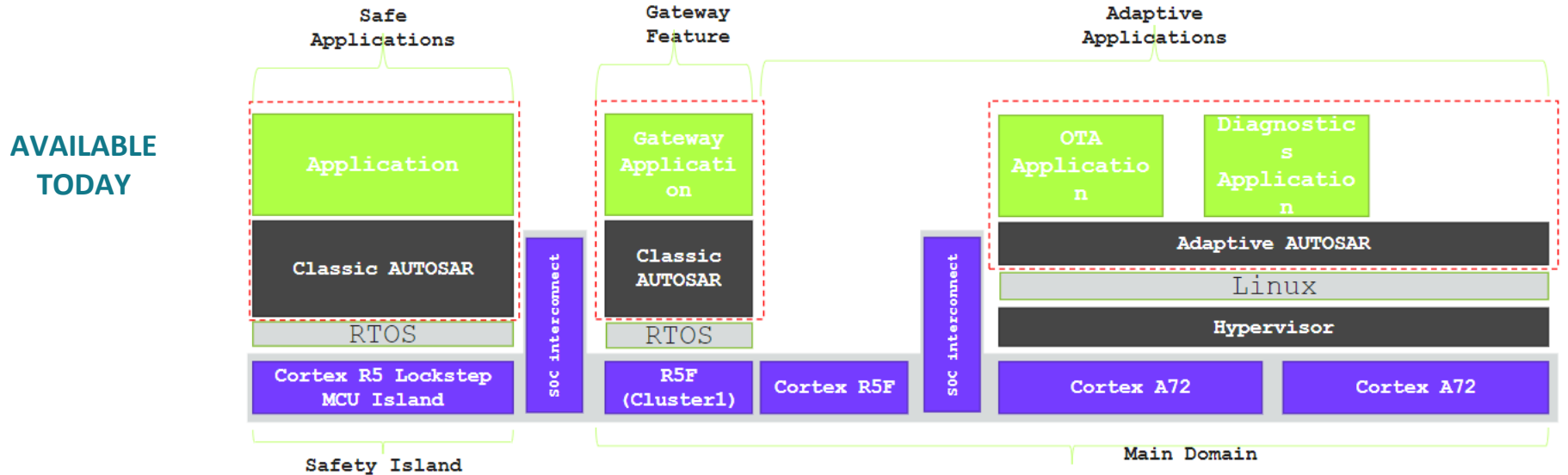
## Simple AUTOSAR communication DEMO app in definition

- Easily re-created by customers with SW packages from Vector and TI

## Enabling Customer Eval on TDA4x – *In work*



# KPIT AUTOSAR pre-integration on TDA4x



## AUTOSAR Classic

- Gateway (CAN TO ETH) on R5F Cluster (Main Domain)
- AUTOSAR Classic on R5F (Safety Island)

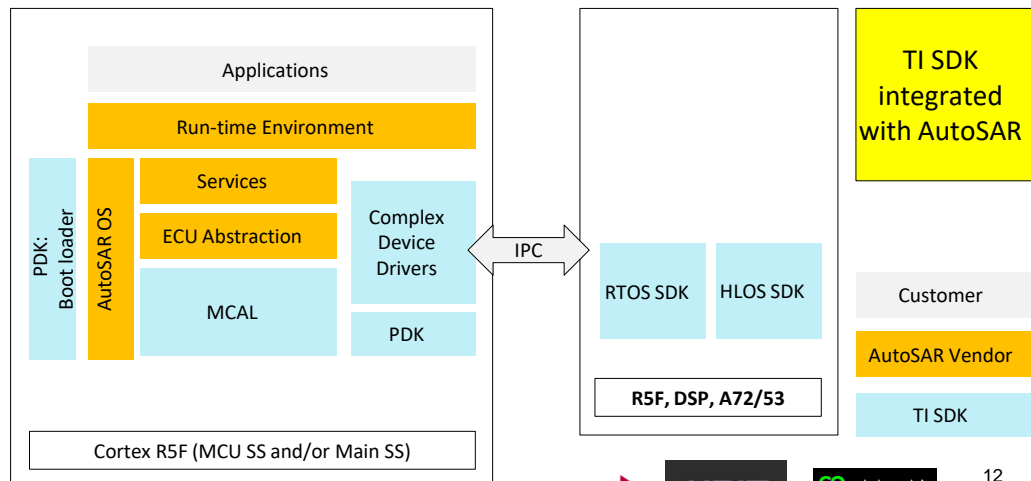
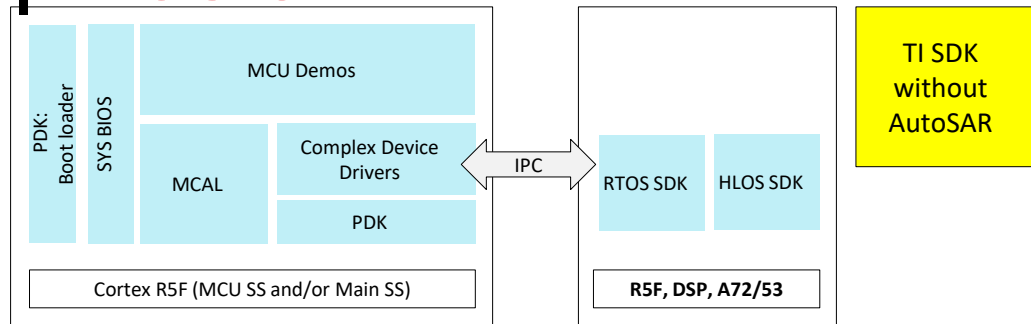
## Adaptive AUTOSAR on A72

- OTA
- V2X stack and applications integration with Adaptive
- Onboard diagnostics services

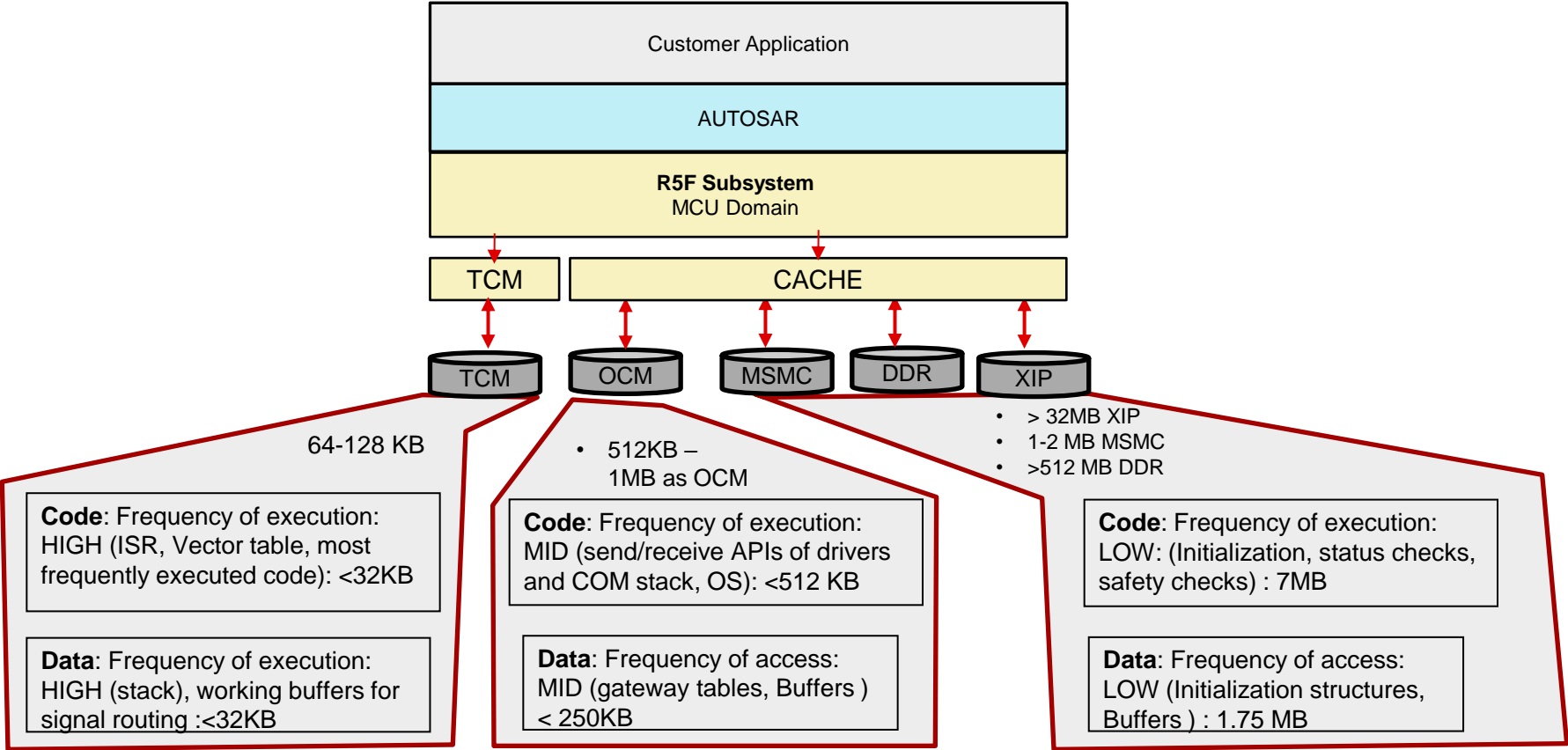
## IPC communication between Classic/Adaptive

# Foundational Software | MCU Software

- Part of **Processor SDK RTOS Automotive**
- TI deliverables enable prototyping with MCAL and without AUTOSAR
  - Inter-Core communication using mailbox and SPI
  - Routing/switching over CAN and Ethernet
  - Reference bootloader for fast boot, XIP execution
  - Other MCU functionality like ADC, PWM in application context
  - Measure CPU load / latency
- AutoSAR integration of TI MCAL available with most AutoSAR vendors
  - **Multi-core AutoSAR support also available**
- MCAL and Complex Device Driver (CDD) delivered by TI
  - ADC, CAN, ETH, ETHTRCV, GPT, PWM, SPI, DIO, WGT
  - CDD: IPC (Inter Processor Communication)
  - EB Configurator tool
- TI MCAL support for functional safety
  - TI MCAL developed with process certified to be compliant with ISO 26262 2018.
  - TI MCAL provided with Compliance Support Package



# Customer SW architecture – recommended mapping for MCU/Main R5F



# TDA4 R5F 1x1GHz performance vs 4x300MHz Flash MCU

1 x lockstep R5F of TDA4 compared to 4 x lockstep cores of non-TI highest performing MCU

TI TDA4

Typical Flash MCU

1 pair x R5F in Lockstep @ 1GHz ~ 2K DMIPs  
**AUTOSAR benchmark on TDA4 R5F**  
 Setup: RTOS, 16 task, I\$ miss rate: 3.5M/sec

4 pair cores in lockstep @ 300MHz ~ 2.4K DMIPS  
**Estimated AUTOSAR benchmark on Other MCU**  
 Setup: RTOS, 16 task, I\$ miss rate: 3.5M/sec

•DRA82x baseline  
 •R5F cache size (32KB)  
 •TCM 64KB

•Performance impact due to multiple core

•SW Architecture – Code placement, DMA  
 •Lockstep TCM: 64 -> 128KB

MCU R5F

OCM	XIP
1	1.8

No impact

• No Impact

Frequency of access

75%	25%
1.2	

20% performance degradation compared to OCM code execution

• Code with higher frequency of access in TCM and OCM RAM : 75%  
 • Code with lower frequency of access in Flash/XIP

• 1 x lockstep R5F pair has XIP performance just 20% worse than 4 x lockstep cores (highest performing external MCU)  
 • TI TDA4x has up to 3 x R5F lockstep cores: ~ 2.5x more performance than typical high performing MCU

• Baseline configuration: Other MCU have similar cache and TCM config  
 • Latency slightly better than TI as they operate at lower frequency  
 • Flash latency similar to OCM latency for code access

MCU R5F

OCM	XIP
0.7	0.8

30% degrade

• Impact of 30% due to function split into multiple cores (Amdahl's law)

• Code with higher frequency of access in TCM and OCM RAM : 75%


Frequency of access

75%	25%
1.0	

Similar performance compared to OCM code execution

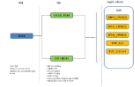
# Software and tools - overview

AUTOSAR MCAL + Configurator



ASIL D capable MCAL for AUTOSAR BSW integration

Bootloader




QM Bootloader given as reference for device boot sequence and operation

Code Composer Studio




Code Composer Studio™ IDE is an Eclipse-based development environment

Emulators




HW emulator for easy debug from multiple vendors- Spectrum Digital, BlackHawk, Lauterbach

Diagnostic Library




ASIL D capable SW diagnostic library for checking the correctness of all checkers

Reference MCU PDK




Reference PDK SW demonstrating MCU Island operation and interaction with Main Domain

Compiler



TI Compiler for various cores of MCU Island – used with CCS or command line

HW Simulation platform




VLAB SoC Simulator from ASTC

Low level Drivers

```
01001000
01100101
01101100
01101100
01101100
01101111
```

ASIL D low level drivers for peripherals, power management and device control

Flash Programming



Flash programming tool for external flash using standard interface

Compiler Qualification toolkit



Qualification tool kit for meeting safety requirements

TI partner Network



Extensive 3P network for AUTOSAR, Safety OS, Hypervisor, Services, Application

# TI TDA4A MCU benefits

## TDA4x for mainstream ADAS Safety

- **Native Safety Support**
  - ASIL-D Systematic Capability
  - Internal diagnostics (up to ASIL-D)
  - Certification and collateral
- **Mixed Criticality**
  - Firewalls, Voltage, Clocks, Interconnect
- **MCU island**
  - High FFI
  - External MCU replacement
- **Extended MCU**
  - More ASIL-D DMIPS
  - DDR

## Lowest risk

- Proven technology node; reliable execution → development can start today!
- TDA4x backed by a team of 600+ TI engineers & domain experts
- Proven support in Automotive

## Best cost of ownership

- Lower BOM with integration of safety MCU
- Reusable: Common micro and SW platform from L1 → L4, gateway/vehicle compute, cockpit
- High performance MCU subsystems
- Architected for lowest external DDR footprint
- Low power to reduce thermal management costs

## Automotive heritage

- TDA4x leverages TI's extensive history in automotive processors (15+ years across 35 OEMs, over 250 Munits)
- Automotive Safety heritage: Over a decade experience with ASIL-D processing (TMS570)
- System level solutions designed for Automotive: SoC, interface and power





**©2020 Texas Instruments Incorporated. All rights reserved.**

The material is provided strictly "as-is" for informational purposes only and without any warranty.  
Use of this material is subject to TI's **Terms of Use**, viewable at [TI.com](https://www.ti.com)

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale ([www.ti.com/legal/termsofsale.html](http://www.ti.com/legal/termsofsale.html)) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2020, Texas Instruments Incorporated