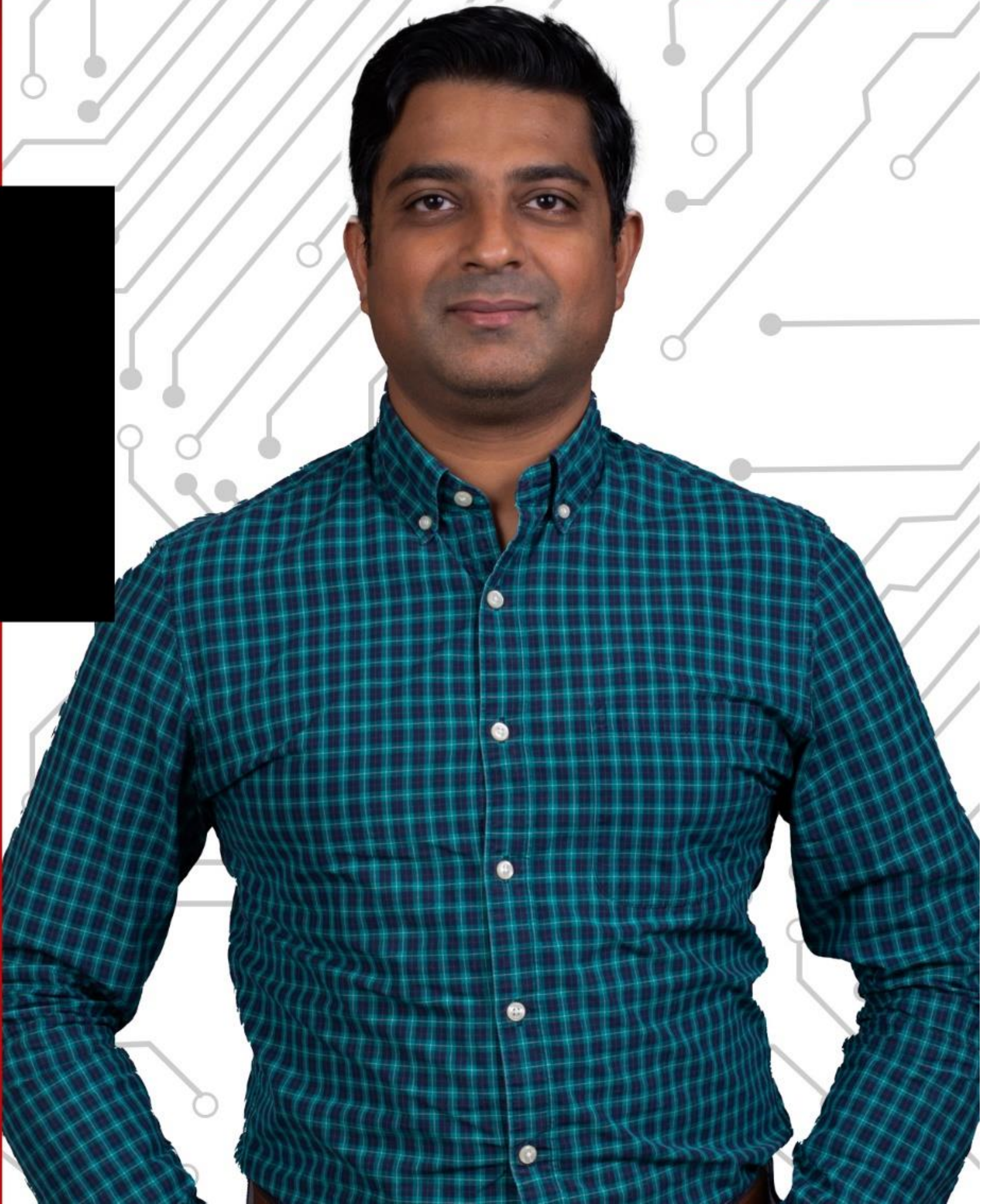
Texas Instruments

TI POWER

TI *Live!* BATTERY MANAGEMENT SYSTEMS SEMINAR

SID SUNDAR

SYSTEM-LEVEL CONSIDERATIONS FOR MULTI-CELL INDUSTRIAL BATTERY PACKS



Key challenges in industrial battery packs

- Handling high energy densities and currents safely
  - Handling high series currents
- Safety criticality
  - Adhering to safety and functional safety standards
- Communication outside the battery pack
- Accurate measurement and gauging, often in the presence of noise
- Large transient and peaky loads
- Optimizing standby power – power management

We will discuss how to tackle each of these challenges using the appropriate combination of electronics

Battery electronics options

Level of Integration

Gauge

- Reports capacity, run-time and state of charge
- Enhanced current, voltage and temperature protections
- Diagnoses battery failure with black box features
- Extends run time of battery by accurately determining how much capacity is remaining
- Extends lifetime by dynamically controlling healthy, safe and fast charging
- Enables battery authentication and traceability

Highest integration

Monitor

- Measures individual cell voltages
- Measures current (coulomb counting)
- Measures die temperature and external thermistors
- Extends battery run time and battery life through cell balancing
- Provides voltage, current and temperature protections with flexible thresholds
- Communicates data and status to MCU or standalone gauge

Highest flexibility

Protector

- Responds to unsafe conditions like over-voltage, under-voltage, over-current, over-temperature, under-temperature, over-current or short circuit

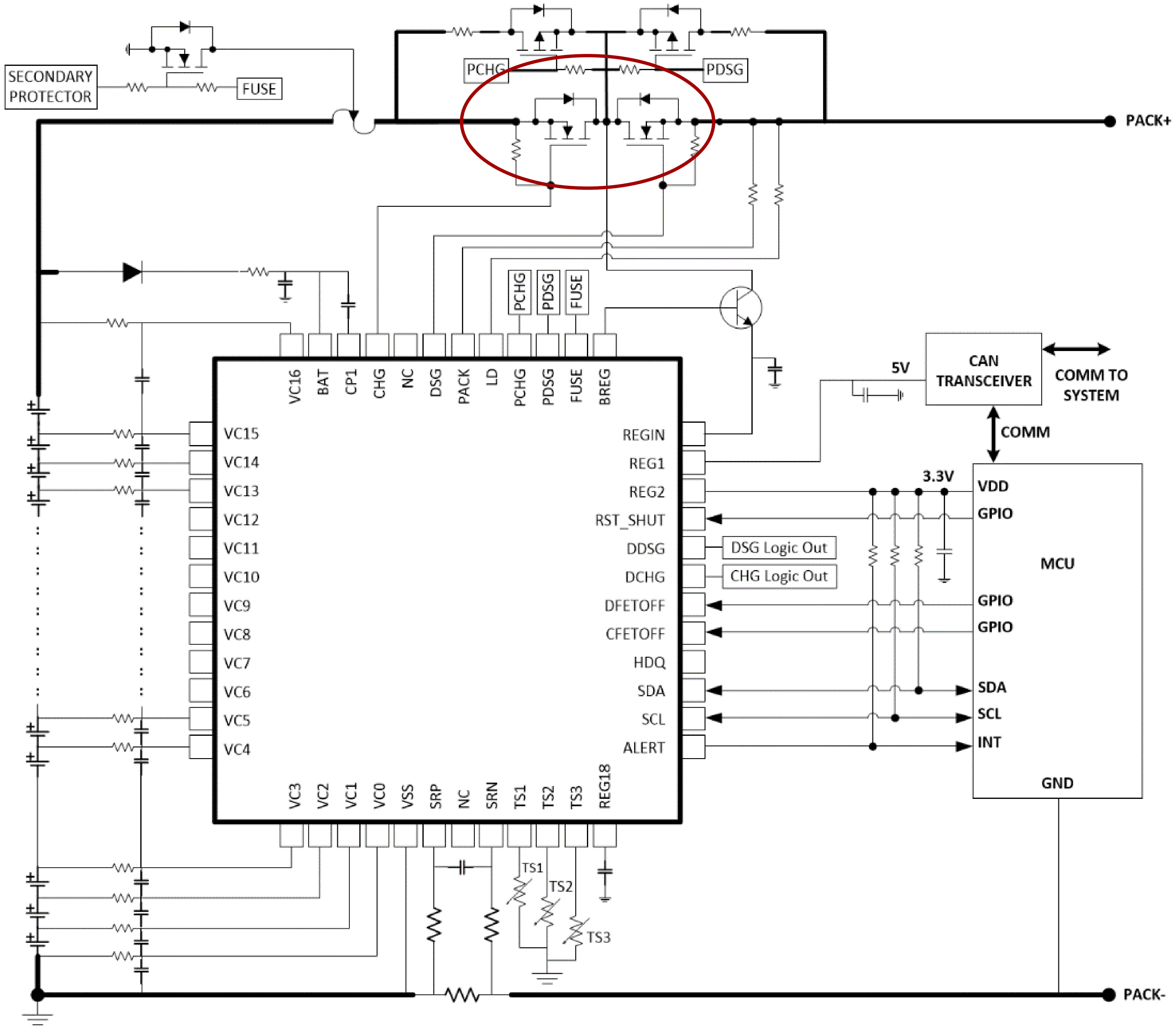
Lowest complexity

Handling high energy densities

- Industrial packs often have high energy storage needs, e.g., UPS
- Need to monitor temperature closely to prevent thermal runaway
  - May need to monitor temperature in multiple places
  - Support by using monitor with multiple thermistor inputs
- Cell balancing may be needed to ensure individual cells don’t get overcharged or discharged
  - Depending on balancing currents, cell balancing may use internal FETs in monitors or need external FETs with for higher currents
- May need distinct thresholds to be used for overcurrent detection in charge and discharge modes
- May choose to use high-side or low-side protection FETs

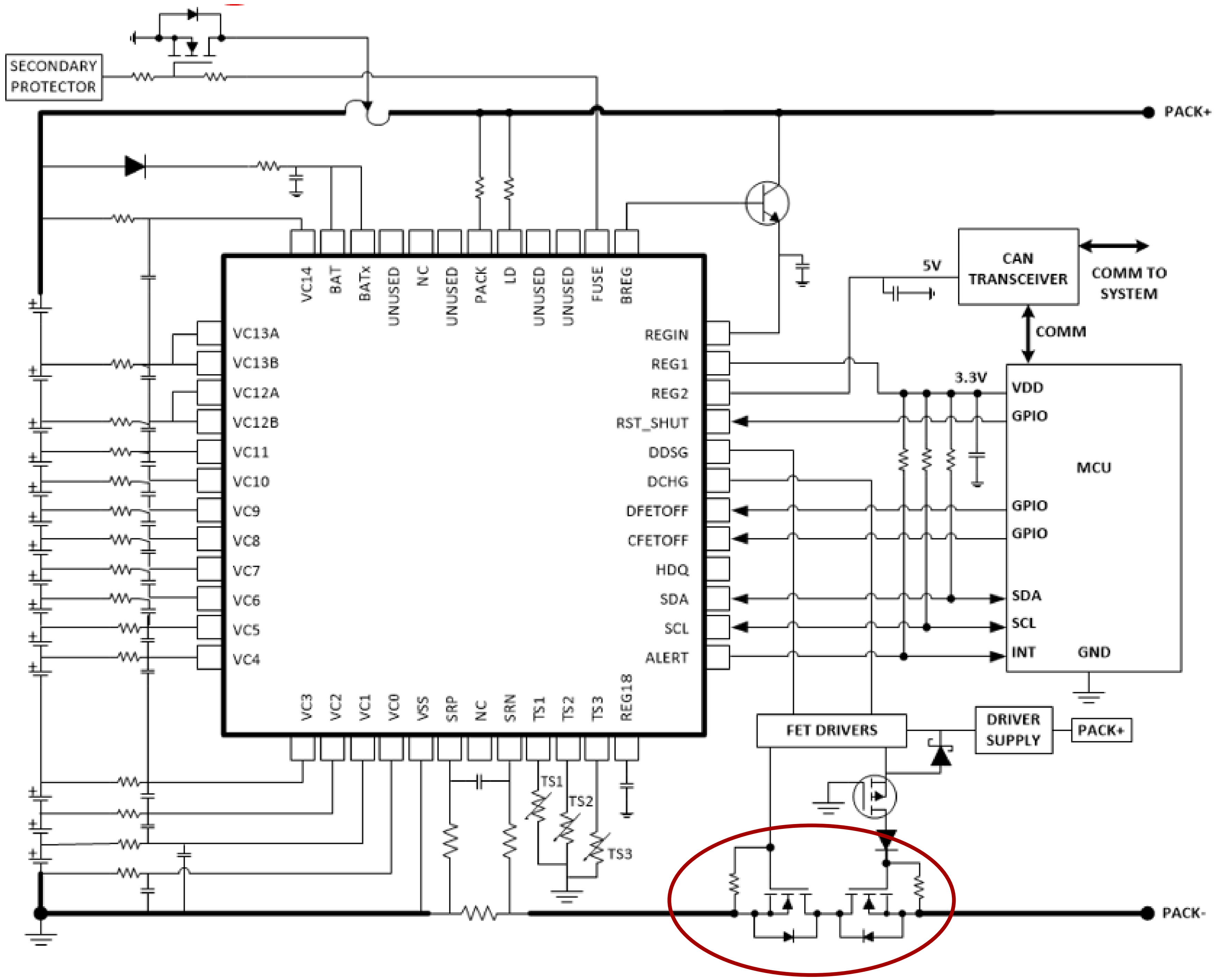
High-side driver

- Benefits
  - Allows for pack communication to outside world during fault conditions – not switching ground
  - No need for isolated communications
  - Typically used in 48 V and lower systems
- Drawbacks
  - Needs a charge pump to drive FETs
  - Increases system voltage
  - Challenges in stacked system and HV systems



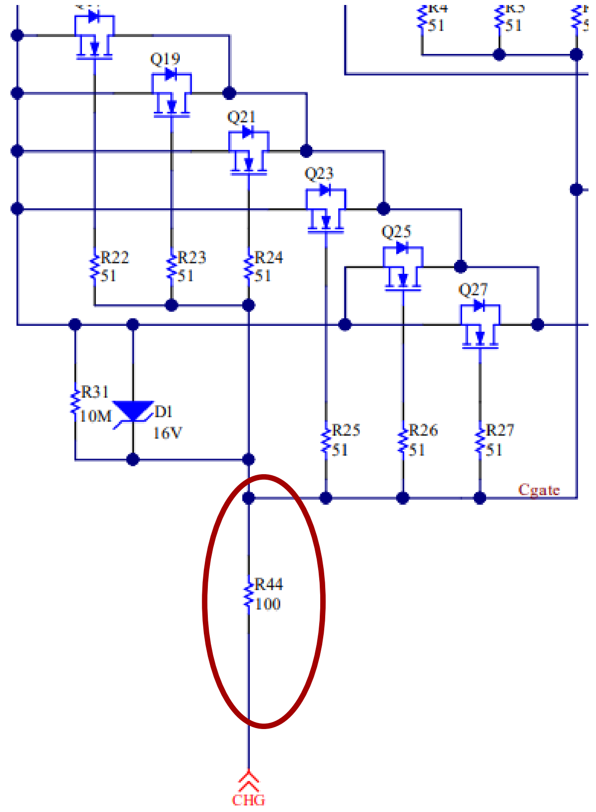
Low-side driver

- Often used in systems where communication to the pack in fault conditions is not needed, or in HV systems where isolated comms are already mandated
- Benefits
  – Typically lowest cost and complexity of implementation
- Drawbacks
  – Breaks ground plane - pack communication during fault is an issue
  – Will need an isolator to communicate outside the pack during faults



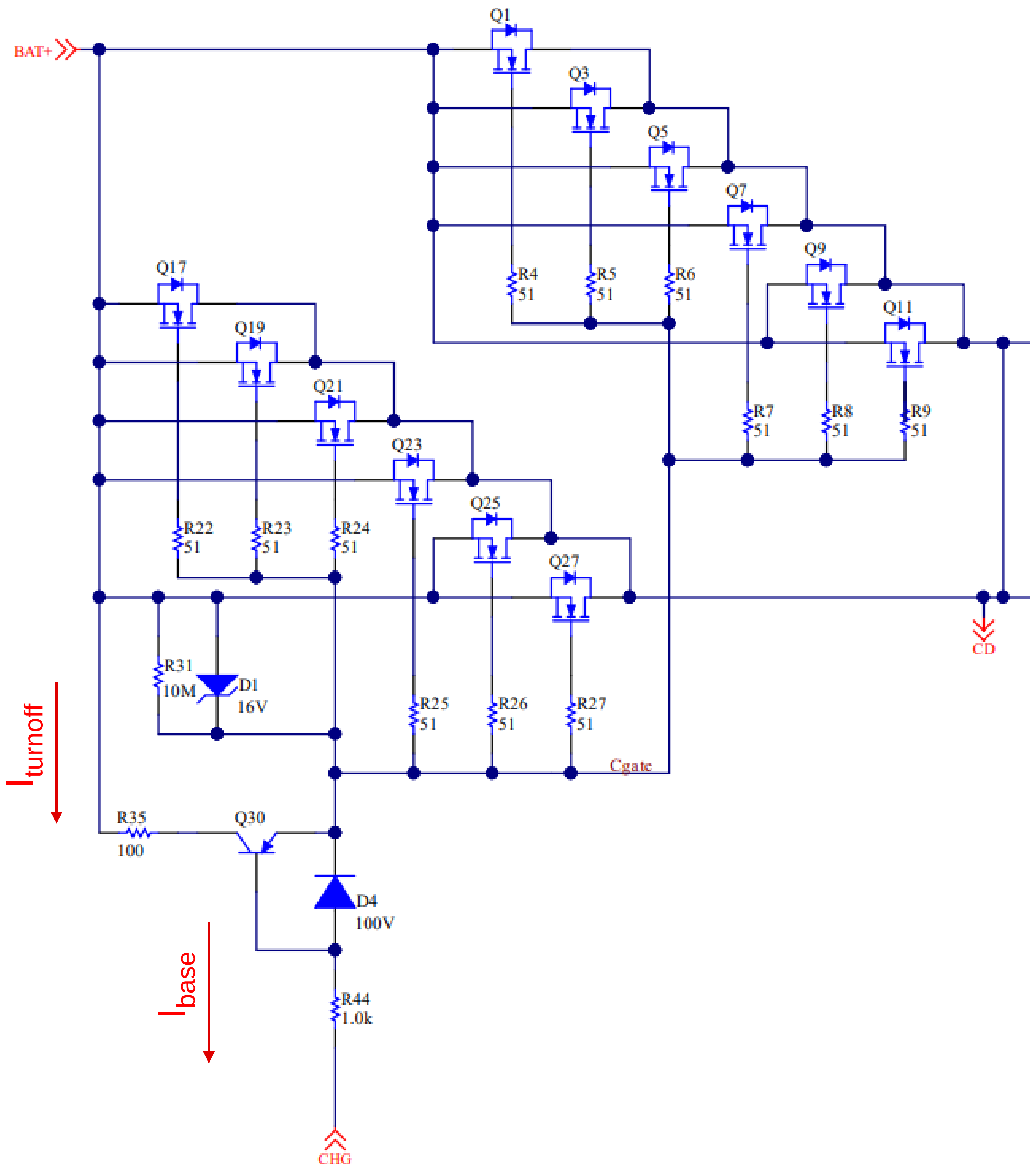
Handling high-series currents

- Applications like power tools and UPS often have very high series current requirements, such as 10s of A, necessitating the use of parallel FETs
  - Ensure the gate driver is capable of driving combined capacitance without excessively increasing risetime
  - Use symmetric layouts to minimize thermal hotspots and current crowding
  - FET capacitance may cause ringing during switching – detune gate capacitance if needed by series resistance on CHG and DSG pins



Local turn-off for large loads

- For large loads, the gate resistance combined with the internal driver resistance may be too large to support rapid turn off.
- Use a PNP (Q30) with smaller series resistance to create a low impedance local discharge loop for FET capacitance during turnoff

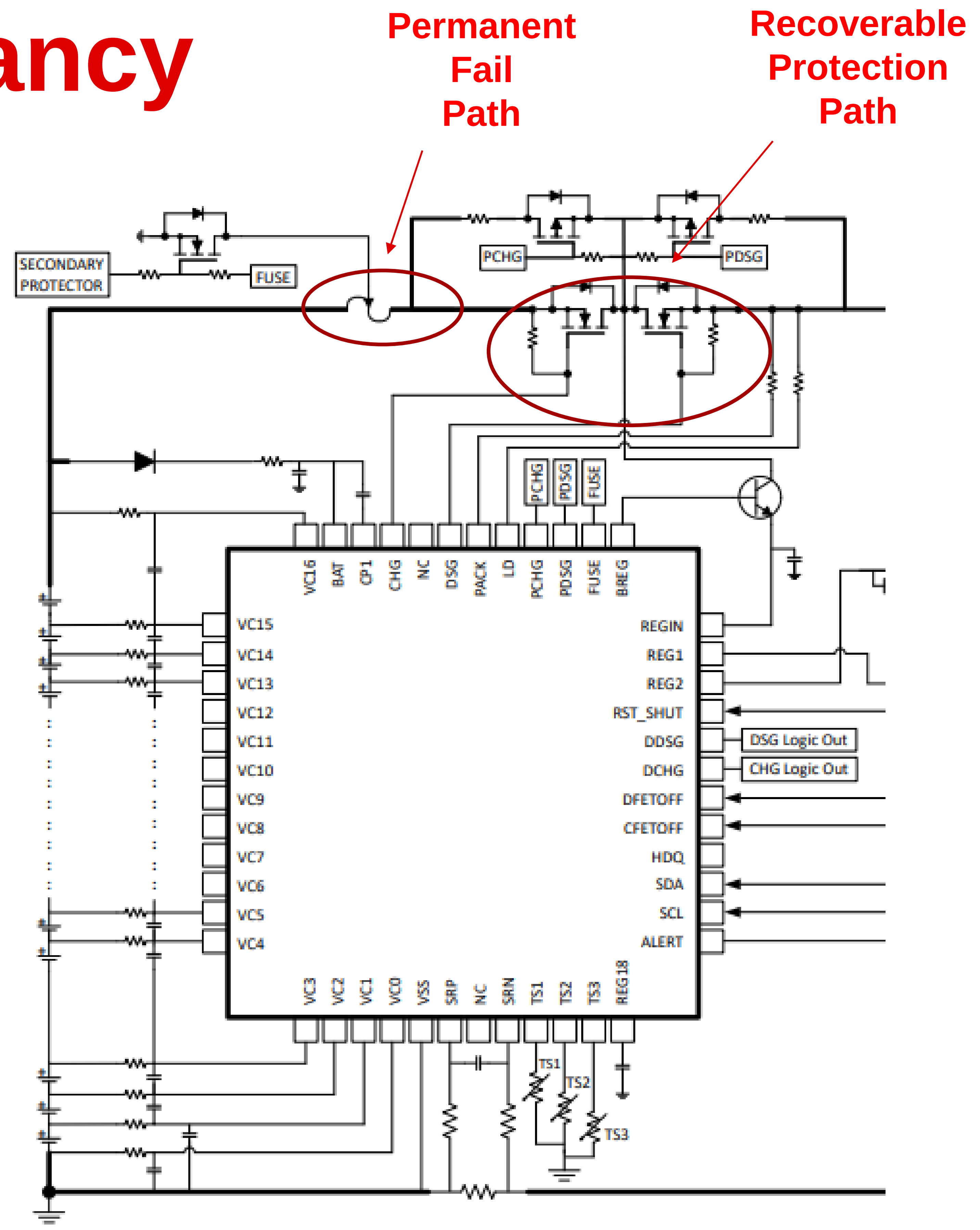


Functional safety and battery management

- Functional safety in battery management systems is often mandated for compliance with regulatory standards, such as:
  - UL 2595, IEC 60335, IEC 62841, etc.
- Some key factors to consider:
  - The goal of functional safety is to detect and handle abnormal events and place the state in a risk-addressed state – normal operation is not generally required
  - Functional safety is generally system level, not component level
  - Independent, redundant systems (circuits/ICs) must often meet requirements
    - Focus is often on tolerance of single point of failure
  - In-built diagnostic features can help to identify faults and place the system in a safe state
- Attend the "Implementing Functional Safety Systems…" session for more info.

Safety criticality and redundancy

- With high energy densities and safety being paramount, redundancy and diagnostic capabilities are often a must
- A typical solution uses a monitor with built-in protection as a first line of defense and protector as redundancy or backup
- Protector may be used to trigger permanent fail or recoverable failure
  – Permanent failure settings are typically set to be more extreme than recoverable settings
  – E.g.: Monitor may have OVP set to 4.2 V, while secondary protector may be set 4.4 V with longer delay



Autonomous operation

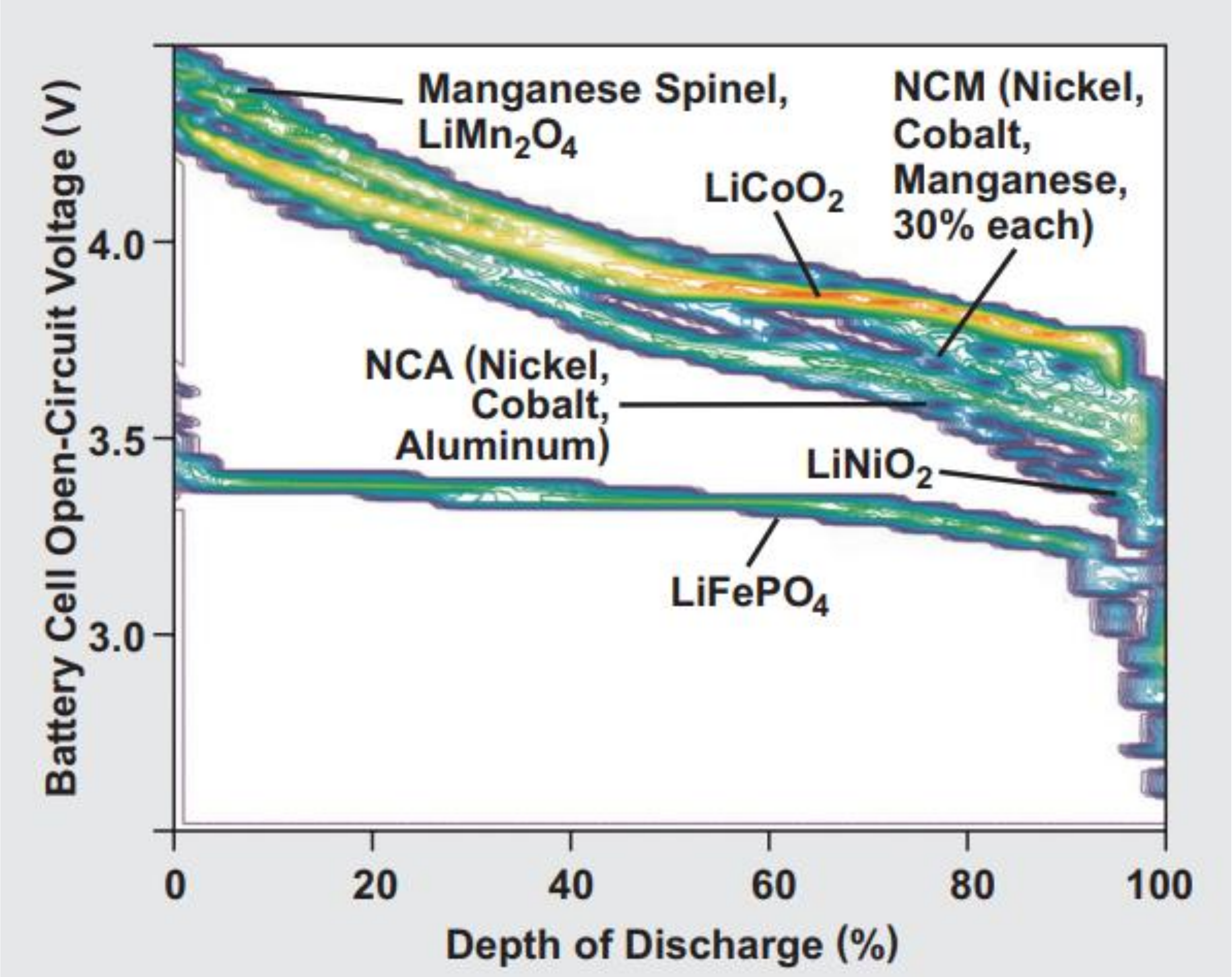
- Traditionally, monitors relay information to MCUs in the pack, allowing MCUs to make final decisions
  - Provides flexibility and allows for system use case modification
  - E.g., it may be safer to allow a drone to drop rotor speed than to disconnect the battery in case of low state of charge
- Increasingly, monitors can operate autonomously of the MCU
  - Trigger and recover protections without MCU intervention
  - Set protection thresholds at factory permanently without MCU involvement
- Benefits of autonomous operation
  - Faster reaction time in case of events like short circuits
  - Eliminates MCU and MCU software from functional safety considerations
  - Uses MCU measurements for complete redundancy
  - Keeps MCU in sleep mode while battery use is enabled
- TI's BQ769x2 family of monitors can work in autonomous or MCU-controlled modes.

Transient performance and electrostatic discharge (ESD)

- Supply voltage may jump above DC during peak loads and short circuit events
- Some best practices:
  - Test the system to ensure short circuit/step loads do not trigger any issues
  - Ensure on board components have sufficient margin to tolerate transient spikes, especially ESD related components
  - Ensure FET turn on/off are managed to not trigger fast transients
  - Ensure tight layout around the power FETs to minimize parasitic inductance
- ESD can be a significant concern in some systems – e.g., vacuum cleaners
  - Onboard ESD components often required to handle requirements like IEC-61000
  - TI has example schematics and layouts illustrating how to design a system to pass these standards - https://www.ti.com/lit/an/sluaa15/sluaa15.pdf

Accuracy

- Higher accuracy can extend operating range, reduce pack size, enhance operating life
- Use of new chemistries like LiFePO4 can enhance accuracy requirements
- Flexibility is paramount
  - Gauging may require high accuracy/lower speed, but needs continuous current measurements
  - Protection may optimize speed of response and power over raw accuracy
  - Continuous vs intermittent measurements to save power during non-active states
- Simultaneous V/I measurements can allow the system to accurately compute impedance of the pack at different loads
- TI has gauges, monitors and protectors with best-in-class accuracy to help you optimize your system



Optimizing power consumption

Normal mode
100s of µA

- All protections enabled
- DFET & CFET on
- Regular voltage, current, and temperature measurements
- LDO enabled

- Highest performance for system active state
- Full protections, V / I / T data collected continuously

Sleep mode
10s of µA

- Most protections still enabled
- DFET on (multiple modes), CFET off
- ADC intermittent, CC in current wake detect mode
- LDO enabled (can keep MCU powered)
- Wake by current / comm / charger / reset

- Optimized for system idle state – low load
- MCU can be in low power mode without compromising safety
- V / I / T data collected periodically

Deep sleep mode
10µA

- Most circuits off, FETs off
- No ADC/CC, no protection
- LDO enabled (can keep MCU powered)
- Wake by selected comms / charger / reset signal

- Optimized for system in standby or sleep mode
- Lowest power mode while still providing LDO operation to keep MCU powered

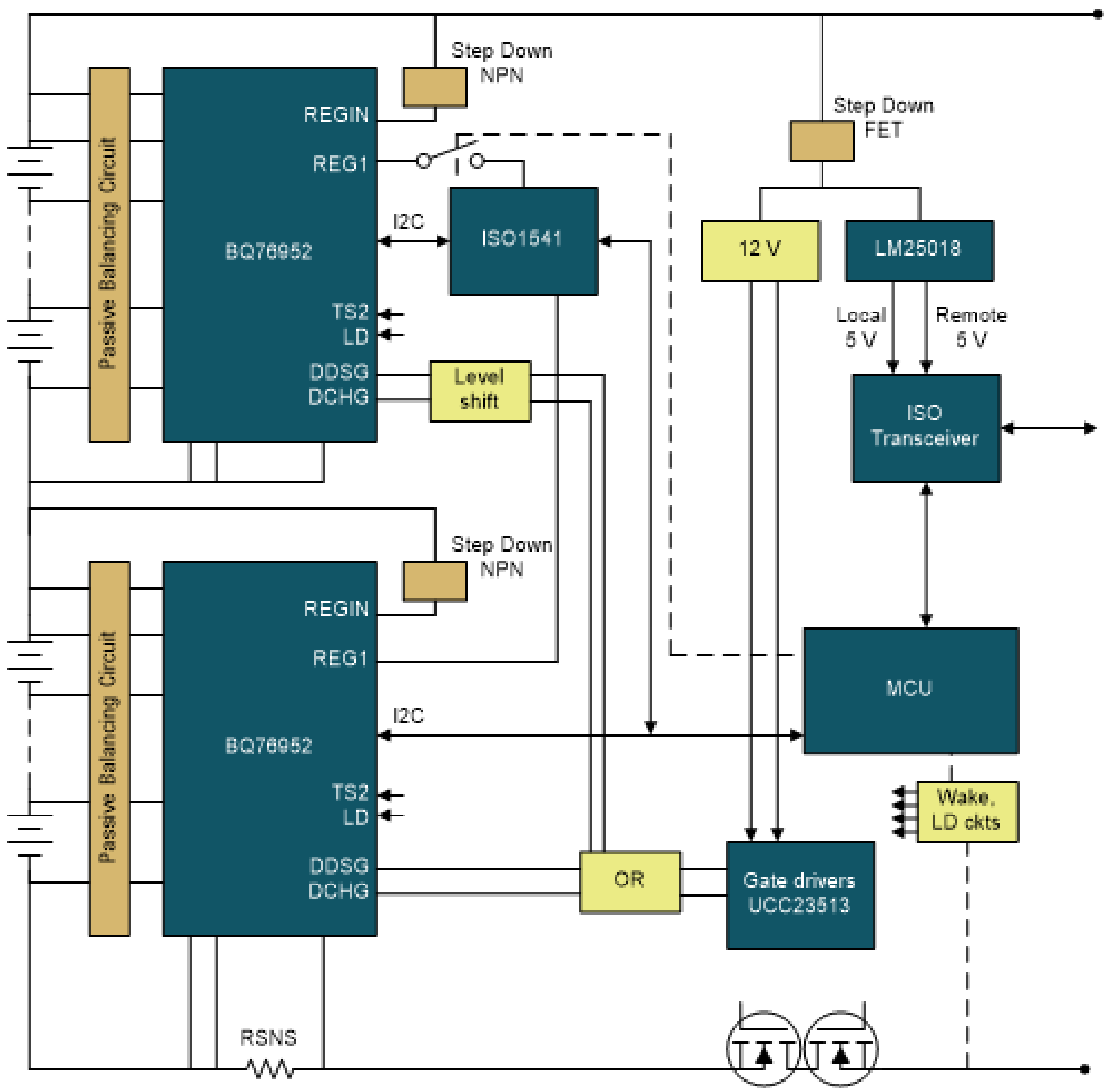
Shutdown mode
sub - µA

- All circuitry off (except wakeup detector)
- No measurements, no protections
- LDO powered off
- Wake by charger attach or button push

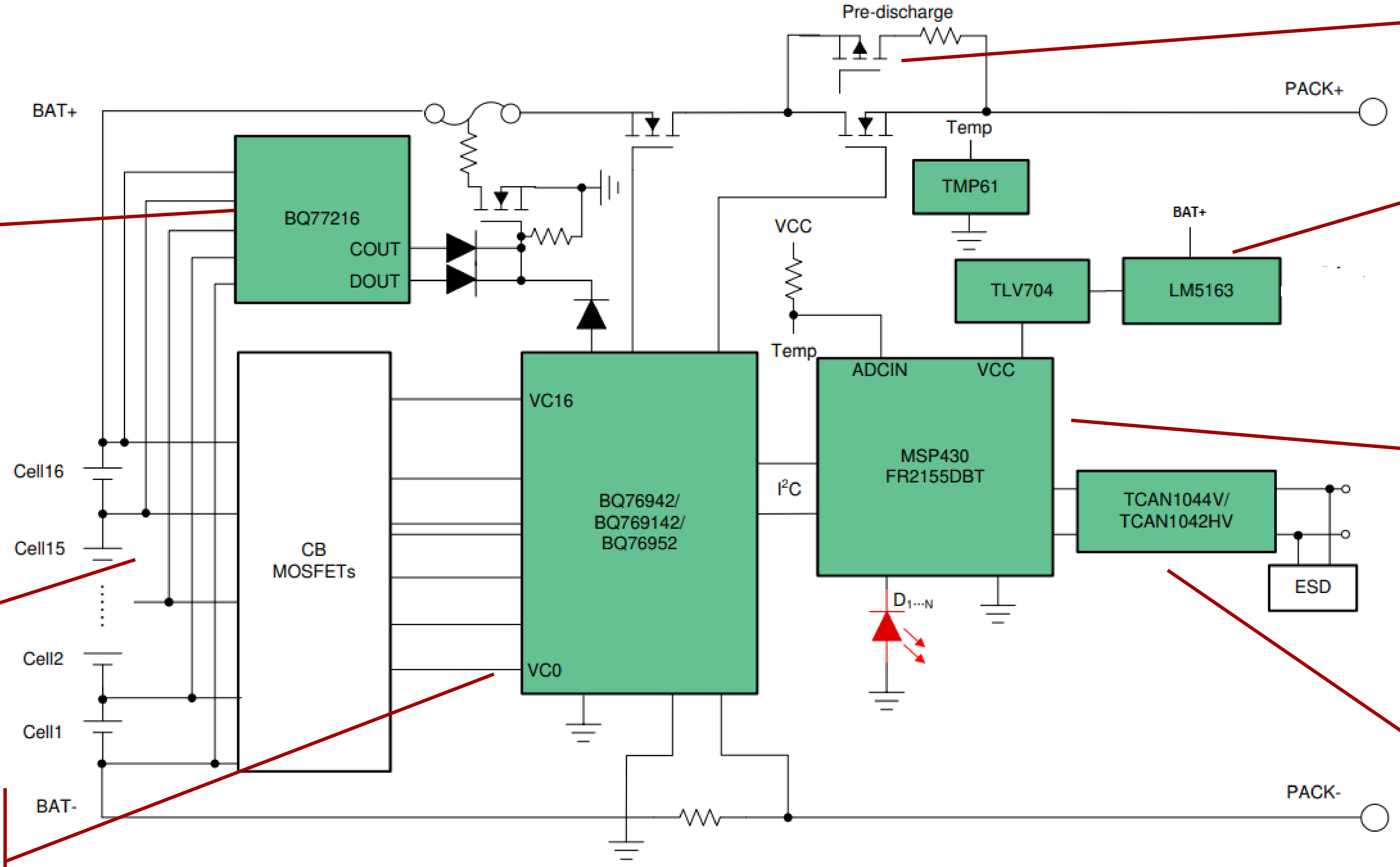
- Lowest power mode for shipping, storage or long-term power-down

Tackling ultra-high cell count systems

- Above a certain cell count (typically 14 -16 cells), there may not be a monolithic monitor capable of measuring all the cells
- Some form of stacking is needed
  - Built in stacking interface
  - On-PCB level translation
- Considerations for on-PCB stacking
  - Use isolated level translators to communicate to upper device comms
  - Can use on board level shifters for basic digital protection signal
  - Consider using a regulator from top of stack to minimize cell imbalance
  - Generally simpler to use low side FETs
  - See here for more details



Reviewing a complete design – TIDA-010208



High side protection FETs with pre-discharge PFET
Pre-discharge FET to soft start

16-cell secondary protector
Secondary voltage protector for redundancy

Discrete LDO arch
Discrete LDO architecture for ultra-low power shutdown mode with memory retention

System MCU
MCU is used to measure thermistor, control comms, LEDs and monitor

Optional external CB
External cell-balancing FETs for high-power systems

CAN transceiver
Industrial systems often use UART or CAN to talk outside the pack

16-cell monitor
Monitors voltage, current and primary protection to control CGH and DSG FETs. I2C comms to MCU

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