TEXAS INSTRUMENTS

TI *Live!* INDIA AUTOMOTIVE SEMINAR

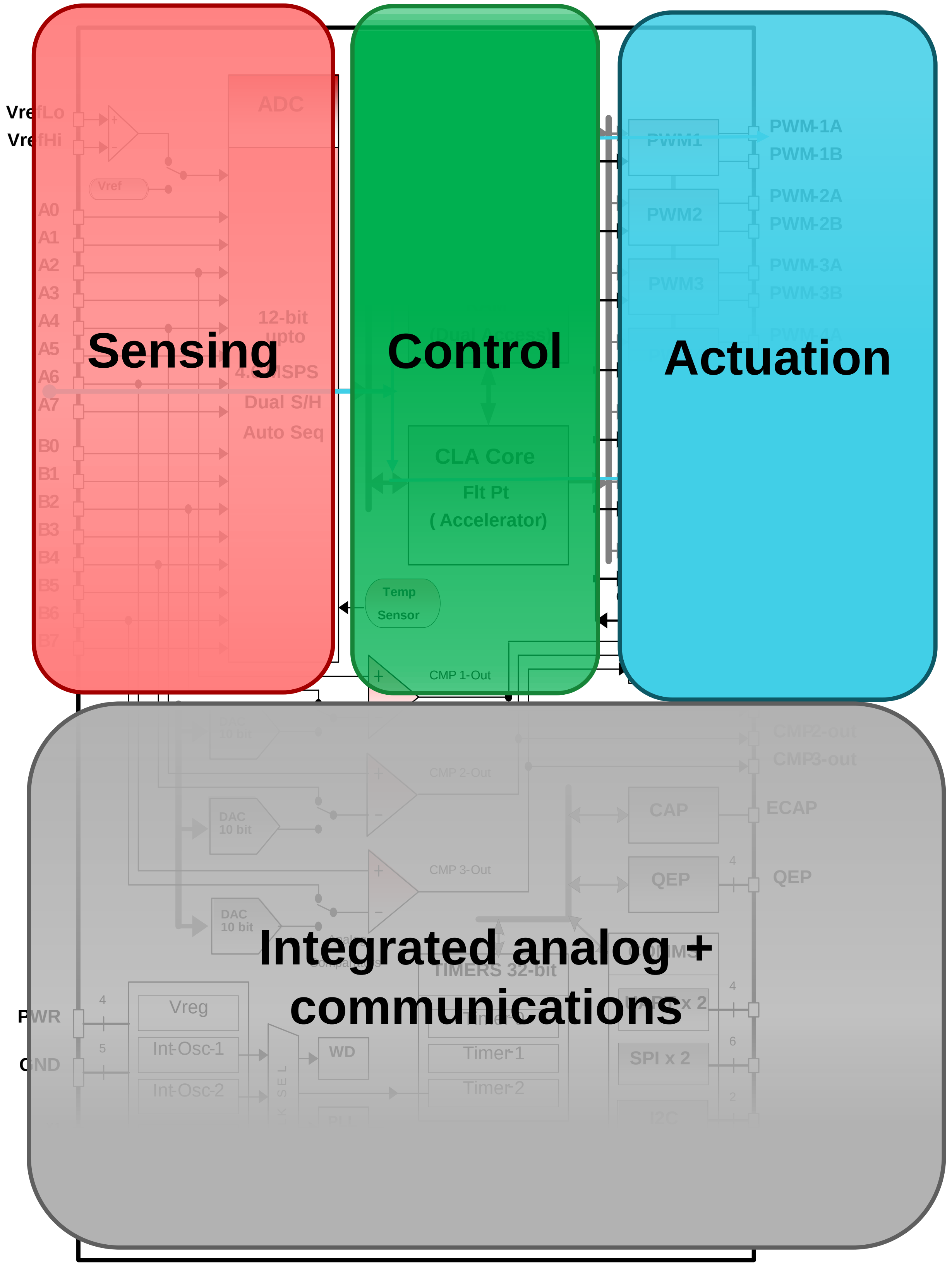
MANISH BHARDWAJ

SOLVING POWER EFFICIENCY AND INTEGRATION DESIGN CHALLENGES WITH C2000™ MCUs IN ON-BOARD CHARGERS

Outline

- Onboard charging (OBC) trends and C2000™ MCUs
- OBC PFC Converter
  - Single-phase totem-pole PFC design challenges
  - Three-phase PFC design challenges
- OBC DC/DC Converter
  - CLLLC design challenges
  - Dual Active Bridge (DAB) design challenges
- High voltage-to-low voltage(HV-LV) DC/DC Converter
  - Peak Current Mode Control (PCMC) to eliminate DC blocking capacitor
- Integration Trends : Single Microcontroller solution

C2000™ MCUs architected for power electronics



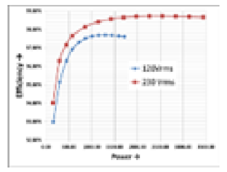
Leading real-time control performance

- High-performance C28x DSP core for math-intensive control algorithms
- Intelligent peripherals (PWMs & ADC) optimized over 20 years for control applications
- On-chip analog integration
- Robust software libraries (digital power / motor control)
- Extensive reference designs for OBC

C2000™ real-time MCUs address EV challenges

Power Density

- Higher switching frequencies
- Faster execution of the control loop (TMU, CLA)
- Advanced topologies



Efficiency

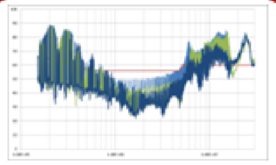
- GaN and SiC power devices
- Control techniques such as active synchronous rectification, without using external logic
- Comparator subsystem on chip and PWM features enable adaptive dead time and phase shedding

Time to Market

- Robust reference designs suite ranging from 3.3kW-22kW
- Quick prototyping with powerSUITE
- Measure loop bandwidth with SFRA

Cost

Multiple power stage control, CLA advanced topologies & control techniques



EMI

Meet CISPR 25 Class B
Use advanced techniques to reduce size of EMI filter

Safety

Broad portfolio of devices with Functional Safety-Certified devices, up to ASIL B

Bi-Directional Control

Emerging concepts such as V2G possible with TMU to accelerate grid synchronization (PLL) algorithms

C2000™ real-time MCU portfolio for OBC and DC/DC conversion applications

Future devices, lower cost, lower package

Device	PWM	ADC	MIPS
TMS320F280025	14	16	100
TMS320F280049	14	21	200
TMS320F280039	14	23	240
TMS320F28377D	24	24	800
TMS320F28388D	32	24	925

Future Devices, higher PWM channels, ADC channels, more compute

C2000™ real-time MCU reference designs

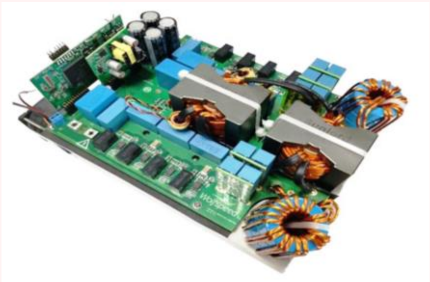
Bi-directional on-board chargers

22kW F2838x

6-Switch PFC
CRD-22AD12N [+]

F28377D

DC-DC CLLLC
CRD-22DD12N [+]



F28377D

[+] *Wolfspeed Designs*

11kW F2838x

Vienna/ T-Type PFC
TIDA-01606

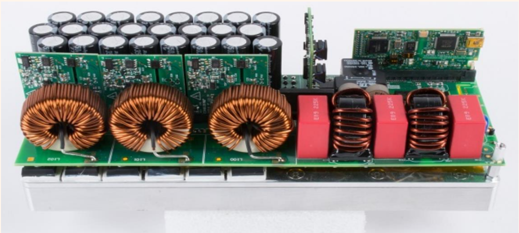
F28377D

DC-DC Dual Active Bridge (DAB)
TIDA-010054

F28377D

6-7kW F280049

Totem Pole PFC
TIDA-01604

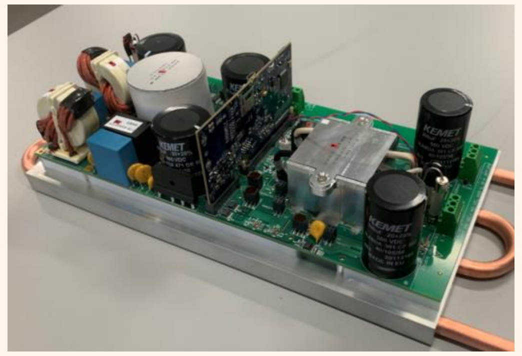


F280049

DC-DC using CLLLC
TIDM-02002

F280049

Single Controller, GaN based PMP22650



F28388D/F280039

Bi-directional HV-LV DC/DC

TIDM-02009 , DC-DC Section
400V-12V, 3.6kW DC/DC, PCMC

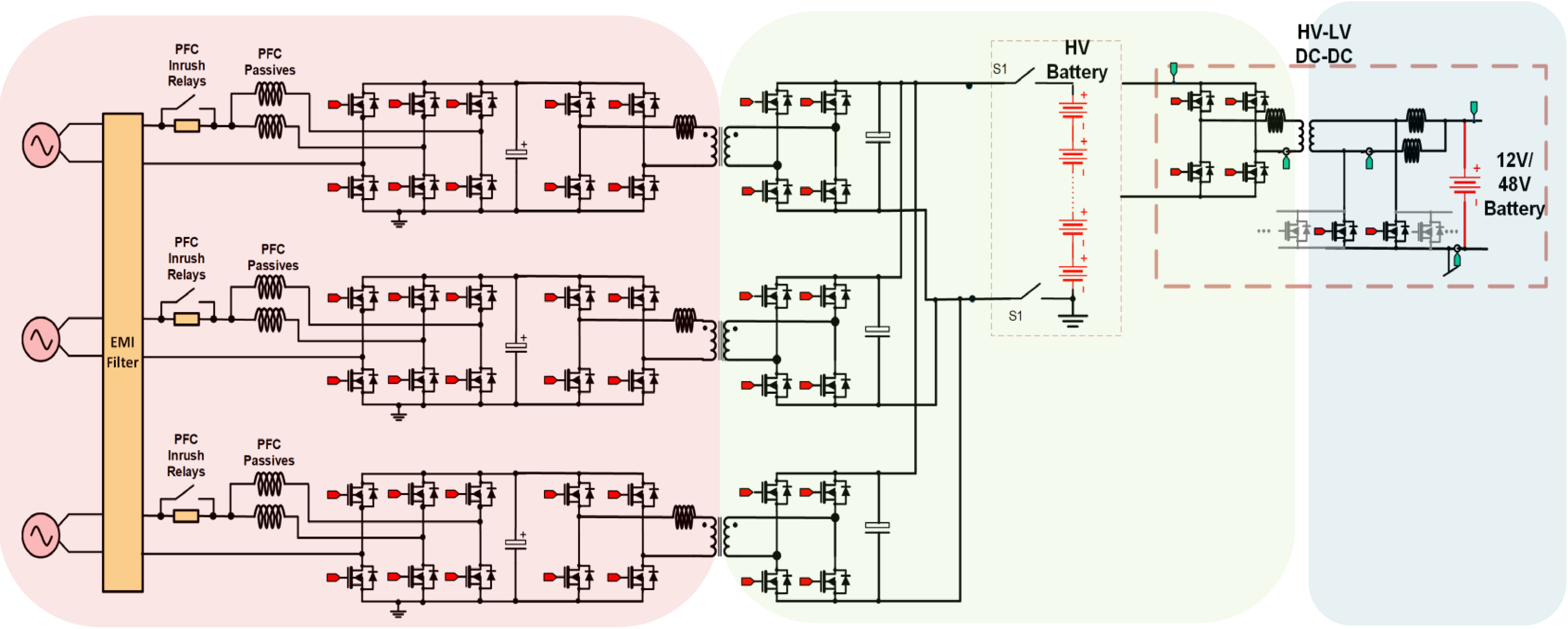
F28388D

3kW F280049

Software is available in **C2000Ware-DigitalPower-SDK** for TI reference designs

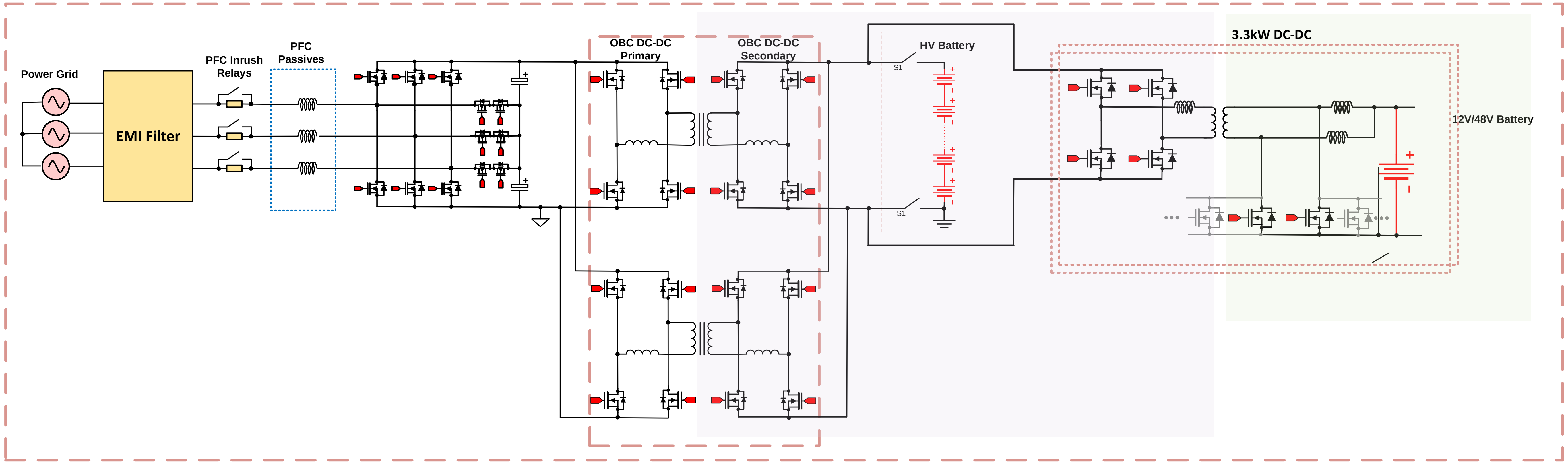
C2000™ MCUs for 22kW OBC (modular power stages)

C2000 MCU portfolio
F280024 to F2838xD address all the power levels and architectures



	OBC PFC	OBC DC-DC	HV-LV DC-DC
Lowest isolation cost	3 x F280025	3 x F280025	1 x F280025
Modular development	3 x F280049		1 x F280025
Integrated solution	F28388D		

C2000™ MCUs for 22kW OBC (non-modular power stages)



<u>C2000 MCU portfolio</u>
F280025 to F28388D
address all the power levels and architectures

	OBC PFC	OBC DC/DC	HV-LV DC/DC
Lowest isolation cost	F280049	F280049	F280049
Modular development	F28388D		F280049
Integrated solution	F28388D		

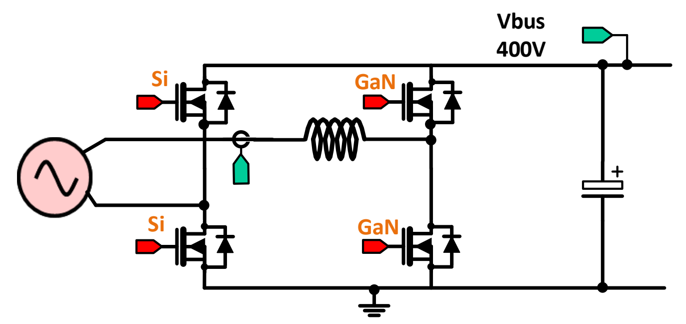
OBC PFC Converter

Single-phase PFC

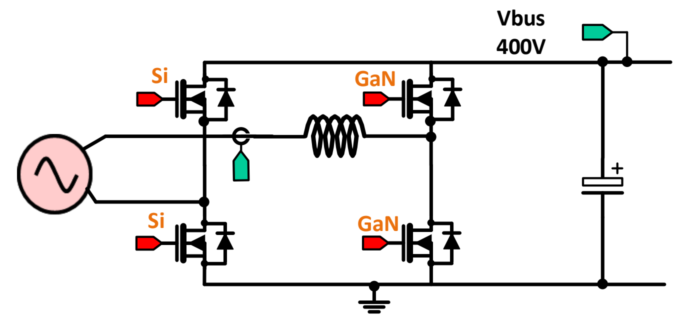
Three-phase PFC

PFC selection for 11 kW – 22 kW OBC

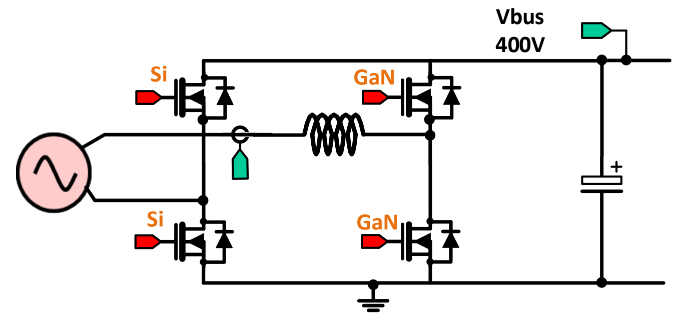
Modular power stage



Totempole PFC (3.3kW/ 6.6kW)

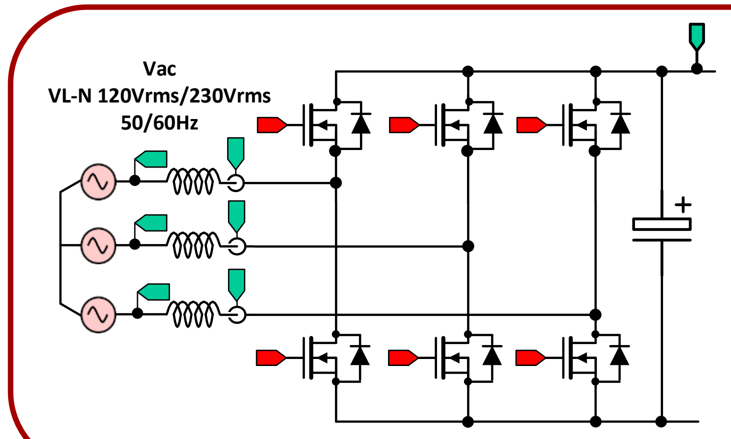


Totempole PFC (3.3kW/ 6.6KW)



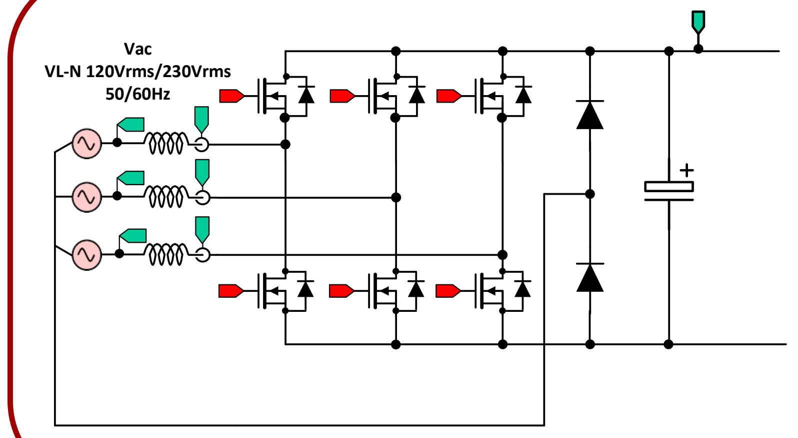
Totempole PFC (3.3kW/6.6kW)

6-switch PFC



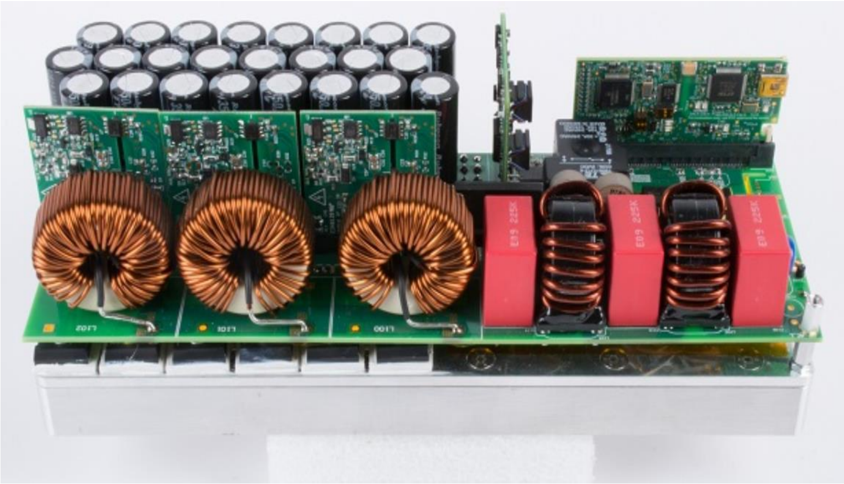
Power needs to be
de-rated 1/3rd
for Single Phase operation

6-Switch PFC with 4th leg



Bus Capacitor needs to sized properly to support full power flow

OBC 1-phase PFC design challenges



TIDA-01606

Time to Market

<u>Implement robust grid synchronization</u>

- Totem pole PFC requires accurate, noise-free grid angle information.
- **C2000™ MCU feature:** Trignometric Math Unit (TMU) helps accelerate the necessary SPLL computation

Cost

<u>Improving power factor using advanced control</u>

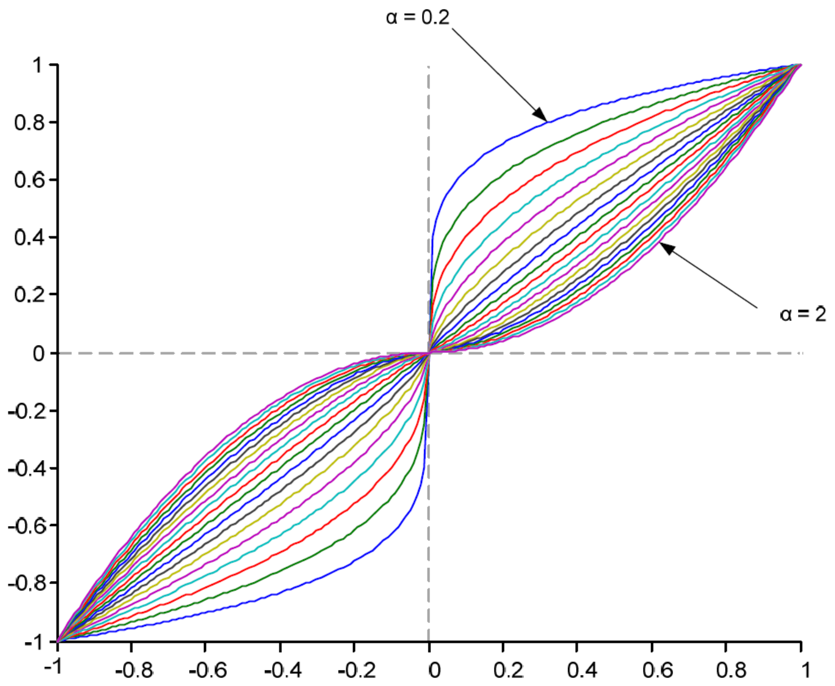
- Input capacitor causes degradation to the power factor. With advanced control such as DPLLVC, the error due to input capacitor can be offset to improve achieved power factor.
- **C2000 MCU feature**: 32-bit floating point unit simplifies control computation

Tackle tough control challenges with trignometric math unit

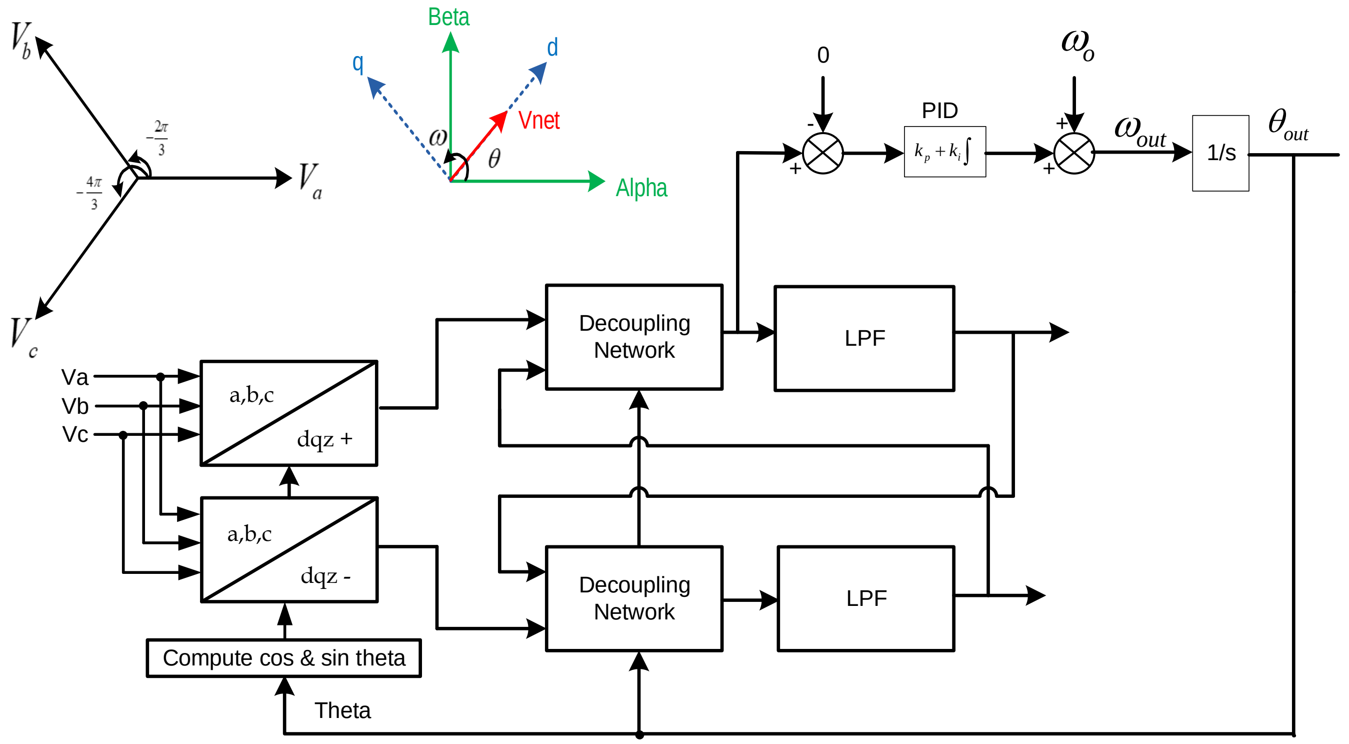
- Dedicated instruction set to accelerate sin, cos and other trignometric operations
- Achieve fast transient response with hardware acceleration of log, pow and exp math functions for challenging fast load switching applications

TMU Operation	Pipelined cycles
Sin	4
Cos	4
Atan	4
Divide by two Pi	2/3
Multiply by Two pi	2/3
Square root	5
Exponent (type1)	5
Log (Type1)	5

Fast transients using non-linear control (log, pow, exp)



Advanced control using sin, cos and atan acceleration

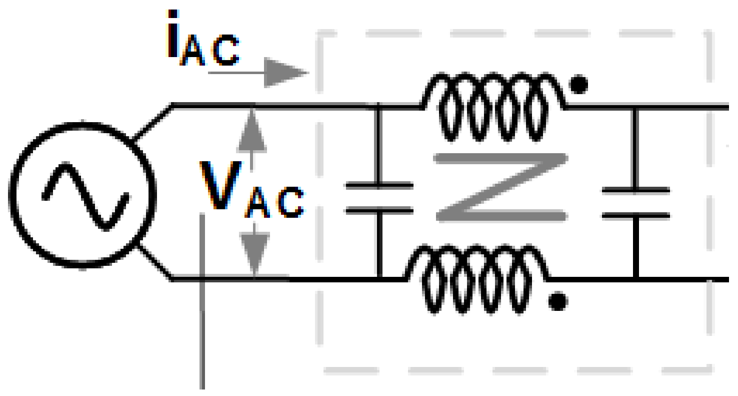


Run phase-locked loops 30% faster

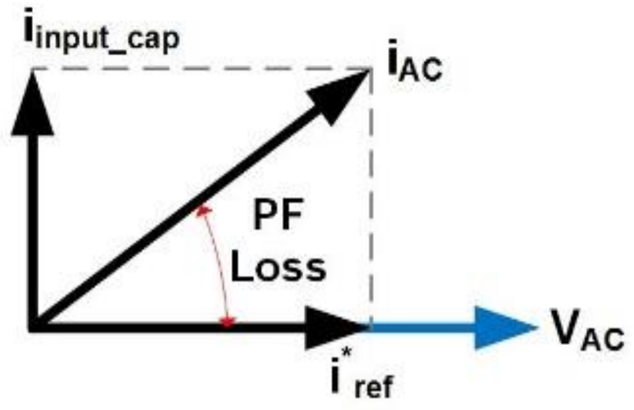
C28x FPU	C28x FPU + TMU
455	315

Totem pole PFC design challenge: improving power factor

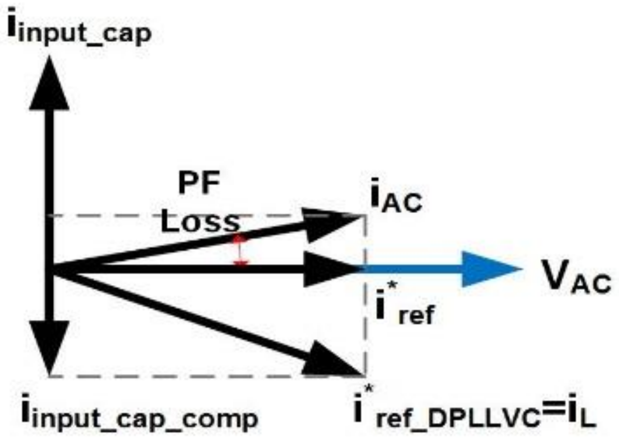
PFC input filter



Reactive power draw causes PF Loss



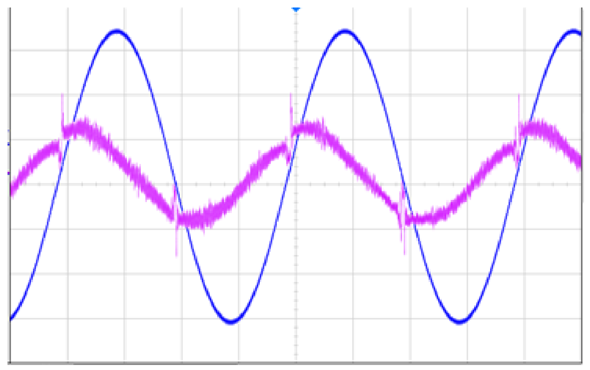
Reactive power draw offset by shifting the reference vector, need PLL computation for the grid angle



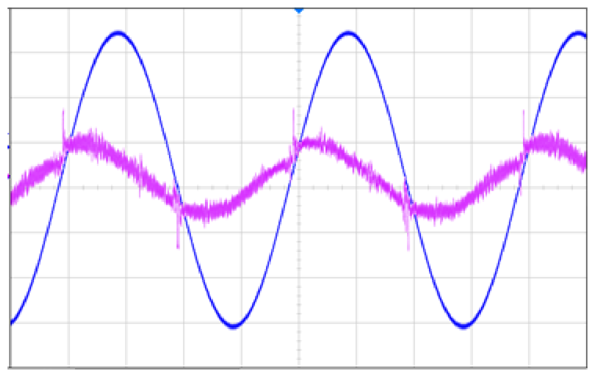
$$i^*_{ref\_DPLLVC} = i^*_{ref}\sin(\omega t) - i_{input\_cap\_comp}\cos(\omega t)$$

$$i_{AC} = i_{ref}\sin(\omega t) + (i_{input\_cap} - i_{input\_cap\_comp})\cos(\omega t)$$

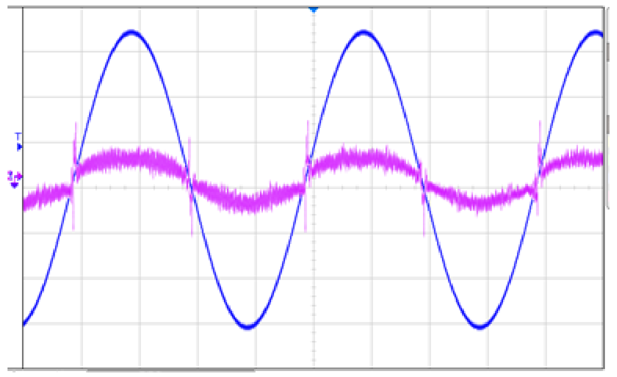
Results



No Adjustment Applied

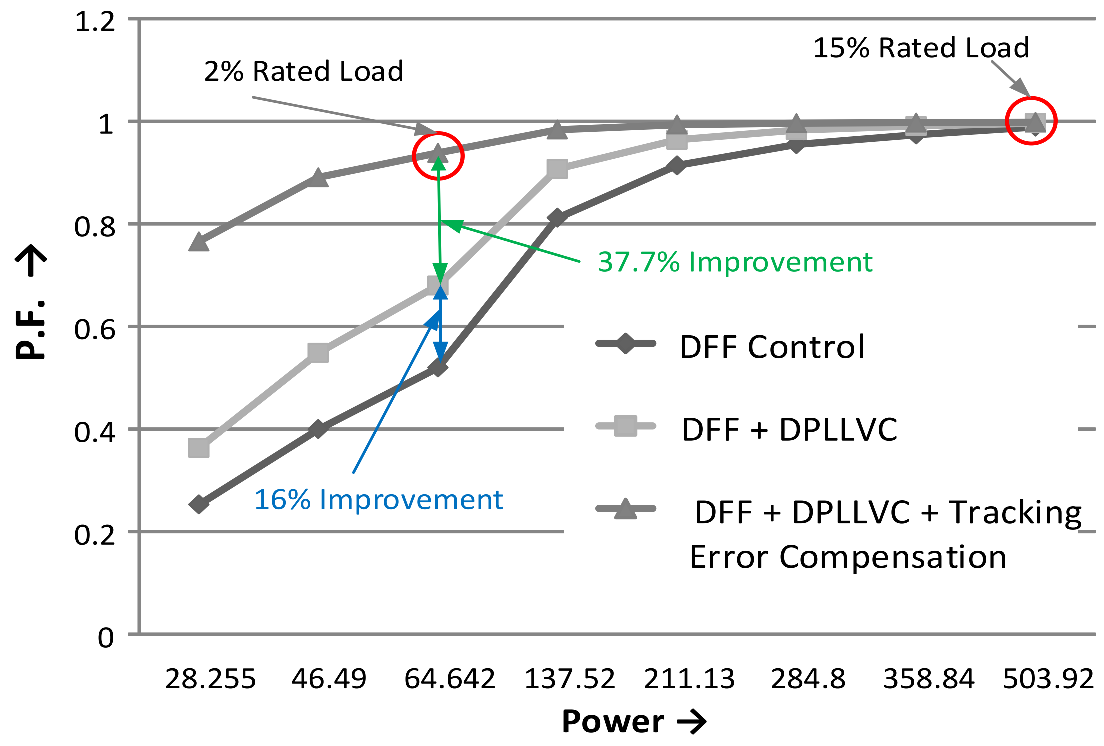


With DPLLVC

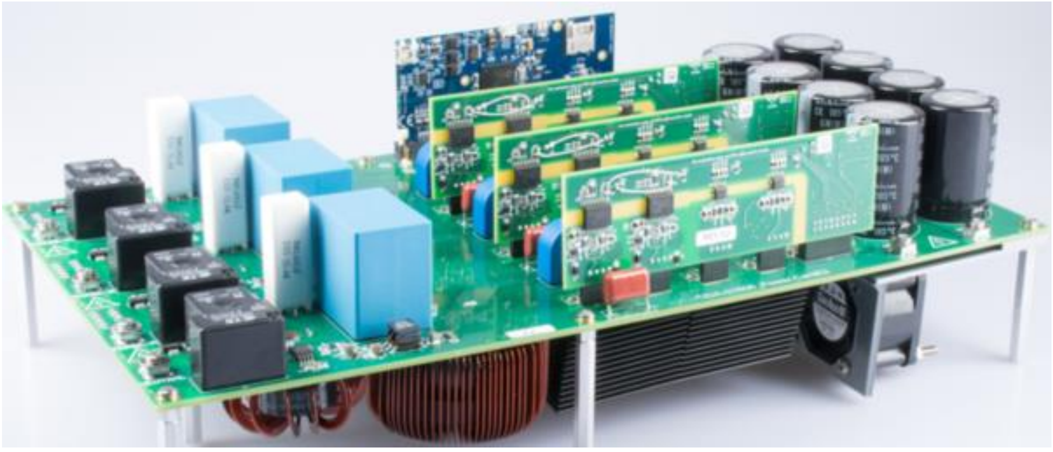


With DPLLVC + TC

Test waveforms: Voltage(blue) and Current(pink)
Test condition: Vin=230vrms, P_{out}=64.80W.



OBC 3ph PFC design challenges



TIDA-010039

$ Cost

Implement Protection for phase currents

- Multiple comparators (up to 6) and references using DACs (up to 2) needed to implement protection
- **C2000™ MCU feature:** Comparator Sub System enables adding protection without any external circuity

Time to Market

Measure loop bandwidth for DQ-based systems

- Conventional tools cannot be used to measure control loop performance for DQ based control as no physical control variable exists on the board.
- **C2000 MCU feature:** Software Frequency Response Analyzer enables measuring loop response which eases system design and test

Run Phase Locked Loops for Grid Angle Detection Faster

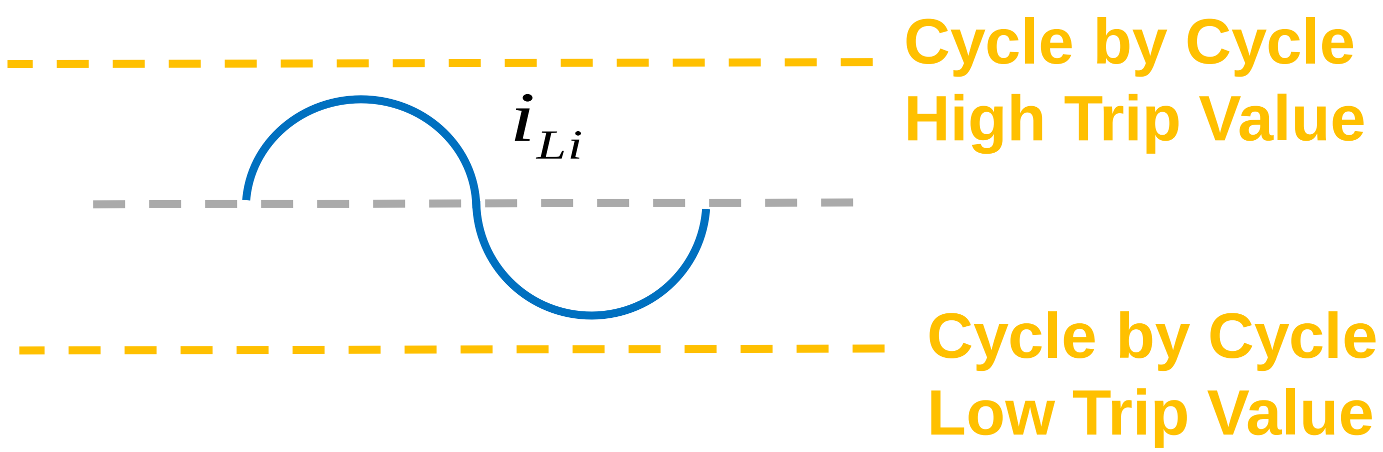
- Accurate estimate of the grid voltage using PLL allows more noise immunity and less distortion
- **C2000 MCU feature**: Trigonometric Math Unit (TMU) runs trigonometric operations faster which accelerates PLL computation and enables better performance

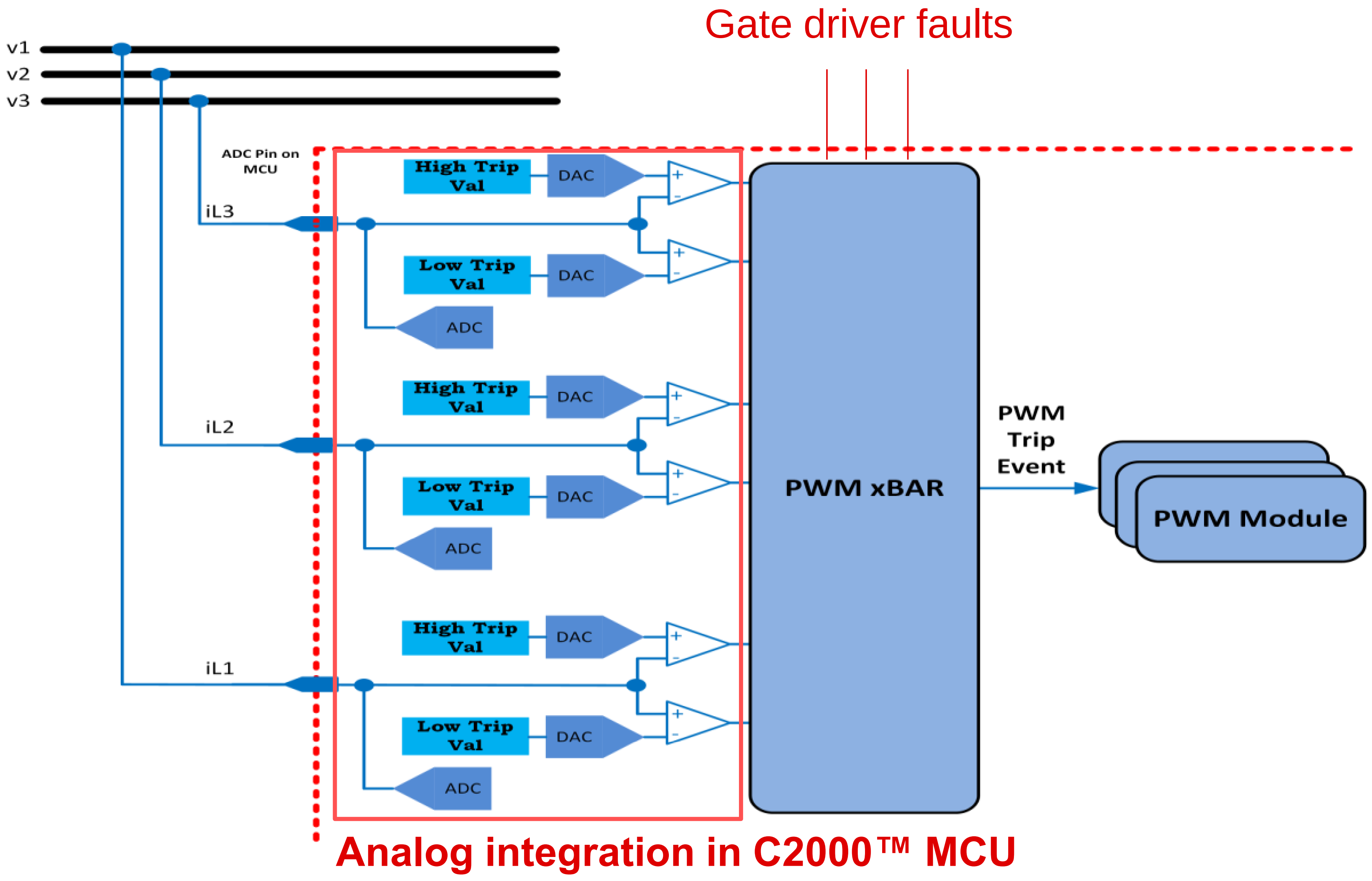
Advanced protection implementation

- Integrated comparator subsystem (CMPSS) enables protection *without any extra components on the board or extra pins on the device.*

- xBAR-type mechanism combines comparisons of three current inputs and generates signals for PWM tripping

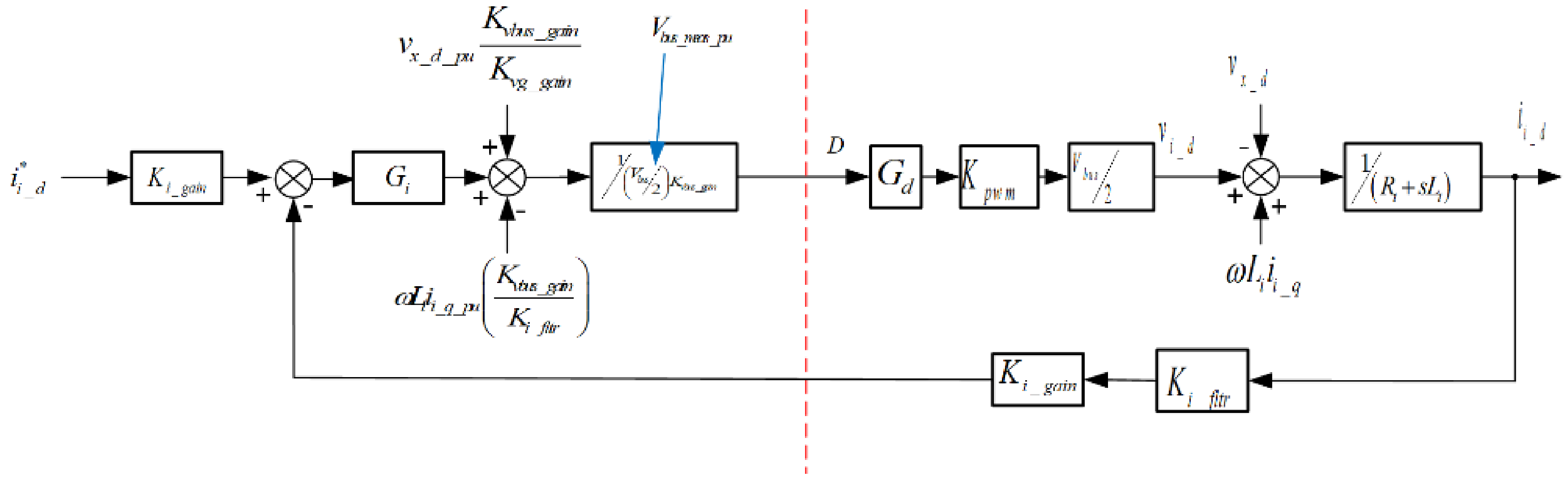
- Additional trips can be managed, such as gate driver faults, via INPUTXBAR



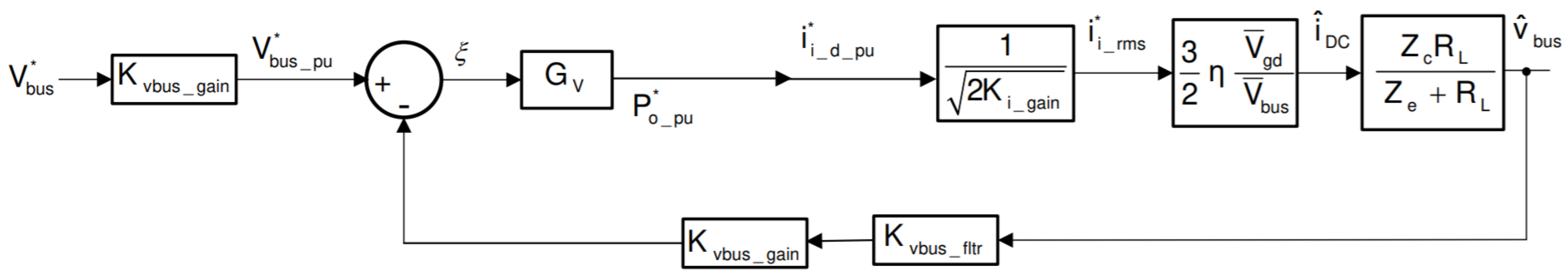


Software Frequency Response Analyzer(SFRA) for measuring the control loop performance

Current loop model

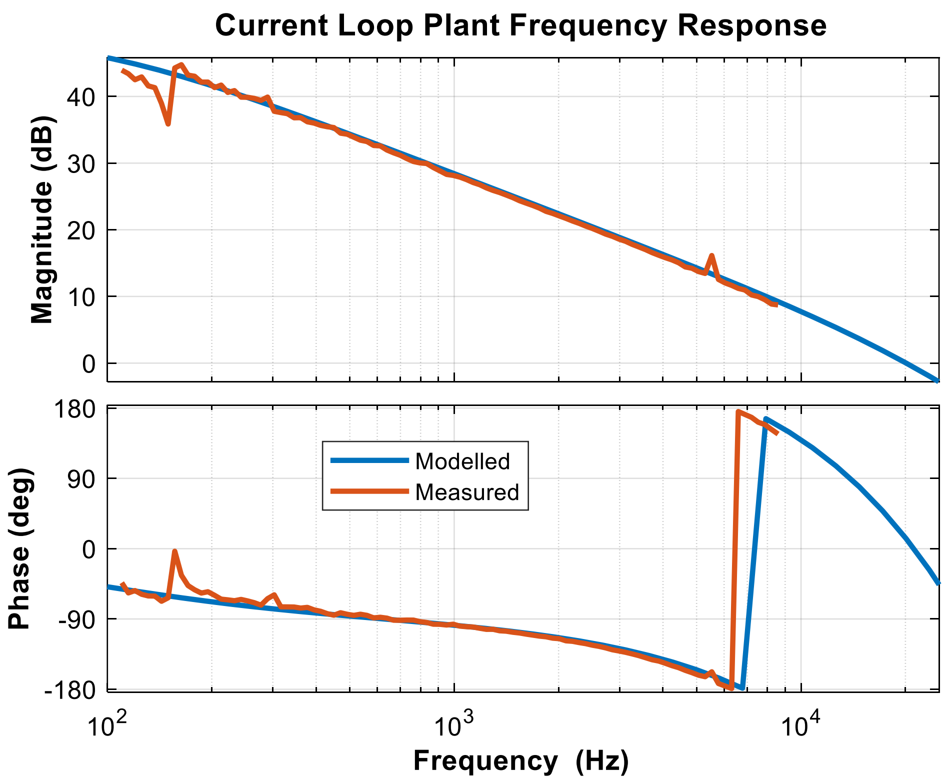


Voltage loop model



TIDA-01606, Vbus 800 V, Vac 230 startup waveform

Measured SFRA comparison to mon TIDA-01606



OBC DC/DC Converter

CLLLC

DAB

OBC and DC/DC conversion design challenges


TIDM-02002

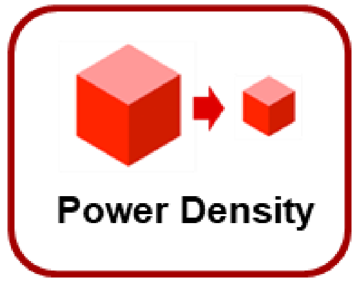
Implement synchronous rectification which an save up-to 2% in power losses but is challenging to implement

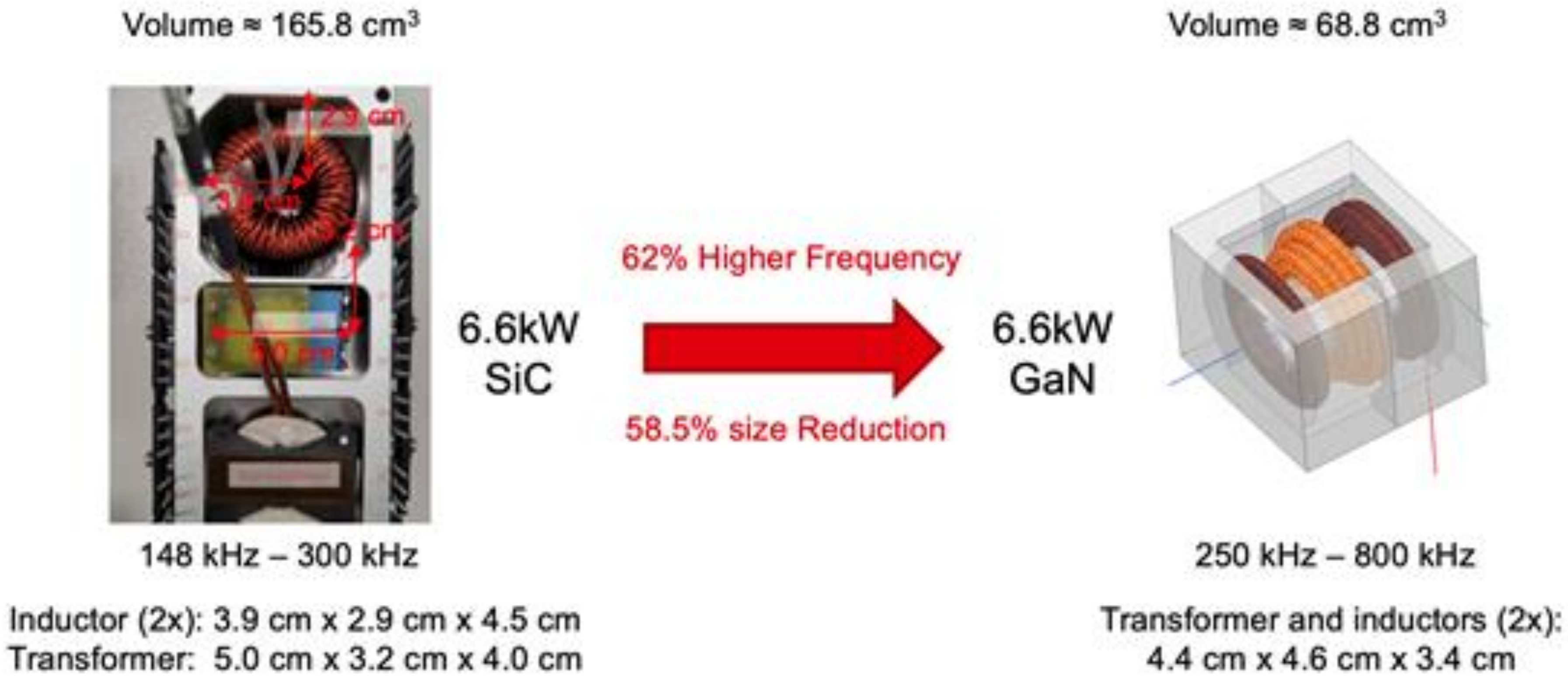
- 120 W of power losses at 6.6 kW
- 220 W of power losses at 11 kW

- **C2000™ MCU feature:** Implement robust synchronous rectification scheme with no external logic required
  - Reduce heat sink requirements
  - Improve power efficiency
  - Improve power density

User High PWM Switching to Reduce Size

- Higher switching frequency helps reduce magnetics by up-to 60%
- **C2000 MCU feature:** Control high-resolution phase shift, frequency, dead-band and duty for accurate control.
  - PWM features such as global link and load reduce CPU loading as PWM frequencies are increased and multiple bridges are updated

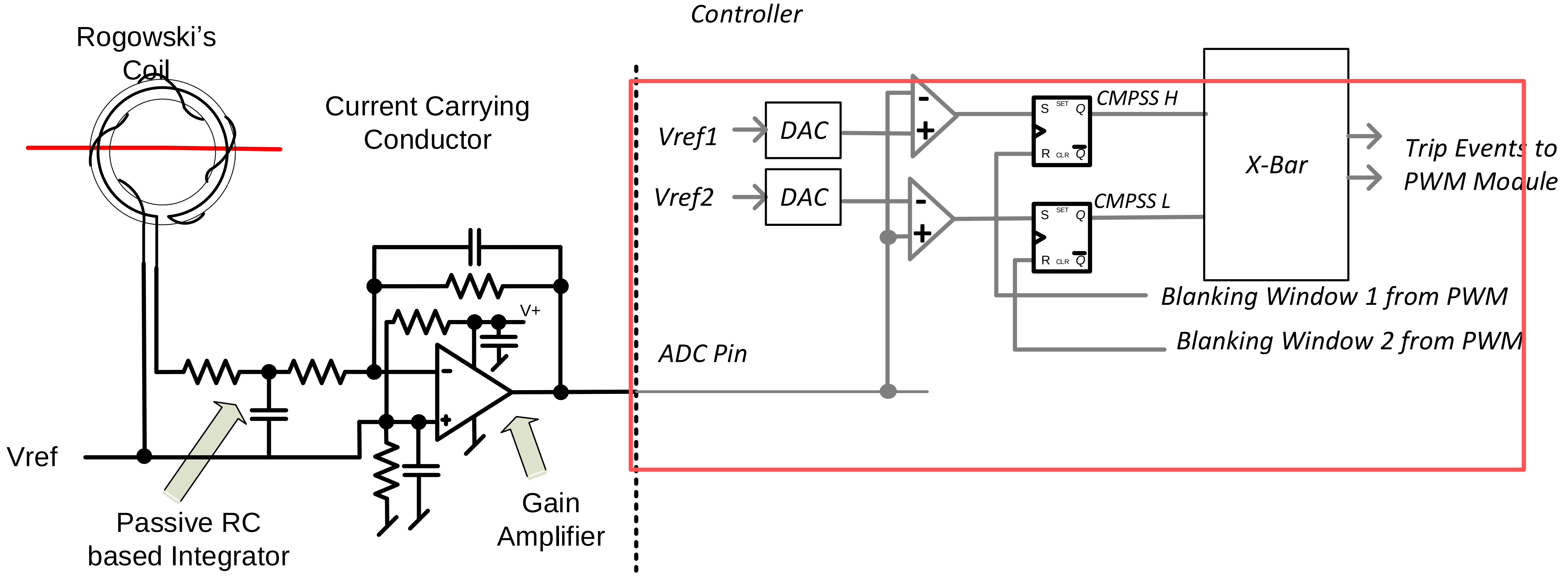




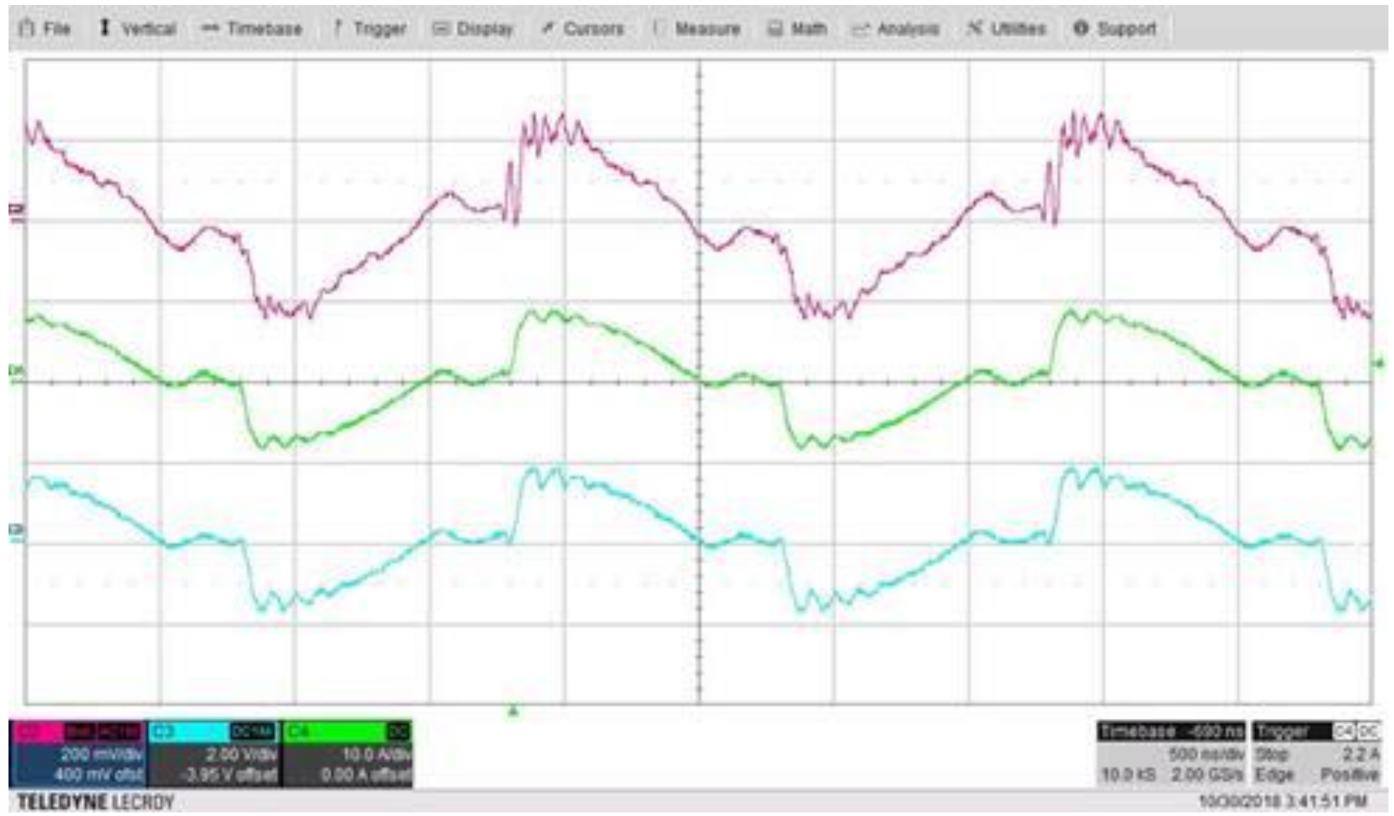
Synchronous rectification implementation for CLLLC

- Sensing high frequency current improves efficiency up to 2%.
- A high-frequency Rogowski's coil can be used to sense currents up to 2-3 MHz per signal.
- Integrated C2000™ PWM module and connection to CMPSSS enable accurate he synchronous rectifier switches using PWM features such as blanking window to add robustness from noise and inserting dead time before a trip.
- C2000 MCUs allow implementation of this scheme without external logic, references, DAC and comparators, and enables programmability to optimize turn on to account for sensor delays.

Analog integration in C2000 MCU



CH2: Amplifier output designed Rogowski's coil,
CH3: Off the shelf Rogowski coil probe measurement,
CH4: Current probe measurement



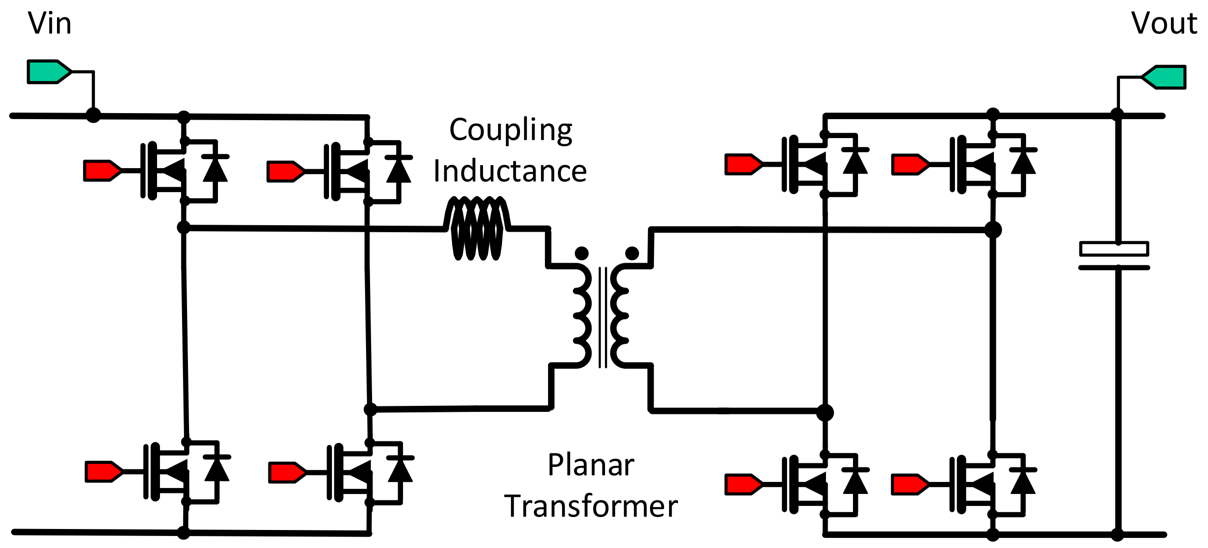
400Vin, 251.616V/3.425A output, 500kHz

High-resolution phase shift control in dual active bridge

- Power transfer in single phase shift DAB is related to the coupling inductance (L) value, switching frequency (Fs) and the phase (θ)
- Output capacitor C_L required for a desired voltage ripple is dependent on the switching frequency, inductance and phase shift
- Switching frequency of 100 kHz and a leakage inductor of 35 uH improves power density
- High-resolution phase shift enables high power density and efficiency and enables DAB topologies

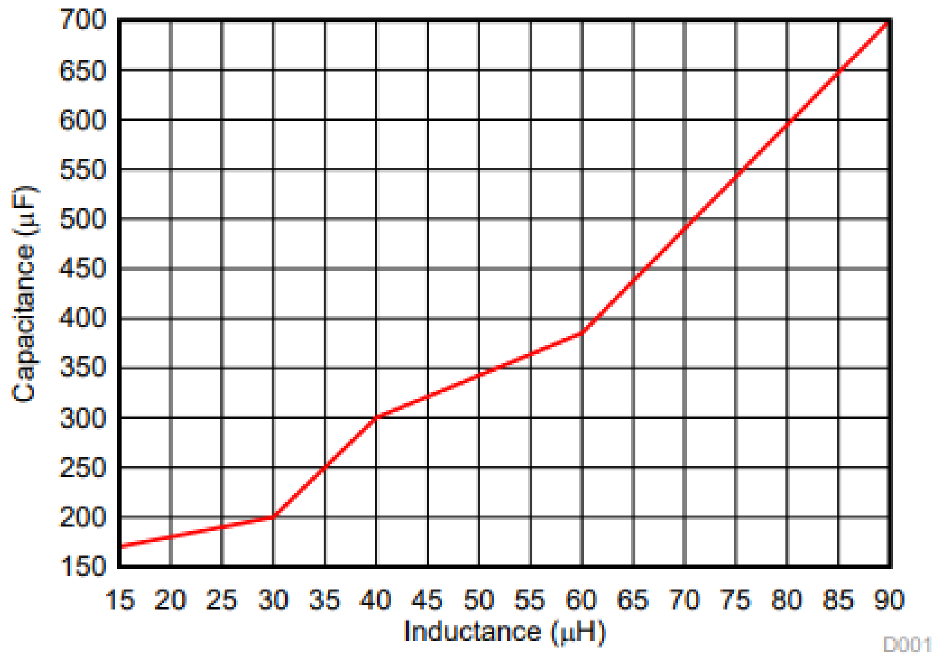
$$P_{output} = \frac{nV_{in}V_{out}\theta(\pi-\theta)}{2\pi^2F_sL}$$

$$\theta = \frac{\pi}{2}\left[1-\sqrt{\left(1-\frac{8F_sLP_{out}}{nV_{in}V_{out}}\right)}\right]$$



Vin= 800 V, Pout = 10000 W, Fs= 100 kHz	Vout	Nanosecond of phase shift needed
Ø = 29.4169 Degrees	400	817.14
Ø = 29.2353 Degrees	402	812.09
Ø = 29.0560 Degrees	404	807.11
Ø = 28.879 Degrees	406	802.19
Ø = 28.7042 Degrees	408	797.34

Output cap required for a given ripple vs coupling inductor



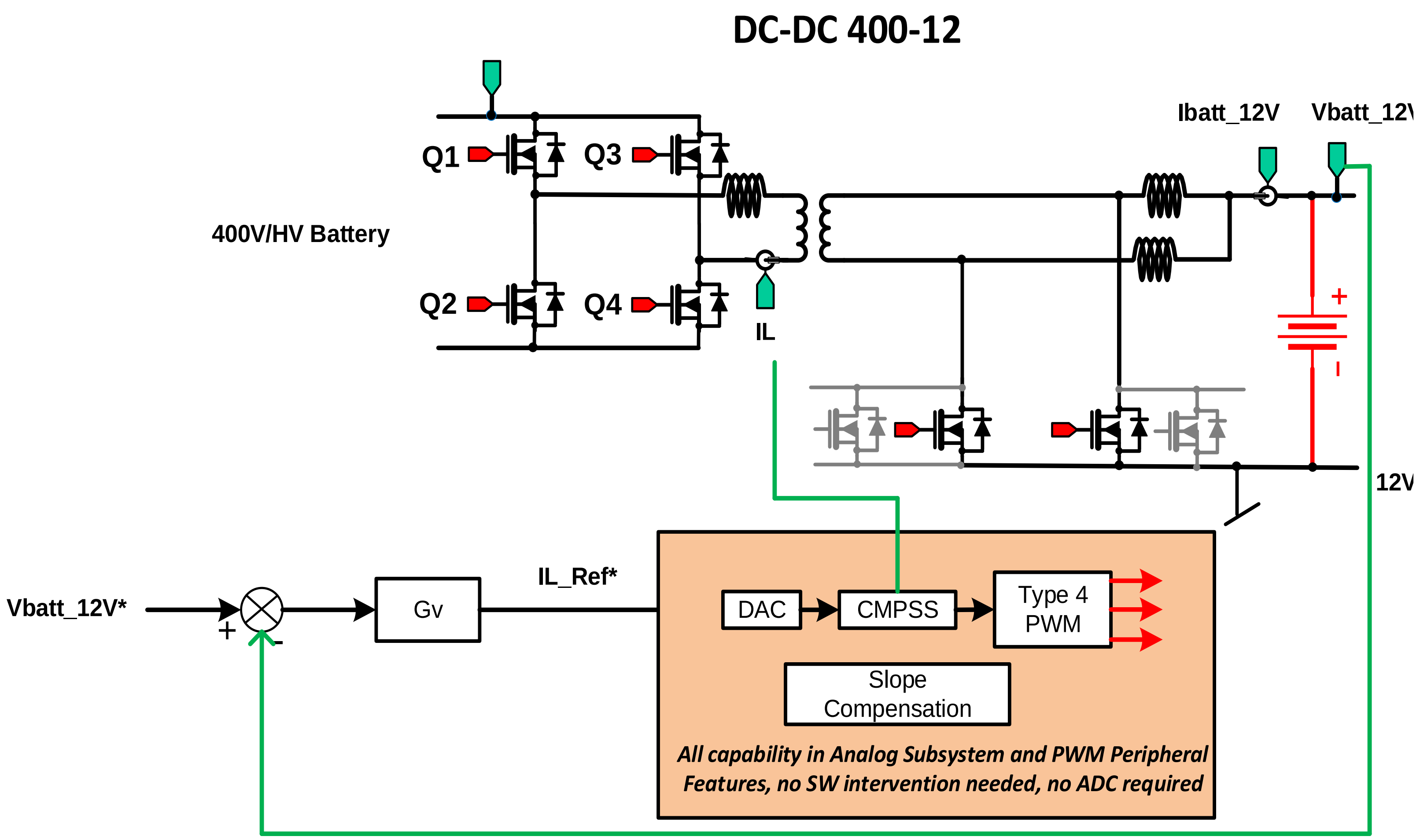
High voltage-to-low voltage DC/DC (HV-LV DC/DC) Converter

HV-LV DC/DC converter design challenge

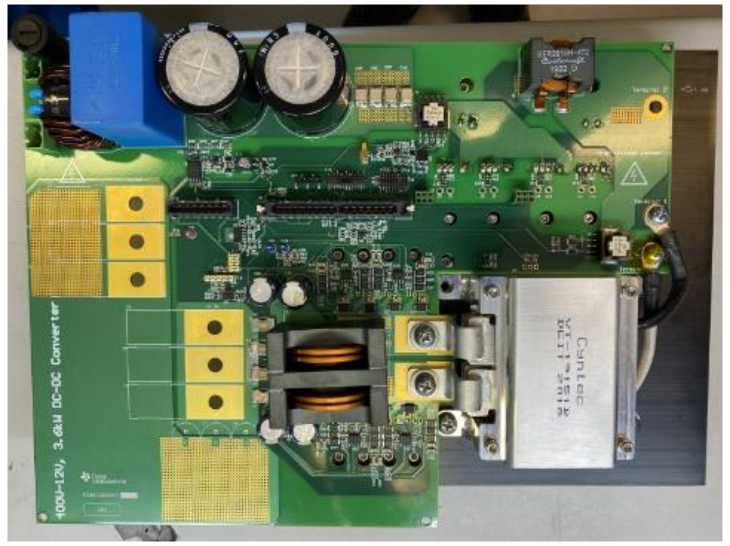
PSFB is a commonly used topology for HV-LV DC-DC stage. If average current of voltage mode control used a DC-blocking capacitor is required but not preferred because:

- It must be rated for the high frequency current it will carry
- It must be non-polarized
- It must be rated for the worst case voltage that can appear across it
- It causes the circulating current to decay more quickly during the freewheeling interval (Toff) than it would if the voltage were zero
- It reduces the energy available to drive the ZVS transition at the start of the next cycle (QA and QB, or PA leg) and makes ZVS operation more difficult

Peak Current Mode Control (PCMC) for PSFB is thus commonly used to eliminates the need for DC-blocking capacitor. For this the inner current loop needs to run in a purely analog fashion. C2000 Real-time MCUs with advanced analog integration enable this to be run with a digital MCU, giving designer the best of both an analog and digital solution.



TIDM-02009 DC-DC

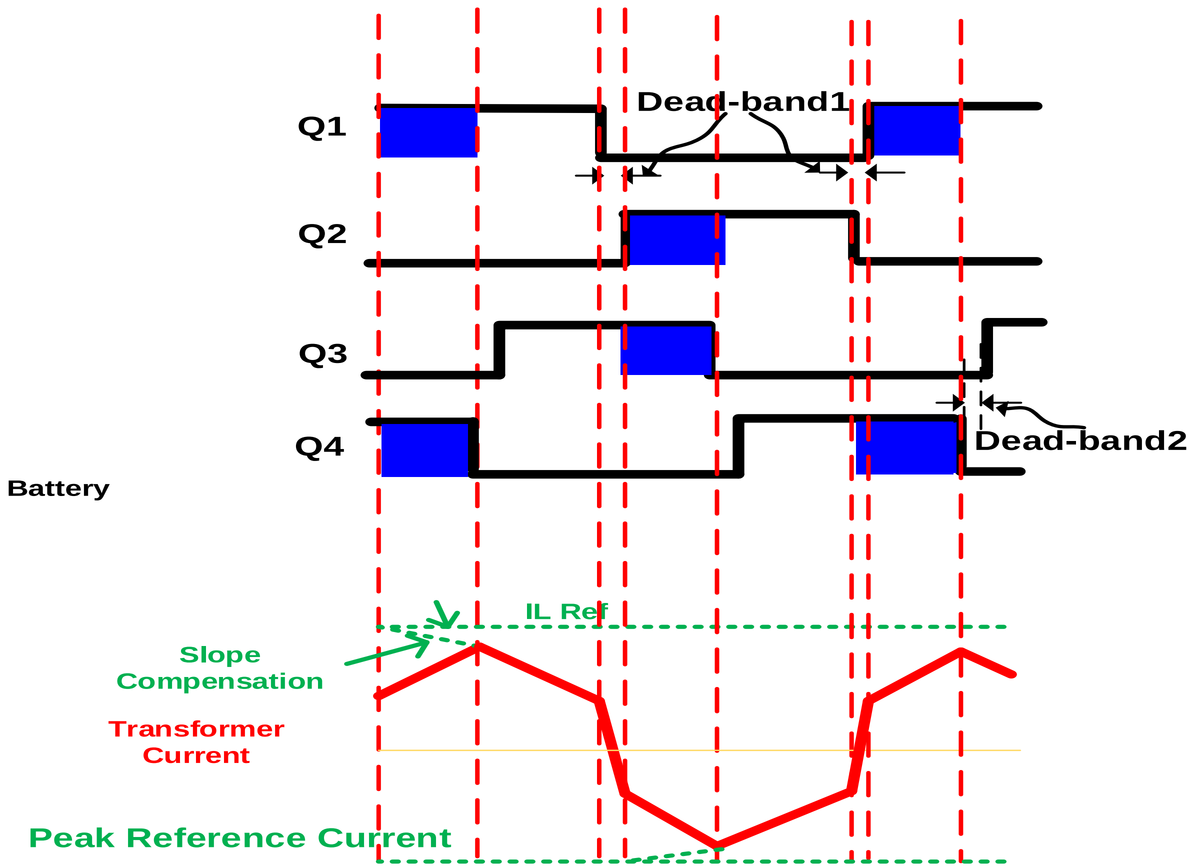


C2000™ MCU solution for PCMC

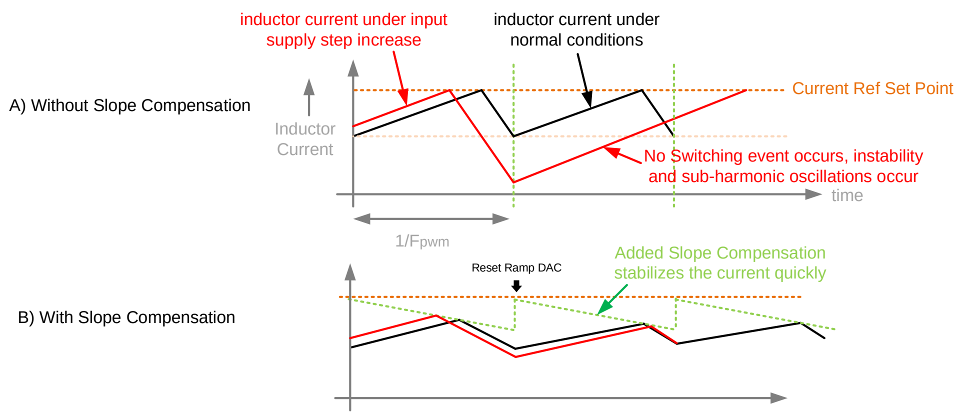
- Peak current mode control (PCMC) requires slope compensation to avoid sub-harmonic oscillations
- Comparator subsystem with ramp generation capability for the internal DAC enables implementing the inner current loop without any software
- Type 4 PWM allows insertion of dead-time after comparator events which allows optimization of deadtime with load

	Requirements
PSFB Peak current mode control	Switching frequency: 100 kHz Control frequency: 100 kHz MIPS: 30 ADC: 5-6, PWM: 6, CMPSS: 3 **TIDM-02002 (F280049)** **TIDM-02009 – DC-DC (F28388)**

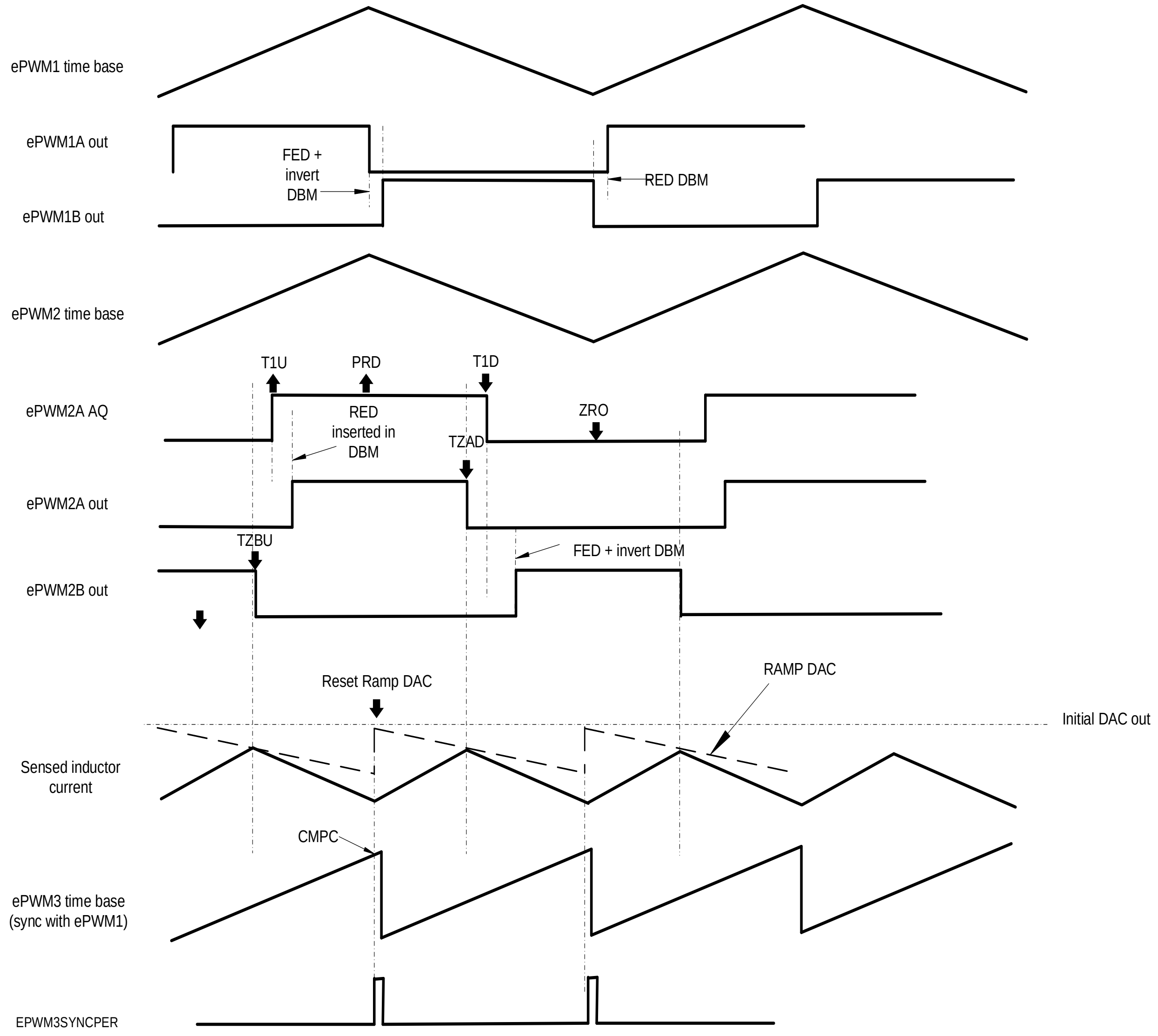
PSFB with PCMC



Slope compensation needed in PCMC



Implementation with Type-4 PWM for PSFB



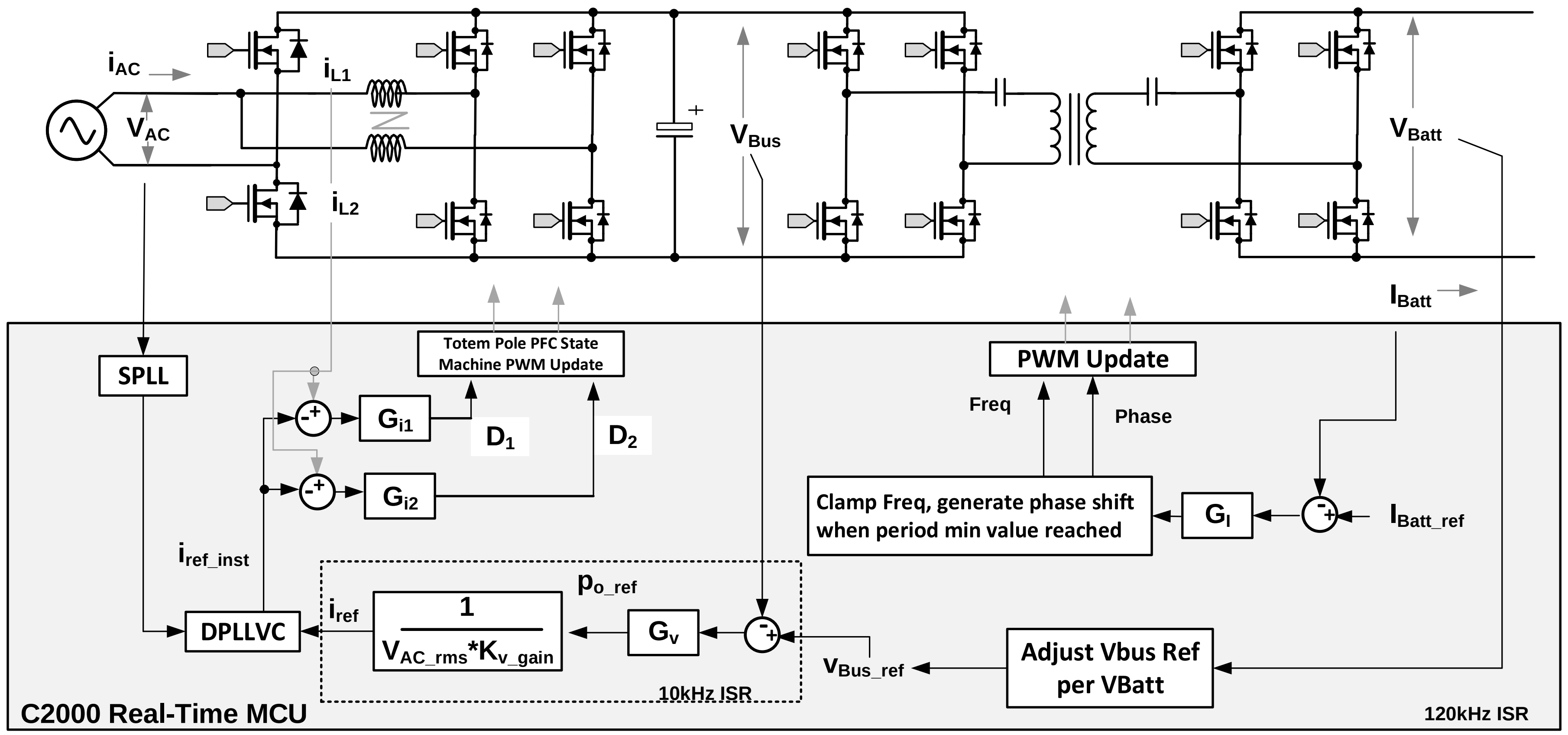
Integration challenges: Single microcontroller solutions

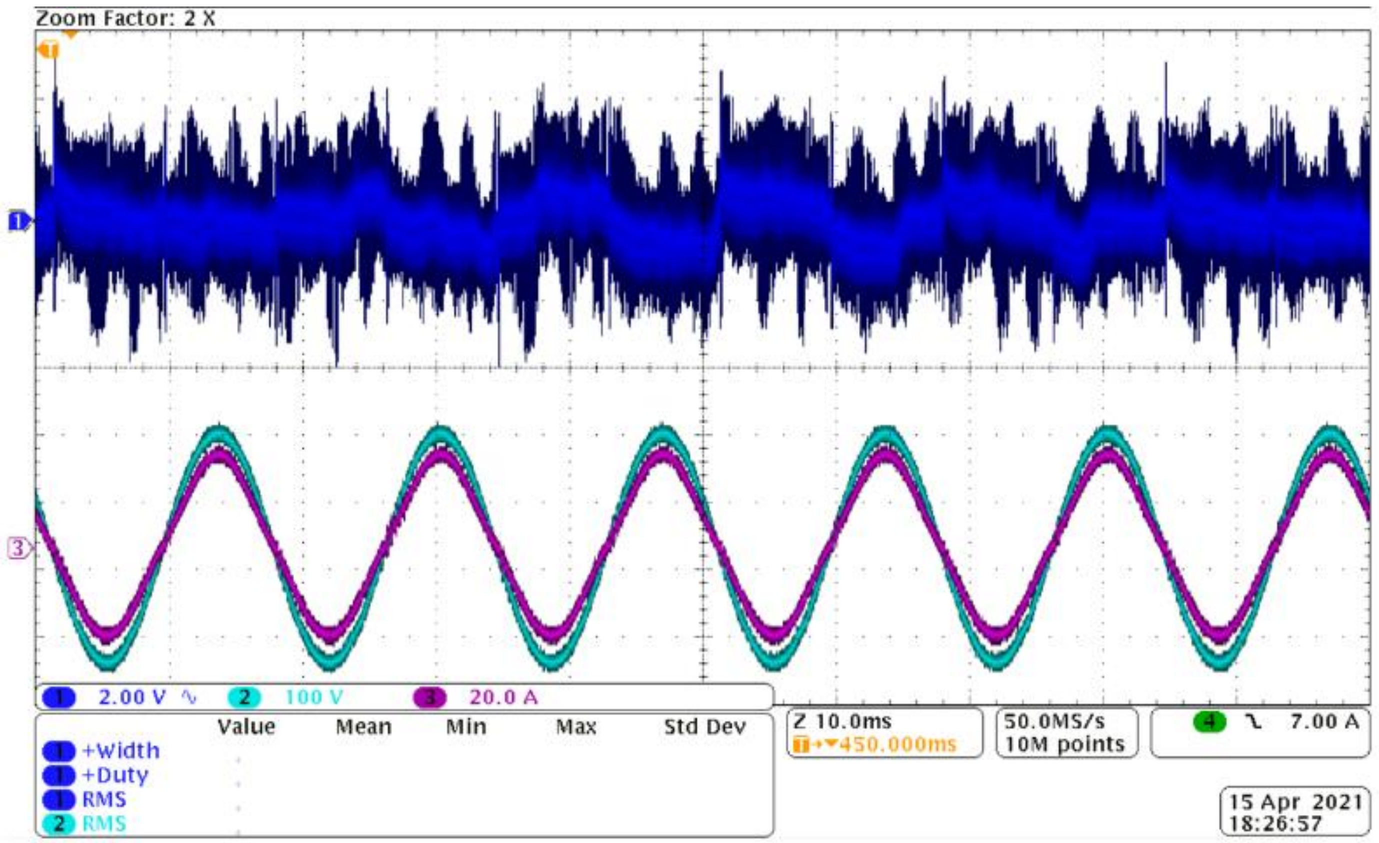
Single microcontroller-based OBC with TI-GaN FETs

MCU Usage

- **RAM:** 20 kB
- **Flash:** 40 kB
- **MIPS:** 170 for control
- ISR1 120kHz Sync to PWM : Fast PWM update (6-7 MIPS)
- ISR2 120kHz : PFC Current Loop + CLLLC Control Code (146 MIPS)
- ISR3 10kHz: PFC Voltage loop, Instrumentation (16 MIPS)
- **ADC channels:** 14
- **PWMs:** 14
- **GPIOs:** 32 (SFRA SCI 2, CAN 2, LED 2, **Ga**N Telemetry 19, Inrush relay 1)

Current device used: F28388, can be ported to F28004x

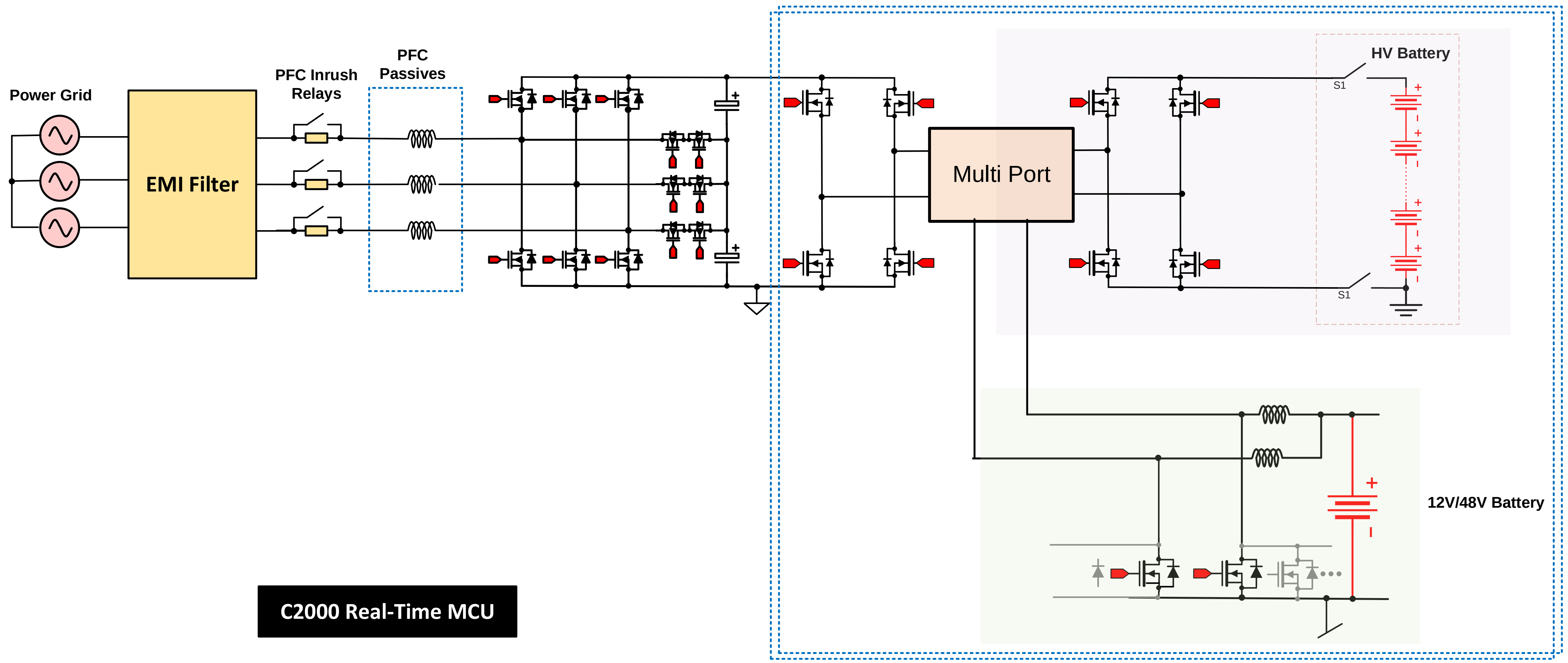




Vac 120Vrms, 50Hz
Vbatt 350V
Pload 2kW

Power Stage Integration

- Power stage integration between OBC and HV-LV DC-DC can enable cost savings.
- Further control of HV-LV DC-DC and OBC DC-DC can be done on a single MCU to save cost and simplify the design.
- C20000 MCUs broad portfolio of devices allow users to split the system in multiple different ways to achieve the desired integration.



Resources

- **Achieving High Efficiency and Enabling Integration in EV Powertrain Subsystems Using C2000™ Real-Time MCUs** , Whitepaper
- **PMP22650, GaN Based OBC Reference Design**
- **TIDM-02008/1007,** "Bidirectional Interleaved CCM Totem Pole Bridgeless PFC Reference Design Using C2000™ MCU." TIDM-1007/02008 User Guide." Texas Instruments user guide, literature No. TIDUD61D.
- **TIDM-02002,** "Bidirectional CLLLC Resonant Dual Active Bridge (DAB) Reference Design for HEV/EV Onboard Charger."
- **TIDM-02000,** "Peak Current Mode Controlled Phase-Shifted Full-Bridge Reference Design Using C2000 Real-Time MCU." Texas Instruments reference design No. TIDM-02000. Accessed Oct. 26, 2020.
- **TIDA-01606**, Texas Instruments. n.d. "Three-Level, Three-Phase SiC AC-to-DC Converter Reference Design." Texas Instruments reference design No. TIDA-010039. Accessed Oct. 26, 2020.
- DIGITAL POWER SDK
- Essential Guide for Developing with C2000 Real Time MCUs

TEXAS INSTRUMENTS