Breaking down accuracy errors in a precision high-speed ADC signal chain

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Introduction

Data converters, amplifiers, professional athletes—they all have accuracy errors. As it relates to electronics, however, an accuracy error is the sum of numerous fluctuations that move the DC conditions within each part in a signal chain. These errors can eat up the useful signal dynamic range of the system in different ways.

This article examines error-producing conditions in the signal chain where the fully differential amplifier (FDA) meets the high-speed analog-to-digital (ADC) converter in a receiver system.

Signal-chain overview and resistor errors

Figure 1 gives an overview of the signal-chain subset. Here, the analog input signal connects to the primary of the balun, which converts the input signal to a differential signal. In this example, the FDA gains up the signal by 4 or 12 dB; the signal then moves through a matching network to eventually interface to the high-speed ADC for sampling of the analog signal.

Table 1 separates the high-level signal-chain specifications in a spreadsheet, a good starting point for keeping all of the specifications in order.

For the following analysis, assume that there are no errors associated with the balun. See References 7 through 9 for descriptions of balun and transformer nuances.

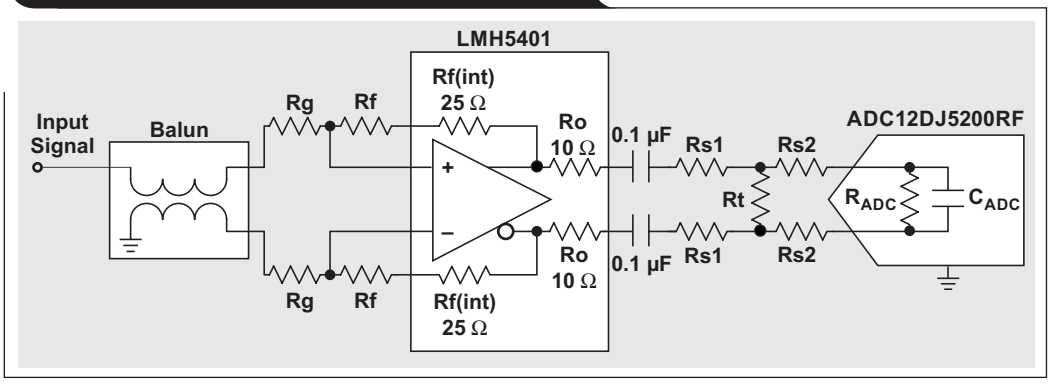
Table 1. Signal-chain specifications

Overall Signal Chain Specifications	Value	Unit
Input Signal	0.3	V
Temp. Range (–40 to +85°C) ⇒ 1 = 26°C at Room Temp.	1	
Kelvin (Room Temp.)	299.15	K
Boltzmann's Constant	13.8×10^{-24}	W-s/K
LDO Reg Line Regulation	0.05	%/V
ADC Supply Voltage-VA19	1.9	V
ADC Supply Voltage-VA11	1.1	V
ADC Supply Voltage-VD11	1.1	V
DIFF Amp Supply Voltage	5	V
BW	1	GHz
Noise BW—1st Order System	1.57	GHz
Noise BW—2nd Order System	1.22	GHz

There are three significant contributors to resistor errors:

- Resistor tolerance (R_{tol}) is the value tolerance, usually specified in percent.
- Resistor temperature coefficient (R_{tempco}) is the value's drift, usually specified in parts per million per degrees Celsius.
- Resistor life (R_{life}) or qualification is the value's drift over thousands of hours, usually specified in percent.

Figure 1. Subset of a receiver signal chain



For example, a simple 50-Ω resistor with a 5% tolerance, 1,000 ppm/°C over a –40°C to +85°C temperature range (125°) and a life drift of 2% over 1,000 hours would yield a resistance error of ±9.75 Ω.

Or, using Equation 1, where the total resistor tolerance is equal to:

$$R_{value} \pm (R_{tol} + R_{tempco} + R_{life}) \quad (1)$$

Therefore,

$$\begin{aligned} \text{Total Tolerance} &= R_{value} \pm \left(\frac{R_{tol}}{100} \times R_{value} \right) \\ &+ \left[\left(\frac{R_{tempco}}{10^6} \times \text{TempRange} \right) \times R_{value} \right] \\ &+ \left(\frac{R_{life}}{100} \times R_{value} \right) \\ &= 50 \pm (2.5 + 6.25 + 1) \\ &= 40.25\ \Omega \text{ to } 59.75\ \Omega \end{aligned} \quad (2)$$

Initially, 40.25 Ω to 59.75 Ω looks like a big range of resistance variability, especially for a 50-Ω resistor. However, this is over the resistor's entire temperature range and life. For simplicity, it is best to understand the tolerance at room temperature, or 25°C; in this case, setting the TempRange = 1 in the example. This setting tightens up the resistor's error range, yielding 46.45 Ω to 53.55 Ω, which is a bit more realistic for a lab setting. Tighter tolerance resistors can also have a dramatic effect in cleaning up the error range as well.

Table 2 captures all of the resistor values in the spreadsheet and organizes them neatly. Eventually, the errors and tolerances can be factored in for each resistor throughout the signal chain. A table at the end of this article includes a minimum and maximum value for each resistor and how it influences the signal chain.

Amplifier errors

There are two types of amplifier errors:

- Inherent errors like bias current, offset voltage and common-mode error.
- Environmental-type errors like power-supply rejection ratio (PSRR) and temperature. These errors are more dependent on or influenced by outside parameters at the system level.

Table 2. Resistor error specifications

Diff Amp Circuit & Resistor Specs	Value	Unit
Amp Gain (Av), [Calculated]	4	
Amp Gain (dB), [Calculated]	12.04	dB
Rg	50	Ω
Rf	175	Ω
Rfint [DS][1]	25	Ω
Rs1 and Rs2	8.66	Ω
Rt	282	Ω
Characteristic Impedance (Z)	50	Ω
Resistor Coefficient	1000	ppm/°C
Resistor Tolerance	5	%
Resistor Life Tolerance, 1000 hours	2	%

[1][DS]—Value from datasheet

References 3 and 4 provide a fully functional model on amplifier errors and how they are manifested. Both documents go into great detail on the derivations of amplifier model errors. For simplicity, Figure 2 and Table 3 offer a breakdown of these errors.

The equations in Table 3 yield a referred-to-output (RTO) summary of errors that can be root-sum-squared (RSS) to achieve a total cumulative error for the amplifier as well as an output signal level in the signal chain.

With all resistor errors captured and organized, to start the amplifier analysis, it is best to solve the feedback factors, coefficients and equivalent resistances defined in Table 3. Each of these will provide a minimum and maximum, based on the minimum and maximum resistance values previously defined in Table 2.

Solving for the feedback factors, coefficients and equivalent resistances is the first step in understanding the output signal-level error or gain error based on the qualitative factors shown in Table 3. Next, calculate through all of the other errors listed in the amplifier error

Figure 2. Simple amplifier error model

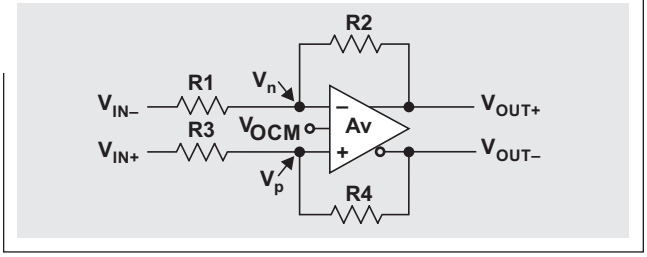


Table 3. Amplifier error equations (referred to output)

Quantity	Symbol	General Expression
Feedback Factors	β1, β2	$\beta_1 = \frac{R3}{R3+R4},\ \beta_2 = \frac{R1}{R1+R2}$
Coefficients	b1, b2	$b_1 = 1+\frac{1}{2\times CMRR},\ b_2 = 1-\frac{1}{2\times CMRR}$
Equivalent Resistances	R_{EQ1}, R_{EQ2}	R_{EQ1} = R1 || R2, R_{EQ3} = R3 || R4
Applied Input Common Mode	V_{ICM}	$V_{ICM} = \frac{V_{IN-}+V_{IN+}}{2}$
Desired Output	V_{OD}, Desired	$V_{id}\frac{2-(\beta_1+\beta_2)-\frac{1}{2\times CMRR}\times(\beta_1-\beta_2)}{(\beta_1+\beta_2)+\frac{1}{2\times CMRR}\times(\beta_1-\beta_2)+\frac{2}{a}}$
Output Error Due to Input Offset Voltage	$\Delta V_{OD}(V_{IO})$	$\frac{2V_{IO}}{(\beta_1+\beta_2)+\frac{1}{2\times CMRR}\times(\beta_1-\beta_2)+\frac{2}{a}}$
Output Error Due to Input Bias Currents	$\Delta V_{OD}(I_{IB})$	$2I_{IB}\frac{(R_{EQ1}-R_{EQ2})+\frac{1}{2\times CMRR}\times(R_{EQ1}-R_{EQ2})}{(\beta_1+\beta_2)+\frac{1}{2\times CMRR}\times(\beta_1-\beta_2)+\frac{2}{a}}$
Output Error Due to Input Offset Current	$\Delta V_{OD}(I_{IO})$	$I_{IO}\frac{(R_{EQ1}+R_{EQ2})+\frac{1}{2\times CMRR}\times(R_{EQ1}-R_{EQ2})}{(\beta_1+\beta_2)+\frac{1}{2\times CMRR}\times(\beta_1-\beta_2)+\frac{2}{a}}$
Output Error Due to Common Mode Mismatch	$\Delta V_{OD}(V_{OCM}-V_{ICM})$	$\frac{2(V_{OCM}-V_{ICM})(b_1\beta_1-b_2\beta_2)}{(\beta_1+\beta_2)+\frac{1}{2\times CMRR}\times(\beta_1-\beta_2)+\frac{2}{a}}$
Output Error Due to Input Common Mode	$\Delta V_{OD}(V_{ICM})$	$\frac{2V_{ICM}/CMRR}{(\beta_1+\beta_2)+\frac{1}{2\times CMRR}\times(\beta_1-\beta_2)+\frac{2}{a}}$
Output Error Due Power Supply Variations	$\Delta V_{OD}(\Delta V_S)$	$\frac{2\Delta V_S/PSRR}{(\beta_1+\beta_2)+\frac{1}{2\times CMRR}\times(\beta_1-\beta_2)+\frac{2}{a}}$

equation table and collect them in a spreadsheet: input offset error, input bias current error, common-mode mismatch, PSRR, etc. See Table 4.

Once completed, subtotal the simple RSS summation of the errors and add that total to the output signal level to obtain the total RTO error.

Interface errors

An anti-aliasing filter helps minimize the noise bandwidth coming from the amplifier. Even simple resistor-capacitor-type low-pass filters will wiggle and ripple through the pass band because of tolerances, parasitics and frequency mismatches. However, for simplicity in this signal-chain design, bandwidth is key, so a simple matching pad will interface between the output of the amplifier and the input of the ADC.

As previously described in the *Signal-chain overview and resistor errors* section, first calculate the values used to create the matching pad. Next, calculate the K-ratio errors based on standard 3-dB pad calculations found in most radio-frequency (RF) cookbooks or even an internet search. See Figure 3.

After obtaining the variance in loss of the pad (in this case, 3 dB nominal), it is possible to then determine the signal loss through this portion of the signal chain coming from the output of the amplifier, and what signal level the ADC will actually sample.

Table 4. Amplifier error specifications

Amplifier Specs	Design Spec.	Unit
Input Offset Voltage Drift	10	mV
Input Bias Current Drift	150	µA
Input Bias Current	70	µA
Input Offset Current	2	µA
PSRR	–80	dB
Input Offset Voltage	1	mV
Open Loop Gain (Av)	60	
Amp CMRR	72	dBc
Input CM	0.4	mV
Output CM	–27.0	mV
Input Voltage Noise	1.25	nV
Input Noise Current	3.5	pA

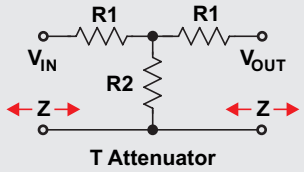
Figure 3. X-dB, T-attenuator pad calculations

dB = Attenuation in decibels
Z = Source/load impedance (resistive)
K > 1

$K = Z \times V_{IN}/V_{OUT} = 10^{dB/20}$

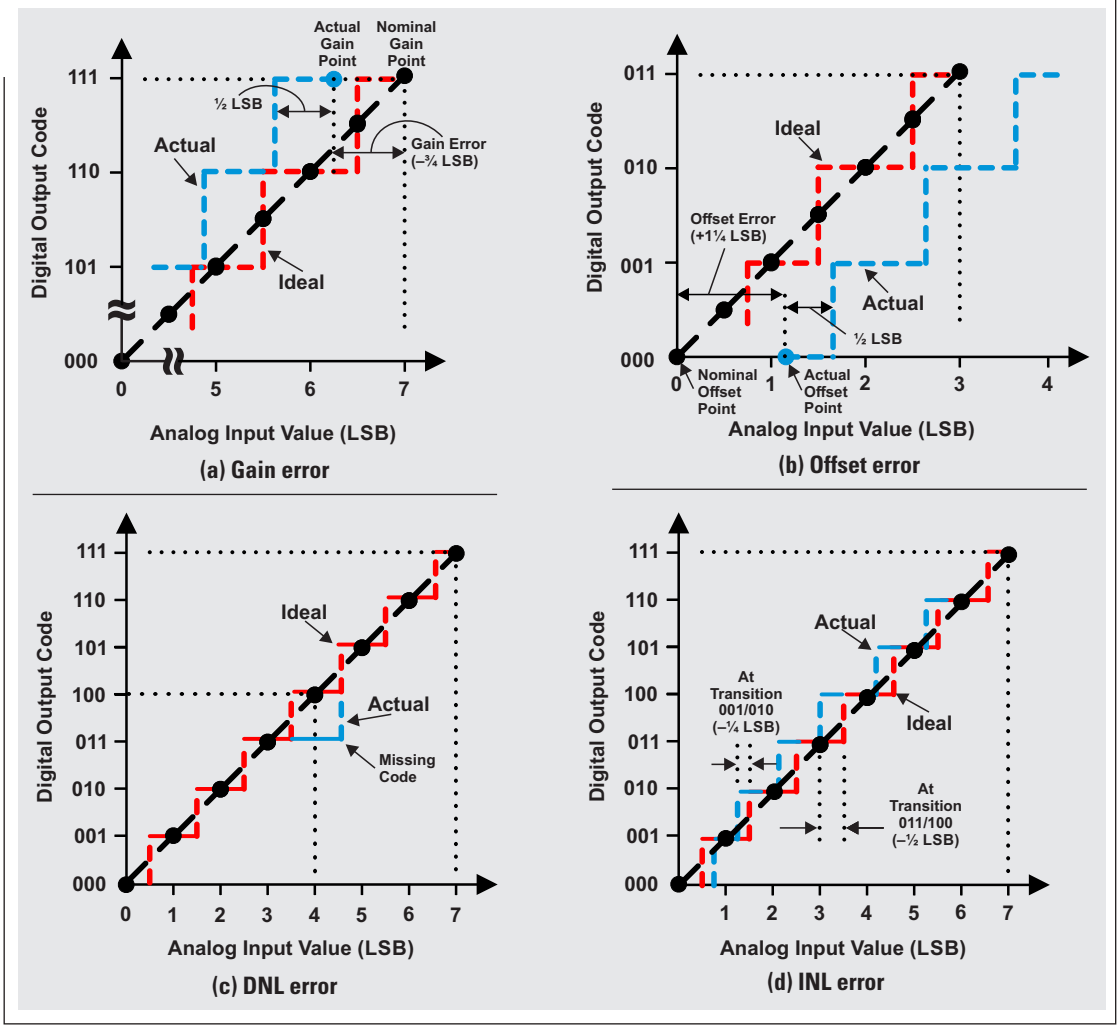
$R1 = Z \times (K - 1/K + 1)$

$R2 = Z \times (2K/K^2 - 1)$



Attenuation		Z = 50 Ω	
dB	$K = V_{IN} / V_{OUT}$	R1 (Ω)	R2 (Ω)
1.0	1.1220	2.88	433.34
2.0	1.2589	5.73	215.24
3.0	1.4125	8.55	141.93
4.0	1.5849	11.31	104.83
6.0	1.9953	16.61	66.93
10.0	3.1623	25.97	35.14
20.0	10.0000	40.91	10.10

Figure 4. DC errors: gain, offset, DNL and INL



Data converter errors

Finally, the signal hits the ADC, but it has errors as well; see References 1 and 6 for more information. Figure 4 illustrates four types of ADC errors: gain, offset, differential nonlinearity (DNL) and integral nonlinearity (INL). To get a better sense of the errors that affect the ADC's accuracy, PSRR should be included as well. While this spec can be difficult to find in some data sheets, the reasoning for including this particular error in Table 5 is that the headroom on data converter supplies is decreasing, largely driven by today's speed and bandwidth demands, which in turn, this drives the designs of these data converters into smaller process geometries. Table 5 sums these errors.

Like amplifier errors, calculating the RSS of these errors together will provide the total accumulation of error given by the data converter.

Table 5. ADC error specifications

ADC Specs.	Datasheet Spec.	Design Spec.	Unit
ADC Number of Bits		12	bits
ADC Input Full Scale (Differential)		800	mV_{PP}
ADC LSB Size, [Calculated]		195.31	μV_{PP}
Linearity (INL)	±2	4	LSB
Offset Error	±2	10	mV
Gain Error	±50	100	mV_{PP}
Offset Drift	23	30	µV/°C, LSB
Gain Drift	–0.01	40	%/°C, LSB
PSRR	5 LSB	–60	5 LSB, V
Clock Rate (fs)		10.4	GSPS
Ideal 12 bit SNR, [Calculated]		74	dB
SNR	55 at 1 GHz	55	dBFS
SINAD	53.4 at 1 GHz	53.4	dBFS
ENOB, [Calculated]		8.58	bits

Final analysis

It is now possible to RSS each subtotal error to get an understanding of the full accuracy error throughout the entire signal chain on the input signal, and what that difference is relative to the full-scale range of the ADC. Table 6 shows the final analysis.

The RSS approach is a popular way to properly sum errors throughout the signal chain because it isn't as pessimistic as a straight summation, also known as a worst-case analysis. There will always be some random variation of these errors, as some errors can cancel or move in opposite directions. Self-heating, temperature and other environmental factors also have an effect. Another approach is to assign a weighting factor into a particular error or set of errors, which helps to understand the sensitivity within a certain part of the signal chain that is critical to the design.

References

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Table 6. Full signal-chain error accumulation

Signal Chain Calculations	Min	Max	Unit
Amp Resistor Errors			
Total Tolerance ($Rg+R_{tol}+R_{tempco}+R_{life}$)	46.45	53.55	Ω
Total Tolerance ($Rf+R_{tol}+R_{tempco}+R_{life}$)	162.58	187.43	Ω
Feedback Factors 1 & 2	0.22	0.18	
Coefficients 1 & 2	1.0001	0.9999	
Equivalent Resistances 1 & 2	36.13	41.65	Ω
Total Tolerance (Gain/Loss)	3.5	4.57	Gain
Output Signal Level	1.10277	1.10281	V
Amp Errors			
Input Offset Voltage Error, [RTO][1]	4.5993	4.5994	mV
Input Bias Current Error, [RTO]	–1.77	1.78	mV
Input Offset Current Error, [RTO]	0.358	0.358	mV
CM Mismatch, [RTO]	–5.38	5.38	mV
Input CM, [RTO]	115.53	115.53	nV
PSRR, [RTO]	23	23	µV
Amp Total Accuracy Error, [RSS][2]	7.307	7.309	mV
Amp Output Signal Level, [RSS]	1.1101	1.1101	V
Network Errors			
Total Tolerance ($Rs1 \& Rs2+R_{tol}+R_{tempco}+R_{life}$)	8.05	9.27	Ω
Total Tolerance ($Rt+R_{tol}+R_{tempco}+R_{life}$)	261.98	302.02	Ω
K Ratio Tolerance (Rs)	1.38	1.46	
K Ratio Tolerance (Rt)	1.45	1.38	
Average Network Loss	2.82	3.25	dB
Amp & Network Output Signal Level	0.80208	0.7636	V
ADC Errors			
ADC Linearity, INL (LSB), [DS][3] = ±2.0		781.25	µV
ADC Offset Error, [DS] = ±2.0		1.9531	mV
ADC Gain Error, [DS] = ±50		800	μV_{PP}
ADC Offset Drift, [DS] = 23		24	µV
ADC Gain Drift, [DS] = –0.01 %		32	µV
ADC PSRR, [DS] = 5 LSB		550	5 LSB, nV
ADC Total Accuracy Error		2.2509	mV
Amp & ADC Total Accuracy Error [RSS]	**7.6459**	**7.6475**	**mV**
ADC Input Signal Level [RSS]	**804.3306**	**765.8546**	**mV**
DC Accuracy-FS	**4.81**		**%**

[1][RTO] = Referred to Output,
[2][RSS] = Errors are Root Sum Squared,
[3][DS] = Datasheet Spec.

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