Protect against high-current faults using hybrid hot-swap architecture

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Introduction

Rapid cloud adoption and technology trends such as the Internet of Things, artificial intelligence, and edge and high-performance computing demand faster and more flexible enterprise systems to manage workloads efficiently. Higher data throughput in data centers requires power-hungry, high-speed processors that push current levels beyond 250 A per server on a typical 12-V power rail, with a load capacitance between 20 and 30 mF to meet system transient load profiles.

A hot-swap circuit (a hot-swap controller in conjunction with a metal-oxide semiconductor field-effect transistor [MOSFET]) at the front end of each server provides inrush current limiting and protection against system faults such as overload, output short-circuit, etc. During a system fault, the hot-swap controller keeps the MOSFET in the saturation region to limit fault currents to a safe level. But these growing system currents, associated with a large output capacitance, pose significant challenges in designing a reliable hot-swap circuit because of the MOSFET's limited ability to handle power stress.

This article discusses the challenges of designing high-current, input circuit protection and how a hybrid hot-swap circuit comprising an eFuse in parallel with regular hot-swap controller can protect the MOSFET during any fault scenario.

A traditional hot-swap circuit

A simplified hot-swap circuit consists of a hot-swap controller, an external current-sense resistor and a power MOSFET. During system faults, the hot-swap controller pushes the MOSFET to operate in the saturation region to limit fault currents, causing a large drain-to-source voltage drop and severe power stress across the MOSFET.

The hot-swap controller implements a power-limit scheme (P_{LIM}) with a programmable fault timer (T_{TIMER}) for FET safe operating area (SOA) protection. Reference [1] iterates a procedure for designing a hot-swap circuit to protect the system and MOSFET. It is important to select appropriate P_{LIM} and T_{TIMER} values to ensure that the selected MOSFET operates under its SOA limits at a maximum operating temperature for stressful events. If the selected FET does not pass the design, you must pick a FET with stronger SOA, making hot-swap circuit design highly iterative and complex.

An eFuse has integrated overtemperature protection circuitry to monitor the internal FET temperature and turn off the FET when stressed for longer durations, ensuring that the FET operates within SOA limits. Currently, eFuse devices are limited to low currents, making external FET-based hot-swap solutions the only option for high-current circuit protection.

Challenges in designing a high-power hot-swap solution

To ensure that the FET stays within its SOA, the hot-swap controller implements a power-limit scheme, triggers the fault timer when the FET's power dissipation reaches P_{LIM} and turns off the FET after the T_{TIMER} duration if the power dissipation does not fall below P_{LIM}.

The hot-swap controller's power-limiting control loop, shown in **Figure 1**, consists of a current-sense amplifier that monitors the voltage across the sense resistance (V_{SNS}) to obtain current information, and a voltage-sense circuit to measure the voltage across the FET. Multiplying the output of the current-sense amplifier and voltage-sense circuit gives you the power loss in the FET, which you can use (once compared to the voltage proportional to P_{LIM}) to regulate the gate voltage. The hot-swap controller regulates the gate voltage, ensuring that the power dissipation in the MOSFET is always below P_{LIM}.
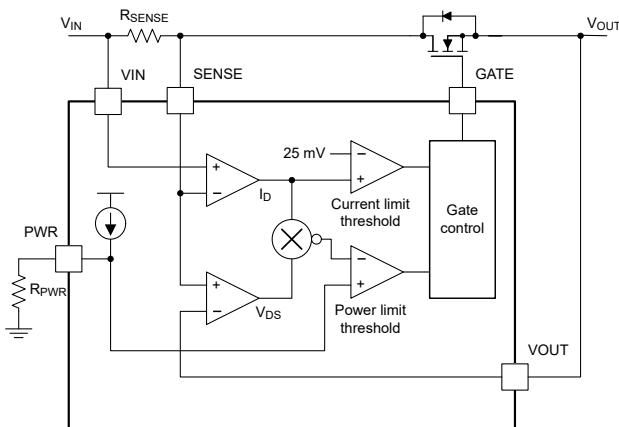

Figure 1. A power-limiting loop in a hot-swap controller.

While a lower power-limit setting reduces stress on the FET, it also reduces the amount of current that the hot-swap controller has to limit, and thus the V_{SNS} that the current-sense amplifier can detect. A low V_{SNS} results in a large error because the offset voltage of the current-sense amplifier puts a theoretical limit on the minimum possible power-limit setting. **Equation 1** provides the recommended minimum sense voltage ($V_{SNS-MIN}$) for most hot-swap controllers:

$$V_{SNS\_MIN} = \frac{P_{LIM} \times V_{SNS\_CL}}{V_{IN\_MAX} \times I_{LIM\_CL}} \qquad (1)$$

where, V_{SNS_CL} is the current-limit sense voltage, V_{IN_MAX} is the maximum input voltage and I_{LIM_CL} is the set current-limit threshold.

High-current applications require a higher current-limit threshold, forcing the need for a higher P_{LIM} setting to meet the V_{SNS_MIN} criteria defined by **Equation 1**. This increase in P_{LIM} demands a stronger MOSFET SOA, eventually leading to difficulty in finding a suitable MOSFET for high-power designs. For example, a 12-V, 250-A design requires a FET capable of handling 560 W of power stress for 1 ms at 100°C, which is impossible with existing commercial FETs.

Challenges with driving large capacitive loads

For designs with large output capacitances, output (dv/dt) control circuitry handles FET power stress during startup. Capacitor $C_{dv/dt}$ placed across Gate-GND limits the slew rate of the gate and the output voltage, which limits the inrush current.

The graphs below show a typical startup waveform with output dv/dt control. You must set a slew rate low enough, with an appropriate $C_{dv/dt}$ value, to keep the MOSFET within its SOA. MOSFETs can handle more energy when the power dissipation in them is reduced and spread over longer durations. Therefore, as the output capacitance increases, you need a higher $C_{dv/dt}$ to reduce the inrush current and power dissipation in the FET during startup. For example, operating a particular FET within the SOA may require a $C_{dv/dt}$ of 47 nF for an output capacitance of 10 mF, whereas a 30-mF output capacitance requires a $C_{dv/dt}$ of 330 nF.
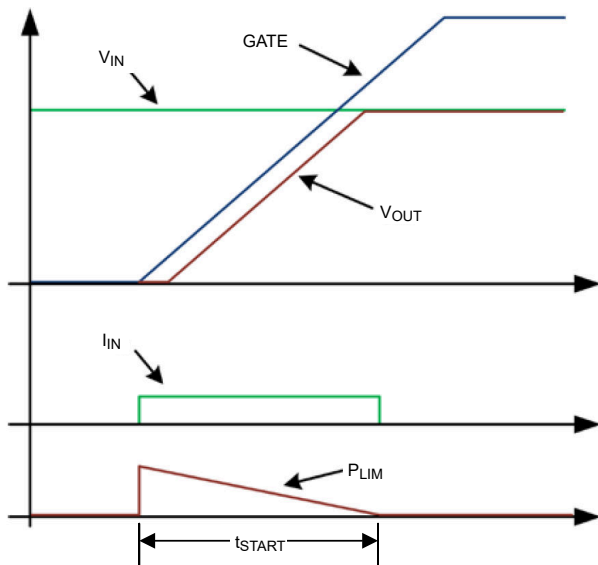
Figure 2. *Startup with output dv/dt control.*

During startup into short, the hot-swap controller requires a certain amount of current (I_{DS-INS} in **Equation 2**) to flow in the path in order to detect and trigger the power-limit fault.

$$I_{DS\_INS} = \frac{P_{LIM}}{VDS} \approx \frac{P_{LIM}}{V_{IN}} \tag{2}$$

A large $C_{dv/dt}$ slows down the gate voltage ramp rate and leads to a delay in reaching the required gate voltage to establish I_{DS-INS}, increasing the fault detection time and causing significant SOA stress on the MOSFET, especially as the impedance of the short (R_{short}) increases, defined by **Equation 3** and shown in **Figure 3**:

$$VG = VGS\_INS + (IDS\_INS \times Rshort) \tag{3}$$
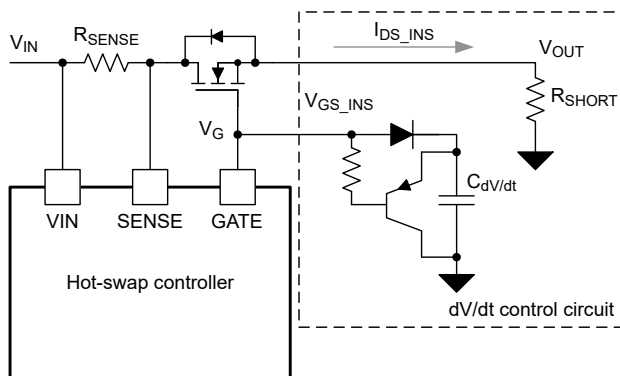
Figure 3. *A gate circuit under a high-impedance short circuit.*
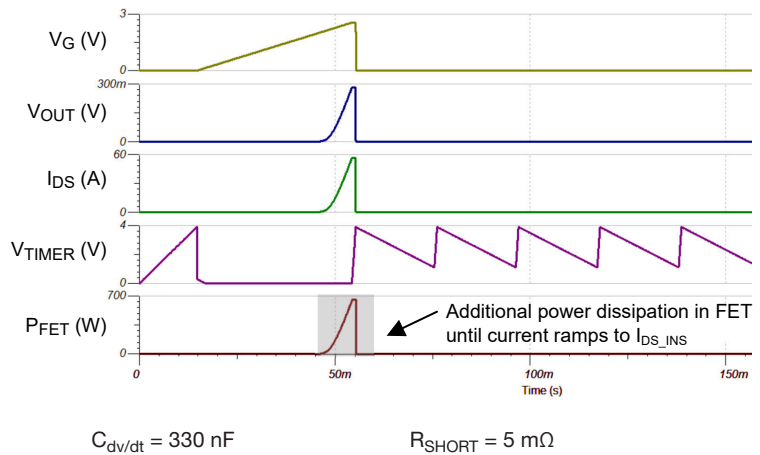
Figure 4. *Power stress on the FET with 5 mΩ impedance short.*
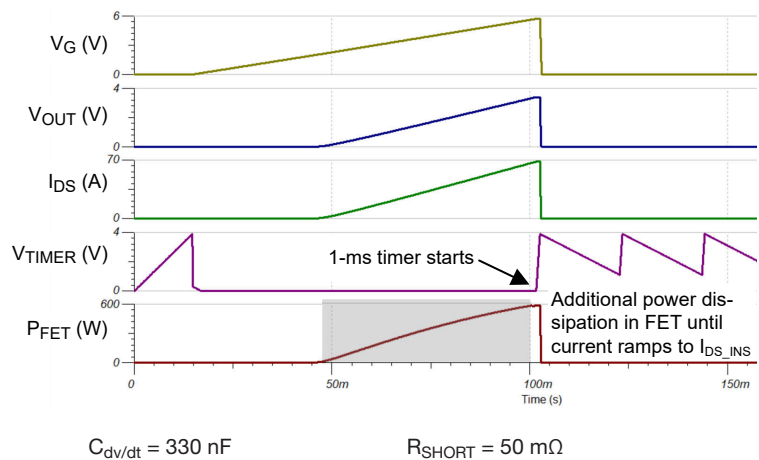
Figure 5. *Power stress on the FET with 50 mΩ impedance short.*

Consider an output short circuit with two different impedances: 5 mΩ and 50 mΩ. During a 5-mΩ short circuit at startup, as the gate voltage ramps up, the short-circuit current rises faster, reaching the power-limit threshold (300 W) in only 6 ms. Once the threshold is reached, T_{TIMER} engages and the FET turns off. On the other hand, a 50-mΩ short circuit impedance slows down how quickly the short-circuit current rises, taking approximately 50 ms for the hot-swap controller to detect a power-limit threshold of 300 W. This wattage corresponds to 15J of energy, which is huge and can damage the FET as shown in **Figure 5**.

A hybrid hot-swap solution

A hybrid hot-swap solution consists of an eFuse connected in parallel with the traditional hot-swap circuit, as shown in **Figure 6**. In this circuit, the eFuse will handle stressful events by leveraging the integrated overtemperature protection function in the eFuse.
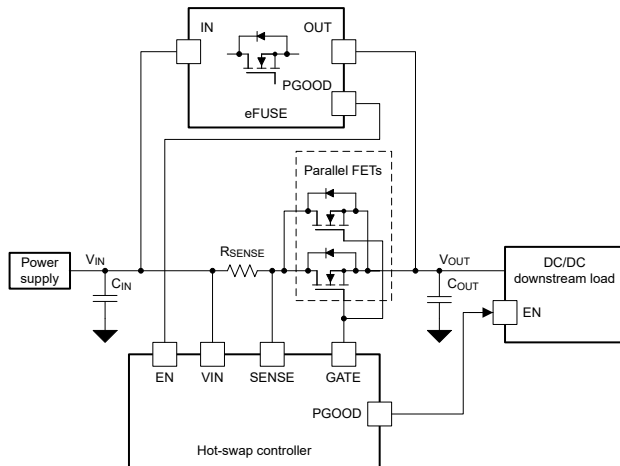

Figure 6. *Hybrid hot-swap configuration.*

The PGOOD signal of the eFuse connects to the enable pin of the hot-swap controller, and the PGOOD signal of the hot-swap controller connects to the enable pin of the downstream load. These connections ensure that:

- The hot-swap FETs turn on only after the eFuse charges the large output capacitor close to the input voltage. The FETs start up with almost zero voltage across them, eliminating power stress during startup.
- The downstream load is enabled only after the hot-swap FETs are fully enhanced so that the FETs can offer a low impedance path (compared to the eFuse) and share the majority of the load current.
- The eFuse endures power stress during all fault conditions, and the hot-swap FETs are not subjected to stress in any condition.

Figure 7 illustrates the functionality of the circuit during startup and different fault conditions. States 1 to 5 depict the sequence of events during startup, while states 6 through 9 are in intermediate states of different fault conditions.
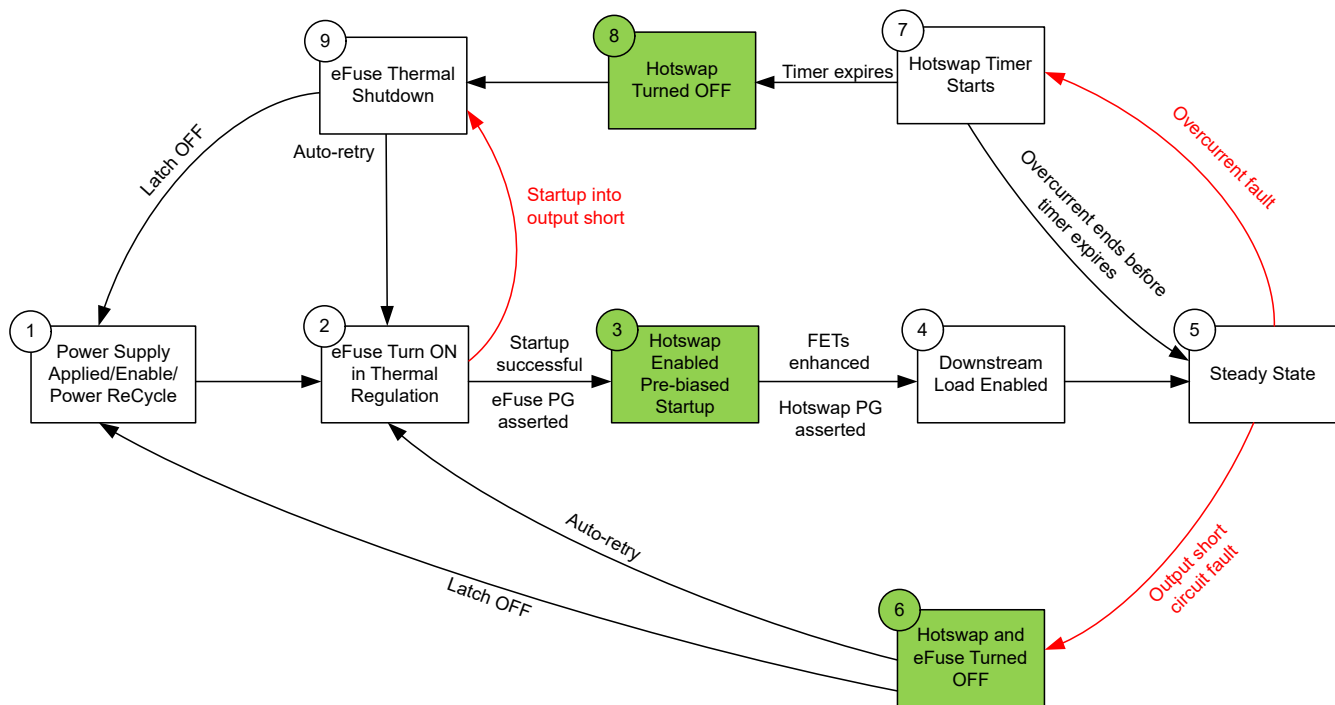
Figure 7. *Flow chart of the hybrid hot-swap solution.*

The major advantage with a hybrid hot-swap approach is that the hot-swap FET SOA is no longer critical; you can select the lowest drain-to-source on-resistance ($R_{DS(ON)}$) FETs, which are generally cheaper and significantly reduces the number of FETs.

Key design considerations

The first design consideration is the number of parallel FETs in the hot-swap path. We recommended operating the FETs in steady state such that the junction temperature is less than 100°C. **Equation 4** calculates the number of FETs required in parallel for a given load current:

$$T_J = \left[\left(\frac{I_{LOAD(MAX)}}{\text{No\_of\_FETs}}\right)^2 \times R_{ds(on)} \times R_{QJA}\right] + TAMB \leq 100^oC \tag{4}$$

where, T_J is the FET junction temperature, $I_{LOAD(MAX)}$ is the maximum load current, $R_{ds(on)}$ is the maximum $R_{ds(on)}$ of the selected FET and R_{QJA} is the FET's junction-to-ambient thermal resistance.

Next, select the eFuse. The **TPS1663** eFuse has an integrated thermal regulation loop to provide a clean startup with large capacitive loads. Reference [**2**]

explains how to power large and unknown capacitors with this device.

In steady state, the hot-swap path offers low impedance compared to the eFuse path, and thus shares most of the load current. The hot-swap controller still determines the overcurrent protection threshold, just like in the traditional hot-swap design. Set this threshold at just over the maximum load current.

For the eFuse, set the current limit at its maximum value (6 A for the TPS1663) to achieve the fastest possible output capacitor charging during system startup.

T_{TIMER} is no longer critical for the FET SOA, as hot-swap FETs are not subject to any stress in a hybrid hot-swap architecture. You can select the fault timer duration setting solely dependent on the load transient requirements.

High-power designs use multiple FETs in parallel, but the limited gate-drive strength of the hot-swap controller

increases the FET's turnon delay. It is recommended to add an additional delay (in the range of 5 ms) when turning on the downstream load to provide enough time for the hot-swap controller to fully enhance the FETs.

Figure 8 shows an example hybrid hot-swap circuit using the LM25066 hot-swap controller and TPS1663 eFuse for a 12-V input, 250-A load current and 30-mF output capacitance.
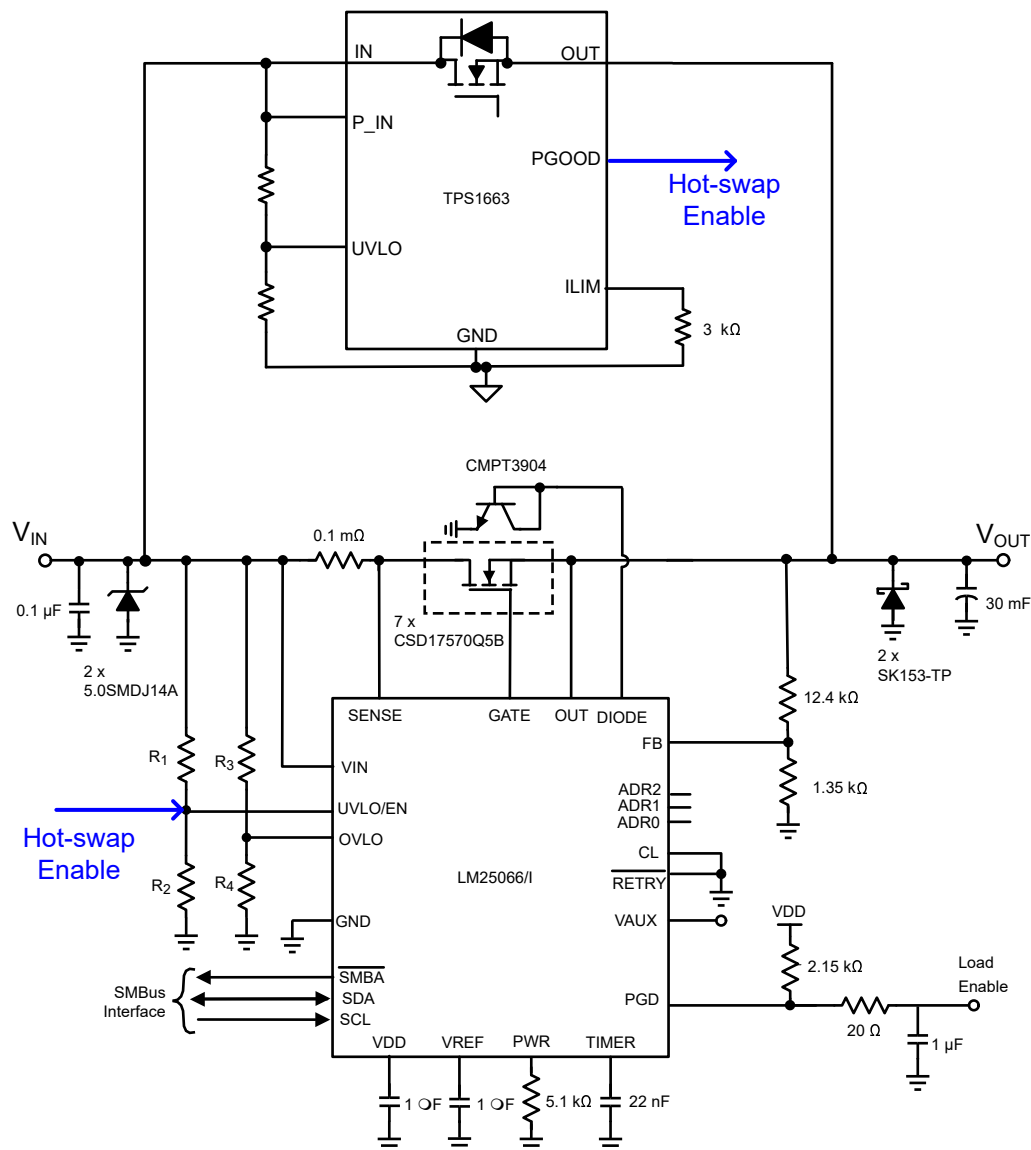
Figure 8. Hybrid hot-swap circuit.

Test results

The hybrid hot-swap solution for stressful events using the **LM25066 evaluation board** and **evaluation module for the TPS26633 and TPS16630** with a 30-mF output capacitor and 10-A hot-swap current limit was verified.

Figure 9 shows the startup and steady-state behavior of the circuit. During startup, the entire current required to charge the output capacitors flows through the eFuse, as the hot-swap path is not yet enabled. After the startup phase, almost the entire load current flows through the hot-swap path as it is the low-impedance path.
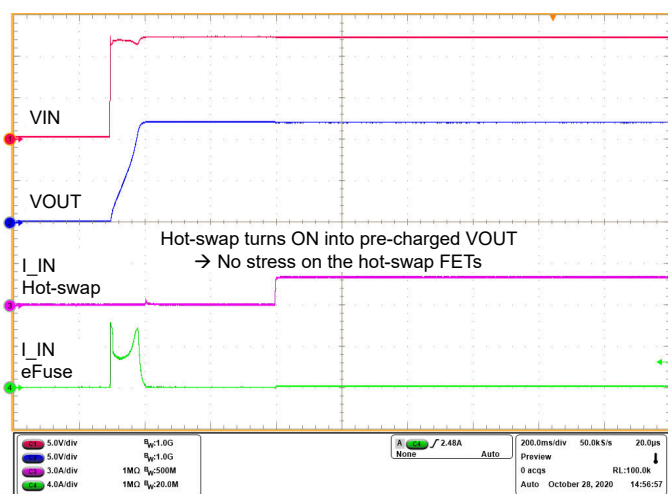
Figure 9. Startup with 30-mF capacitance.

Figure 10 shows the startup behavior of the circuit with a short circuit at the output. The eFuse enters thermal regulation mode at startup and turns off after the thermal regulation timeout. The eFuse continues retrying periodically every 650 ms until removal of the output fault. Because the hot-swap FETs remain off, there is no stress on them.
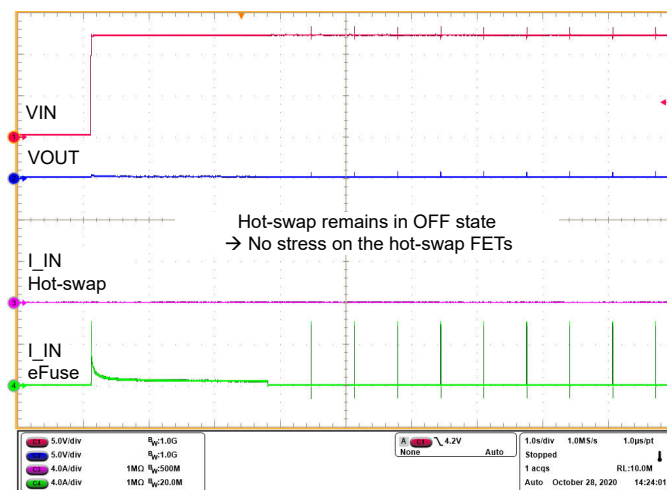
Figure 10. Startup into a short circuit.

In the event of an overload fault, the hot-swap circuit allows the overload current for the timer duration before turning off its FETs. **Figure 11** shows that after turnoff of the hot-swap FETs, the entire load current transfers to the eFuse path, triggering the current limit and eventually thermal shutdown.

Figure 12 shows the circuit behavior during an output short-circuit fault in steady state. Both the hot swap and eFuse turn off immediately in order to protect the input supply from damage. The eFuse continues retrying periodically and the hot-swap FETs remain off until successful startup of the eFuse.
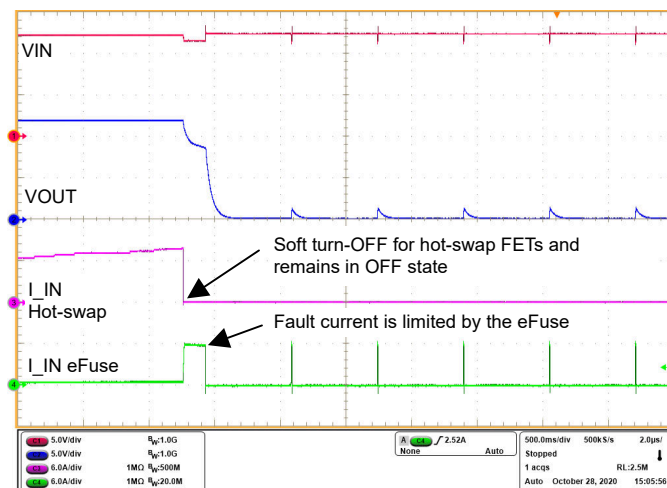
Figure 11. Circuit response during an overload fault.
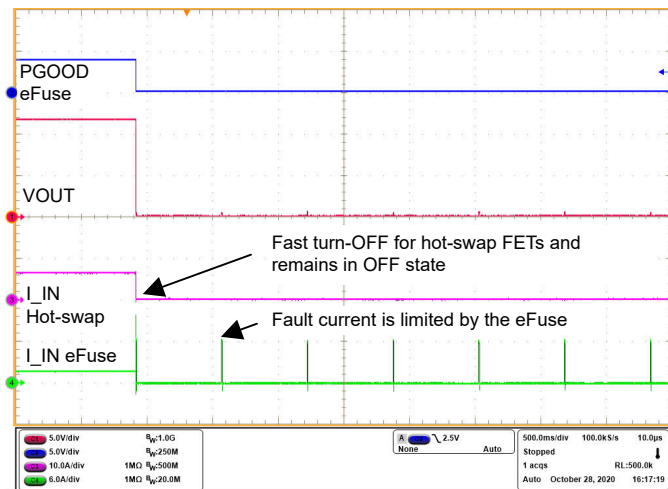
Figure 12. *Circuit response during an output short circuit.*

Conclusion

The ever-increasing power levels of server systems have pushed input bulk capacitance requirements to 20 to 30 mF and full load currents in the 12-V rail above 200 A. A hybrid hot-swap solution that uses an additional eFuse in parallel not only solves the challenges of traditional protection circuits at higher power levels but also eliminates hot-swap FET SOA concerns, simplifying hot-swap designs and significantly reducing solution costs. The hybrid hot-swap solution, when tested for different fault conditions, proves that the circuit eliminates stress on hot-swap FETs.

References

1. Texas Instruments: *Robust Hot Swap Design*
2. Texas Instruments: *Reliable Start-up with Large and Unknown Capacitive Loads*

Related Websites

- **LM25066I**
- **TPS1663**

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