Texas Instruments

ISSUE 1, 2026

Analog Design JOURNAL

Table of contents

Achieving nanosecond-level precision laser pulse control for lidar and ToF systems

Leaphar Castro
Member Group Technical Staff

Anant Sinha
Application Engineer, High-Speed Amplifiers

Introduction

The growing adoption of autonomous vehicles, industrial automation and advanced robotics is increasing demand for reliable 3D ranging and sensing. Lidar and time-of-flight (ToF) systems rely on precisely controlled laser pulses to measure distance and spatial information. Meeting these requirements demands laser drivers that deliver high peak current and maintain pulse-to-pulse stability across temperature and aging. Whether used for navigation or high-speed industrial inspection, these systems depend on fast, stable and repeatable laser pulses under practical conditions. Traditional discrete topologies that use gate drivers, external field-effect transistors, and current-sensing elements can meet specific design requirements; however, they often introduce trade-offs in terms of layout complexity, calibration effort, and thermal performance.

What makes laser pulse control challenging?

Laser drivers do more than deliver current. They directly influence the timing information that lidar and ToF systems use to calculate distance. Consider a simple timing variation budget comprising of several sources, where for the purposes of this article there are three contributors:

- Rise and fall time ($t_{r/f}$): how quickly the pulse moves through the detection threshold.
- Propagation delay (t_{pd}): how long it takes from the trigger to actual light emission.
- Pulse-to-pulse variation (t_{pp}): how much the timing or amplitude drifts from pulse to pulse.

Effects of rise and fall times

Lidar and ToF systems measure the distance by calculating the round-trip time for a laser pulse to travel to a target and return to a receiver. The ability to distinguish small distance changes depends on how quickly the pulse edges transition between no light and full light. Faster rise and fall times reduce distance uncertainty and give the receiver a clearer reference point. In high-resolution systems, rise and fall times typically range from 1ns to 5ns.

When a pulse edge is slow, the system cannot determine the exact moment the signal crosses the receiver detection threshold. A $t_{r/f}$ equal to a 1ns edge therefore introduces about 150mm of distance uncertainty, approximated by **Equation 1**:

$$\Delta D = \frac{ct_{r/f}}{2} \quad (1)$$

where ΔD is the delta distance and $c \approx 3 \times 10^8$m/s.

This uncertainty increases with slower pulse edges, which parasitics such as package and printed circuit board (PCB) inductance can limit, along with the capacitance of the laser diode and driver output. For example, increasing $t_{r/f}$ from 500ps to 1ns doubles the distance, while edges of 2ns expand it to nearly

300mm, limiting the system's ability to distinguish smaller differences in target distance then ΔD.

Propagation delay

In high-speed optical systems, every nanosecond matters. If the propagation delay changes with temperature, supply voltage or component tolerances, it shifts the timing reference used for distance calculations and can also disrupt synchronization between channels. In direct ToF applications (dToF), a 100ps variation in t_{pd} corresponds to roughly 30mm of distance error, based on the ToF relationship shown in **Equation 2**:

$$D = c \times t \quad (2)$$

where $c \approx 3 \times 10^8$m/s, D is the distance and t is the time.

Any excess delay directly translates into ranging error. As shown in **Figure 1**, a 500ps variation could result in more than 150mm of round-trip distance error, which is unacceptable in dToF systems targeting centimeter- or millimeter-level accuracy.

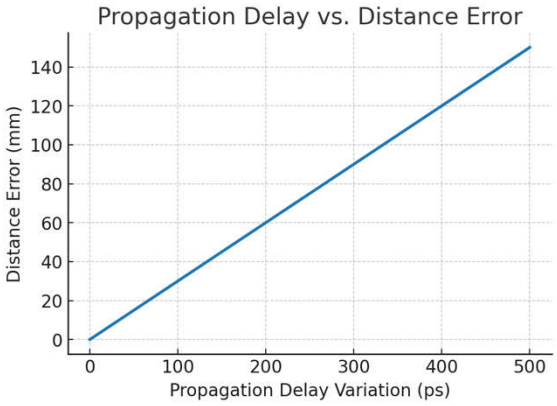


Figure 1. *Propagation delay vs. distance error (estimated)*

It is possible to calibrate fixed delays during system alignment, but variable delays such as self-heating introduce measurement-to-measurement uncertainty that is not easily correctable.

Pulse-to-pulse stability

Even a fast, narrow laser pulse must remain consistent from one pulse to the next. Variations in peak current translate directly into changes in optical power, degrading measurement accuracy and system reliability. Temperature shifts, supply fluctuations and device aging are common sources of this drift.

From a system perspective, the receiver relies on the returned optical signal to determine distance. Differences in pulse strength can therefore be misinterpreted as range variation, particularly at long distances where return signals approach the detection threshold. In threshold-based ranging systems, a 1% change in peak current produces roughly a 1% change in optical power, which can introduce distance errors on the order of tens of centimeters. As shown in **Figure 2**, even modest amplitude variations of ±2% to ±5% can alter the pulse envelope and optical energy delivered per pulse, reducing ranging accuracy and repeatability over time. High-performance designs therefore tightly control the drive current, keeping t_{pp} variation within a few percent across all operating conditions.

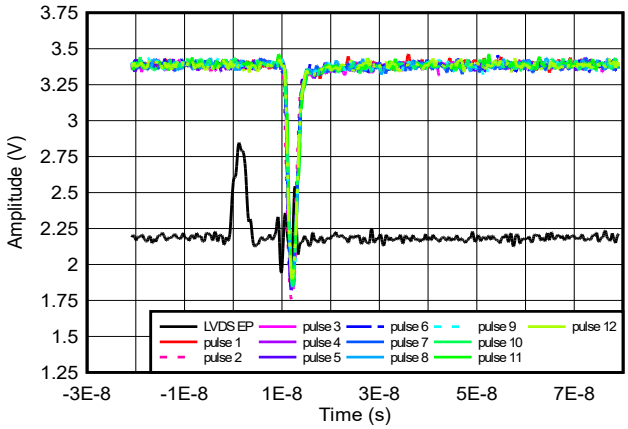


Figure 2. *Pulse-to-pulse amplitude for 12 pulse, 1.5A current, Rdamp =1Ω and 2 snubber pair of 5Ω resistor and 330pF cap, AVDD = PVDD = VLD = 5V*

With the system-level timing constraints defined, the next step is translating them into a practical laser driver implementation.

Implementing precise laser pulse control

Generating accurate laser pulses requires more than delivering current into the diode. The driver must deliver high peak currents with fast edges, predictable delay and

repeatable pulse amplitude. TI's LMH13000 high-speed laser driver generates pulses by converting the input voltage at the V_{SET} pin into a precisely regulated sink current at I_{OUT}, as described by **Equation 3**. A digital-to-analog converter (DAC) or reference source sets V_{SET}, while the device's internal current mirror and control circuitry regulate the current through the laser diode, as shown in **Figure 3**. Careful selection of V_{SET}, R_{SET} and the laser anode bias voltage (VLD) allows designers to tune the pulse amplitude, timing and overall pulse stability.

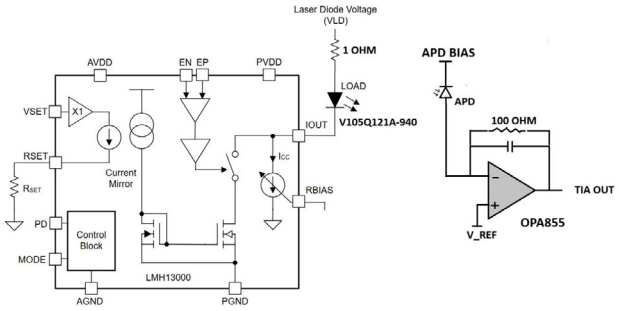


Figure 3. *Circuit schematics transmit path block diagram with a diode and the LMH13000*

Here are the design steps for setting pulse current and speed.

1. Define the target output current (I_{OUT}). Begin with the optical power that the laser diode requires. **Equation 3** expresses the peak output current, set by the laser's slope efficiency:

$$I_{OUT} = \frac{P_{OPT}}{\eta} \quad (3)$$

where P_{OPT} is the desired optical output power and η is the laser's slope efficiency (watts per ampere). For example, if P_{OPT} = 1W and η = 0.5W/A, then I_{OUT} = 2A.

Because the LMH13000 supports pulsed currents up to 5A, the selected laser diode must achieve the target optical power at or below this limit. Accurately setting I_{OUT} is paramount for minimizing t_{pp} and reducing amplitude-driven timing errors.

2. Select R_{SET} and V_{SET}. The LMH13000 sets the output current using the ratio of V_{SET} to R_{SET}, scaled by an internal gain factor k (**Equation 4**):

$$I_{OUT} = \frac{V_{SET}}{R_{SET}} \times k \quad (4)$$

In high-current mode (MODE = 1), k ≈ 50k. For example, with R_{SET} = 20kΩ and V_{SET} = 0.8V:

$$I_{OUT} = \frac{0.8}{20k} \times 50k \approx 2.0A$$

It is possible to make fine adjustments by trimming V_{SET} with a DAC. Because the LMH13000 regulates current on-chip, this approach minimizes sensitivity to temperature and supply variations, helping keep t_{pp} small within the timing budget.

3. Set the VLD. VLD must be high enough to support the laser forward voltage and dynamic voltage required during fast current transitions. The LMH13000 data sheet provides **Equation 5** as a sizing guideline:

$$VLD = V_{OUT(MIN)} + V_F L \times \frac{dI}{dt} + I_{OUT} \times (R_{LASER} + R_{DAMP}) \quad (5)$$

where:

- V_{IOUT} is the minimum compliance voltage at I_{OUT}
- V_F is the forward voltage of the laser at I_{OUT}
- L is the total loop inductance (package and PCB)
- dI/dt is the current slew rate (amperes per second) from rise and fall requirements
- R_{LASER} is the dynamic resistance of the laser diode
- R_{DAMP} is the external resistance of the laser diode

For example, with:

$$V_{IOUT(MIN)} = 6V$$

$$V_F = 2V$$

$$L = 3nH$$

$$\frac{dI}{dt} = \frac{2A}{1ns} = 2 \times 109A/s$$

$$R_{LASER} = 0.3\Omega$$

$$R_{DAMP} = 1\Omega$$

$$VLD \approx 6 + 2 + \left(3 \times 10^{-9}\right)\left(2 \times 10^{9}\right) + 2(0.3 + 1.0) \approx 16.6V$$

A starting value of 17V is therefore appropriate. Increasing VLD improves the edge speed but can increase overshoot, thus requiring careful tuning. Proper VLD selection ensures fast transitions while limiting overshoot, directly reducing the rise and fall time ($t_{r/f}$) contribution to the overall total timing variation (t_{total}) budget.

4. Optimize rise and fall times and damping. Both driver capability and circuit parasitics set the rise and fall times. Without proper damping, fast current pulse transitions can excite ringing in the laser and PCB loop, causing overshoot and unstable optical pulses. Designers commonly address this by adding a damping resistor and snubber network at the I_{OUT} node. Together, the resistor and snubber suppress parasitic ringing, preserve fast edges, and prevent $t_{r/f}$ from unnecessarily increasing t_{total}.

   Select snubber capacitors based on the output capacitance of the driver, calculated using **Equation 6**:

$$C_{SNUB} \approx 5 \times C_{IOUT} \quad (6)$$

   where C_{IOUT} is the effective capacitance at the I_{OUT} pin. If C_{IOUT} = 40pF, then $C_{SNUB} \approx$ 200pf.

   Adding a small damping resistor in series with the laser and snubber network suppresses unwanted oscillations. As shown in **Figure 4**, typical values for R_{DAMP} and R_{SNUB} are in the 5Ω to 10Ω range, with the snubber capacitor sized to the output node capacitance. Select C_{SNUB} for the worst-case (highest) C_{IOUT}, trimming during validation to balance overshoot and edge speed. As illustrated in **Figure 5**, this approach reduces ringing from fast transitions and PCB parasitics, while preserving the sub-nanosecond $t_{r/f}$ required for precise pulse control.

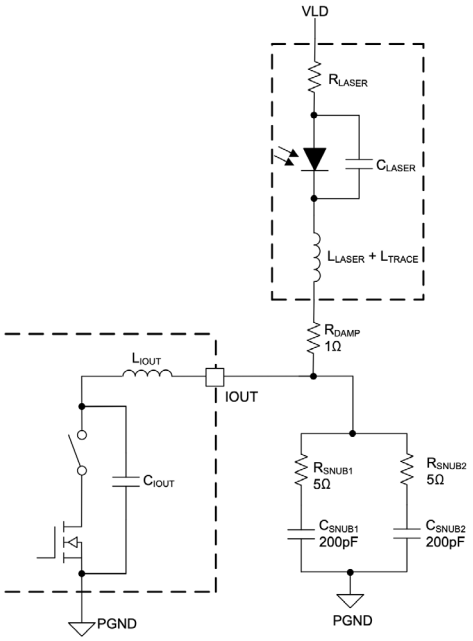


Figure 4. *Damping resistor and snubber network circuit*

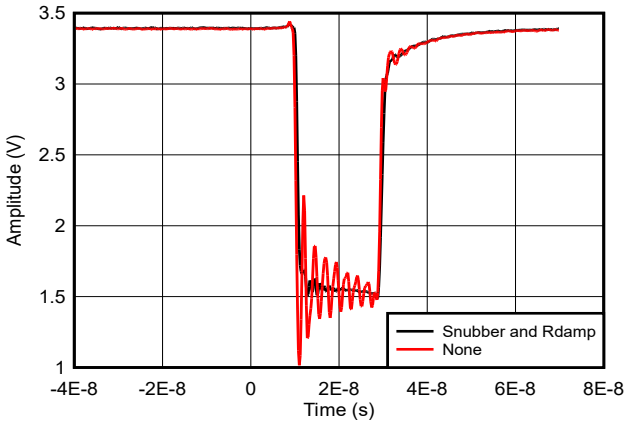


Figure 5. *The LMH13000 pulse with and without a snubber circuit or R_{DAMP}*

5. Control the propagation delay. Unlike rise and fall times, propagation delay is not defined by a formula

but instead depends on these layout and interface practices:

- Input routing. Use differential routing for EP pin and EN pin with 100Ω termination, or route a single-ended input with controlled impedance and proper termination at the LMH13000 input.
- Output loop. Keep the high-current I_{OUT} loop short and tightly coupled to PGND to minimize inductive delay and ringing.
- System calibration. Account for any residual system delay by including the driver-laser path in the ToF measurement budget.

As shown in **Figure 6**, minimizing the trace inductance and ensuring consistent input termination reduces variation in t_{pd}, keeping this contribution small and predictable. For applications that require even higher accuracy or where temperature-based calibration is not practical, Section 6.3.2 of the **LMH13000 datasheet** presents a technique for high-accuracy start-pulse generation by directly monitoring the laser stage.

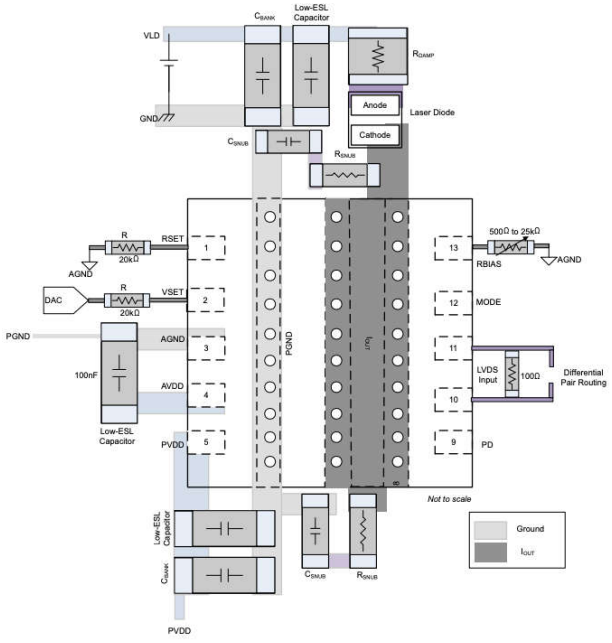


Figure 6. *Layout example of the LMH13000 in the surface-mount device package*

Precise pulse control in pulsed systems

Lidar and ToF systems typically operate in pulsed mode, generating high-current bursts separated by long off-times. In this mode, the current waveform must settle quickly and reach the same peak value on every pulse. A common approach is to pre-bias the laser anode through VLD and use the LMH13000's low-voltage differential signaling (LVDS) inputs (EP, EN) to gate the pulses. This enables V_{SET} pin to set the amplitude while the LVDS inputs independently control the timing.

With R_{DAMP} = 2.6Ω, VLD = 12V and I_{OUT} = 400mA (laser diode: Osram's PLT5 518FB_P), **Figure 7** shows the lab result with a laser diode. In the figure, blue is enable, yellow is the start pulse and orange is V_{ANODE}. Decoupling amplitude and timing minimizes pulse-to-pulse drift and preserves fast edges, improving both amplitude stability (t_{pp}) and edge consistency ($t_{r/f}$), further lowering t_{total}.

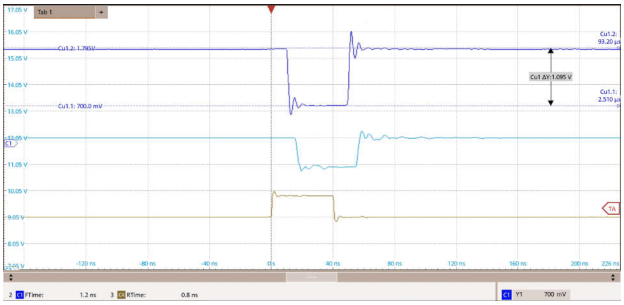


Figure 7. *Precise pulse control in pulsed mode*

Practical example with transmitter test results

Testing the LMH13000 under the lidar transmitter conditions shown in **Table 1** validates the design principles.

Design parameters	Value
Diode	V105Q121A-940
Analog VDD and power VDD	5V
Mode	1
Pulse current	2A peak
Pulse width	0.6ns, 0.7ns
R_{SET}	20kΩ
V_{SET}	0.5V (set by the DAC)
VLD	4.5V, 5V, 6.5V

Design parameters	Value
Damping network	R_{DAMP} = 1Ω R_{SNUB} = N/A C_{SNUB} = N/A (no snubber)

Table 1. *Design parameters for LMH13000 pulse driver example*

Figure 3 shows the test setup, which illustrates the circuit schematic used to bias the laser and configure the LMH13000.

Figure 8 shows the optical response of the LMH13000 at different VLD bias voltages during pulsed operation. The transient waveforms illustrate how VLD directly affects rise times, overshoot and steady-state current regulation. A lower VLD results in slower edge transitions, while a higher VLD improves speed but may increase overshoot. Selecting the appropriate VLD, therefore, balances $t_{r/f}$ against pulse stability to minimize its contribution to the overall variation budget.

This design demonstrates how careful biasing and damping produce fast, stable optical pulses with minimal overshoot and repeatable performance. Based on the variation budget, this design achieves $t_{r/f}$ <1ns, t_{pd} variation <50ps, and t_{pp} <2%. Together, these results yield a t_{total} well below 1ns, enabling millimeter-level range precision. Additional improvement is possible by incorporating a temperature sensor to compensate for delay drift and amplitude shifts in real time, further reducing environmental contributions to the variation budget.

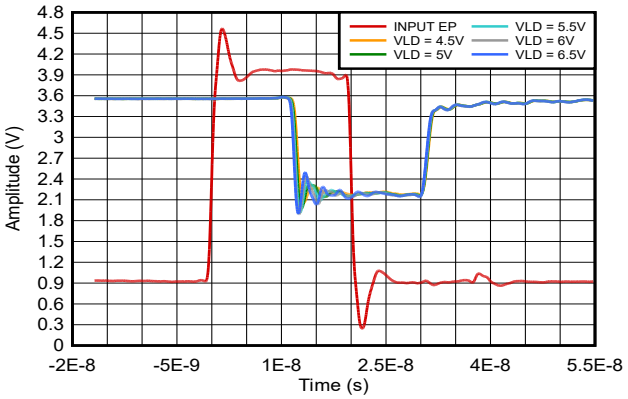


Figure 8. *Optical response at a 4.5, 5, 5.5, 6 and 6.5 VLD bias voltage*

Conclusion

Precise laser pulse control requires balancing edge speed, timing accuracy, stability and optical power consistency. By integrating high-speed current drive and regulation into a compact solution, the LMH13000 reduces design complexity while improving repeatability and performance.

When combined with simple feedback and temperature monitoring techniques, this laser driver provides a reliable platform for both continuous and pulsed laser operation, enabling reliable and accurate performance in demanding lidar, ToF and industrial optical sensing applications.

Additional resources

- Read the application brief, **Automatic Power Control for Laser Diodes Using LMH13000**.
- Check out the white paper, **An Introduction to Automotive Lidar**.
- Download the **LMH13000 TINA-TI™ software Spice model**.

About the authors

Leaphar Castro is a product marketing engineer at Texas Instruments, specializing in high-speed amplifier products and supporting various industrial markets, including industrial automation. He received a bachelor's degree in electrical engineering from the University of Central Florida in 2016. Leaphar is Member Group Technical Staff on TI's Technical Ladder.

Anant Sinha is an applications engineer focused on high-speed amplifier products at Texas Instruments. He received a bachelor's degree in instrumentation and electronics engineering from Jadavpur University.

How integrated isolated bias modules improve power density and reliability

Mark Allen Esquillo
Marketing Manager, High-Voltage Power

Carter Pollan
Applications Engineer, High-Voltage Power

Introduction

Isolated bias supplies are critical building blocks in high-performance power electronics such as traction inverters, solar inverters, and data-center power-supply systems, yet they require trade-offs between power density and development time. Isolated DC/DC designs rely on discrete transformers and switching components, which often introduce challenges in meeting power density, reliability and time-to-market requirements.

Isolated bias power modules with TI's IsoShield™ packaging technology combine switching field-effect transistors (FETs), control circuitry, and a planar isolated transformer in a compact package to address these challenges. In this article, I'll explain how these modules reduce board area while improving immunity to electrical and environmental disturbances, while at the same time simplifying design in modern high-voltage systems.

How increased power density reduces solution size while meeting EMI requirements

The design of isolated bias supplies often involves balancing multiple constraints: board space, thermal performance, and electrical isolation. In applications such as electric vehicle traction systems or data center power architectures, you must provide isolation between high-voltage domains (often ≥800V) and low-voltage control circuits.

Traditional designs implement isolated bias supplies using a discrete flyback converter topology. In these implementations, the transformer is typically the largest component on the printed circuit board (PCB), limiting the achievable power density and increasing solution height.

Isolated bias power modules with IsoShield technology address high power density to meet optimized size requirements in system design by incorporating a planar transformer directly inside the package (as shown in **Figure 1**), and by using a multiple-chip solution with proprietary bonding connections to create a very compact isolated module.

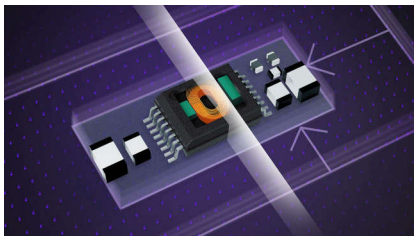


Figure 1. *Isolated power module with integrated planar transformer*

The mid-voltage **UCC34141-Q1** and low-voltage **UCC33420-Q1** deliver approximately 1.5W of isolated output power – the former in a 5.85mm-by-7.50mm-by-2.65mm small outline integrated circuit (SOIC) package, the latter in a 4mm-by-5mm-by-1mm very, very small outline, no-lead (WSON) package.

By integrating the transformer and switching elements, these power modules can reduce bias-supply solution area approximately 70% compared to discrete flyback implementations and >35% compared to previous integrated transformer solutions. These reductions translate into power-density improvements >300%.

In addition to footprint reduction, the vertical profile is significantly reduced. Removing the discrete transformer – the tallest component in conventional designs – enables module heights as low as 1mm, which is particularly beneficial in space-constrained applications. **Figure 2** shows the solution area reduction associated with moving from a discrete flyback converter implementation (on the left) to a fully integrated solution (on the right).

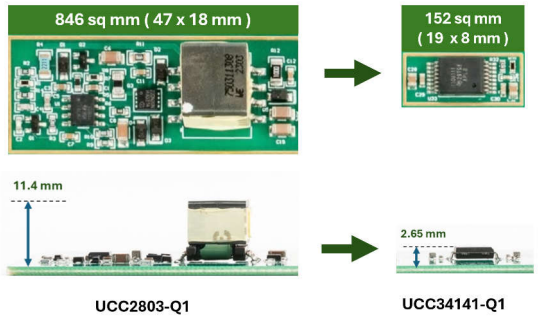


Figure 2. *Top and side view comparison of a discrete solution to a fully integrated isolated module*

Thermal performance and electromagnetic interference (EMI) are often concerns with high-density solutions. However, optimized packaging and internal layout can improve thermal dissipation as much as 30% compared to previous modules while maintaining compliance with Comité International Spécial des Perturbations Radioélectriques (CISPR) 25 and CISPR 32 standards, using only minimal filtering (**Figure 3**).

Figure 3. *CISPR 25 radiated emission data (Pout = 1W)*

Designing an EMI solution for a standard isolated bias supply is a nontrivial task. Balancing costly filtering components with the unique filtering needs of a discrete implementation takes experience, time and testing. The nature of an integrated solution means that the filtering needs are much more standardized. TI has taken advantage of this fact by developing application notes that describe how to implement EMI solutions that will pass CISPR standards.

The layout shown in **Figure 4** with the solution and small filter size meets the CISPR 25 Class 5 requirement. When combined with a few layout techniques, there are only a few additional bill-of-material components needed to pass CISPR 25 Class 5. In this example we use the highlighted capacitors, inductors, and ferrite beads.

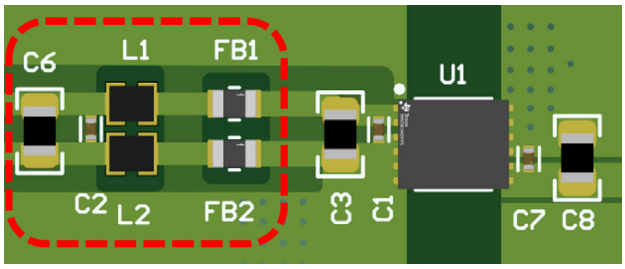


Figure 4. *A small solution and filter size meets CISPR 25 Class 5 requirements*

Several layout techniques can further reduce the number of filtering components. Placing high-frequency filtering capacitors C1 and C7 very close to the IC minimizes high-frequency noise. Removing any copper beneath the filtering inductors and ferrite beads minimizes leakage through parasitics, and extending the ground plane on the bottom layer of the printed circuit board creates a Faraday cage.

Enhanced system durability and reliability

High-power systems operate in electrically noisy and physically harsh environments. Bias supplies must maintain stable operation despite fast switching transitions, strong magnetic fields, and mechanical vibration. Integrated bias-supply modules with IsoShield

technology address these challenges through several immunity mechanisms.

CMTI

Fast switching transitions in modern power stages, especially those using wide bandgap devices, can produce voltage slew rates exceeding hundreds of volts per nanosecond. Isolation barriers with large parasitic capacitance may couple these disturbances across the barrier.

Modules with IsoShield technology minimize parasitic capacitance between the primary and secondary windings to less than 3pF, enabling common-mode transient immunity (CMTI) of approximately 250V/ns and allowing stable operation in high-voltage slew-rate environments such as traction inverters or motor drives.

Using an integrated solution can significantly de-risk CMTI tests compared to a discrete isolated bias supply because engineers have already completed both device- and system-level testing. CMTI results can vary from application to application when using a discrete solution, whereas an integrated solution produces more consistent results.

Radiated immunity

High-frequency electromagnetic fields generated by nearby switching nodes can disrupt control electronics. Integrated modules with IsoShield technology can withstand strong EMI across a wide frequency range, demonstrating continuous operation in electromagnetic fields exceeding 100V/m across frequencies from 10MHz to 1GHz. These modules meet the requirements of CISPR 25 and exceed limits defined by International Electrotechnical Commission 61000-4-3 without additional shielding or complex filtering.

Magnetic field immunity

High-current conductors, such as bus bars in traction inverters, can generate strong magnetic fields that may affect discrete transformer-based supplies because of their external magnetic structure. Modules with IsoShield technology operate in magnetic fields exceeding 100mT, ensuring stable performance even when located close to high-current power paths or large magnetic structures such as those found in medical imaging systems.

Vibration immunity

Mechanical vibration is a common challenge in automotive and industrial environments. Large discrete transformers can introduce mechanical stress on solder joints and PCB pads, potentially leading to reliability issues. The compact form factor and low profile of integrated bias-supply modules reduce mechanical torque on solder connections >90% compared to discrete transformer implementations, significantly improving vibration tolerance.

Accelerated design cycles

Selecting and designing transformers is one of the most challenging aspects of isolated power-supply development. You must balance numerous design parameters, including winding configuration and routing, leakage inductance and coupling, parasitic capacitances, thermal characteristics, and mechanical packaging. Custom transformer development can add significant design complexity and extend product development timelines.

Integrated bias-supply modules eliminate many of these tasks by combining the transformer, switching FETs and supporting passive components in a single device. This integration reduces component count and simplifies system design. For server power supplies and battery backup units, such a reduction in design complexity significantly shortens time to market.

Conclusion

As power demands continue to rise across applications such as electric vehicles, artificial intelligence-driven data centers, and renewable energy systems, the pressure to deliver higher performance within increasingly constrained form factors is intensifying. Designers are no

longer optimizing for a single parameter; instead, they must simultaneously balance power density, efficiency, reliability, and development speed.

Integrated isolated bias-supply modules based on IsoShield technology fundamentally shift this design paradigm. By embedding the transformer, switching elements and isolation barrier into a compact, optimized package, these solutions eliminate many of the traditional trade-offs associated with discrete implementations, delivering a significant reduction in solution size and complexity along with improved electrical immunity, thermal performance, and reliability.

Equally important, this high level of integration enables faster and more predictable design cycles. Engineers can reuse a substantial portion of existing architectures while reducing the need for custom magnetics and extensive validation, accelerating time to market without compromising performance.

About the authors

Mark Allen Esquillo is a marketing manager in High Voltage Power business covering highly differentiated isolated gate drivers and bias solutions. He has over 30 years of experience across product development, marketing, systems / application engineering and operations. Mark Allen holds a bachelor degree in Mechatronics engineering from Nippon Engineering University in Japan, and Electrical engineering from Mapúa Institute of Technology in the Philippines.

Carter Pollan is an applications engineer at Texas Instruments supporting integrated isolated bias and isolated gate driver applications in automotive and industrial systems. He earned his bachelor's degree in electrical engineering from Brigham Young University.

Realizing 5G network potential through mMIMO and precise beamforming technology

Bhavesh Rathod
Applications engineer
Wireless Infrastructure

Introduction

With every new wireless generation, the demand for higher data rates and lower latency increases substantially. 5G advances this trajectory by delivering tens of gigabits-per-second throughput and submillisecond latency, essential for applications such as augmented and virtual reality, industrial Internet of Things (IIoT), and autonomous systems. Achieving performance targets – especially in dense urban areas and high-mobility scenarios – requires two technologies: massive multiple-input multiple-output (mMIMO) and beamforming.

5G mMIMO systems use large antenna arrays, typically ranging from 16 transmit antennas and 16 receive antennas to 128 transmit antennas and 128 receive antennas. These antennas enable spatial multiplexing, transmitting multiple data streams simultaneously over the same frequency in order to enhance spectral efficiency and user capacity without additional bandwidth or power.

Beamforming, implemented through phased array antennas, enables spatial filtering to steer and focus radio-frequency (RF) energy toward intended users, mitigating interference and improving the signal-to-noise ratio. Beamforming requires consistent phase alignment across antennas. It enhances performance at higher RF frequencies (the FR1 and FR2 bands, for example), where free-space path loss and signal blockage are significant challenges.

To overcome these challenges, 5G mMIMO combined with beamforming enables high-throughput, low-latency communication and ensures scalability. These combined technologies empower network operators and developers to create innovative wireless applications for increased frequency bands through precise antenna control.

Realizing mMIMO and beamforming requires the use RF transceivers to convert bits to RF and vice versa. Because both mMIMO and beamforming require spatial and timing accuracy, the bits-to-RF conversion process of the RF transceiver must have a precise time stamp and time synchronization across multiple antennas.

Radio equipment with a 5G-capable RF transceiver enables the radio to operate in both 4G and 5G. According to 3rd Generation Partnership Project (3GPP) specifications for 5G, 5G improves 4G in these specific areas:

- Enhanced mobile broadband (eMBB)
- Critical communication (CC) and ultra-reliable low-latency communication (URLLC) for industrial applications
- Massive Internet of Things (mIoT).
- Flexible network operations to enable adaptability and network optimizations while supporting diverse applications and end-user needs through network slicing, cloud-native infrastructures and software-defined networks.

What is 5G mMIMO?

5G MIMO is the wireless communication technology used in 5G network systems. A typical MIMO radio may have between 16 and 32 transmit and receive antennas compared to mMIMO's 64, 128 or even more antennas in a single radio unit. Packing these many antennas into a single radio unit helps serve more users with higher data rates.

mMIMO-based 5G network support for spatial multiplexing enables a substantial increase in channel capacity without adding any extra bandwidth or transmit power.

As the industry moves toward higher 5G frequencies such as millimeter wave (mmWave) (from 24GHz to 40GHz), beamforming becomes even more important. mmWave frequencies make it possible to have a high number of antennas in a constrained space because the antenna sizes are small. mMIMO proves to be a blessing in disguise, as it not only enhances throughput and coverage but also enables support for multiple users at the same time without having to add more resources (bandwidth, power, radios). This makes 5G mMIMO an essential technology required for achieving higher data rates, ultra-low latency and the massive connectivity targets defined by 3GPP for 5G networks.

5G mMIMO and beamforming

Beamforming is one of the primary technologies required for 5G wireless communication systems. 5G ultrawide-band frequencies operate in the sub-6GHz frequency range and mmWave frequency bands. This spectrum of frequencies is susceptible to higher signal attenuation and interference from objects in its path, and mmWave cannot penetrate walls as easily as 4G. Thus, 5G requires beamforming in order to focus power in a specific area to achieve high data rates, especially in dense urban deployments. See **Figure 1**.

Another benefit of beamforming is maintaining connectivity with mobile targets such as moving vehicles using beamsteering and beamtracking as defined in the 3GPP releases. Beamforming can be either digital, analog or hybrid beamforming architectures. Let's look at the math behind this technology.

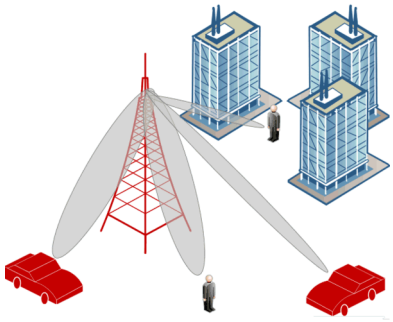


Figure 1. *How beamforming helps connect more people over a 5G network in a densely populated urban area.*

The math behind beamforming

Equation 1 models signal propagation over a channel, **Equation 2** shows the detailed H matrix. Each element h_{mn} in matrix Hrepresents the complex gain from each transmit antenna n to each receive antenna m. where ρ is the signal at the receiver, τ is the transmitted signal and the matrix H is the channel characteristics matrix. Matrix H represents the gain and phase response of every channel.

$$\rho = H \times \tau \tag{1}$$

$$\rho = \begin{bmatrix} h_{11} h_{12} \cdot \cdots h_1 n \\ \vdots \\ \vdots \\ \vdots \\ h_{m1} h_{m2} \cdot \cdots hm_n \end{bmatrix} \tau \tag{2}$$

Under linear precoding, **Equation 3** calculates the transmit signal τ as:

$$\tau = \Sigma w \times s \tag{3}$$

where s is the symbol being transmitted and w is the linear precoding vector.

The precoding vectors determine the direction of the beam by adjusting the relative phase difference of each transmit channel.

To calculate the precoding vectors, estimate the H matrix. It is important that each transmitter has a deterministic relative phase difference; otherwise the estimated H matrix and the calculated precoding vectors will not hold true. Beamforming relies on the phase accuracy of transmitted signals to constructively combine them at the receiver.

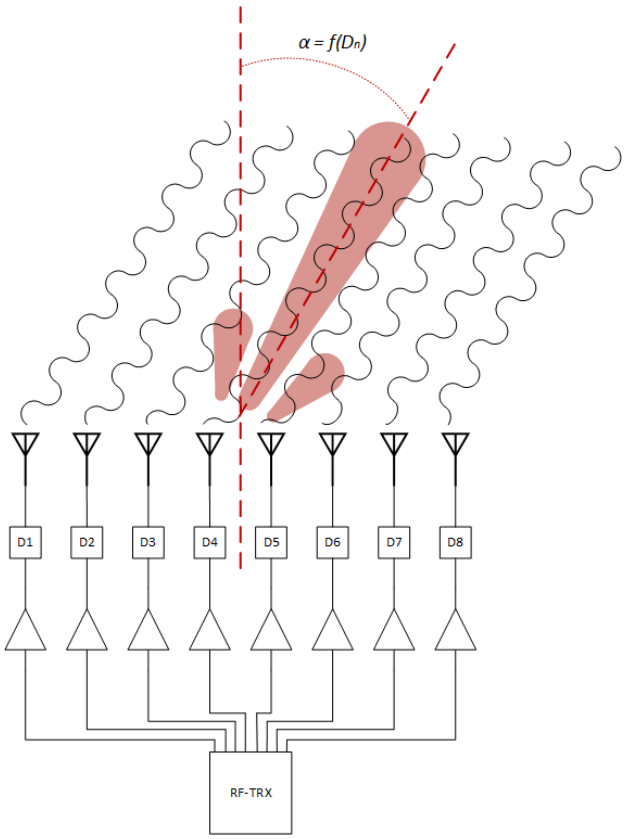


Figure 2. *A beam formed (using an eight-channel transceiver) by adjusting the phase between time-synchronous antennas.*

Synchronizing the output phases of multiple transmits from one mMIMO becomes tricky when there are multiple analog front-end devices on the radio unit. A 128-antenna mMIMO system would have eight- to 16-channel analog front-end devices.

Current challenges for mMIMO systems

In a typical 5G mMIMO transceiver, a single board houses multiple RF transceivers. For a 64-channel configuration, the board can be populated with eight 8 channel transceivers or four 16-channel transceivers. Reliable beamforming requires that all transmit and receive paths remain phase-synchronized throughout the entire system life cycle, including initial bring-up, subsequent JESD204B and JESD204C link reinitializations between the analog front end and application-specific integrated circuit (ASIC) or field-programmable gate array (FPGA), and power-on resets. This is a fundamental challenge that all radio system designers face. The deterministic relative phase relationship ensures that the composite antenna array forms and steers beams predictably.

Exploiting the internal phase-shift capability of the numerically controlled oscillator (NCO) embedded in the transceiver can compensate only for any residual static phase offset that exists across the multielement antenna array. Because this offset remains invariant across bring-up cycles, JESD relink events and power cycles, a one-time NCO calibration will align the phases of all channels and thereby preserve beamforming performance. But the fundamental need for all RF transceivers on the radio to be time-synchronized remains.

TI's AFE80xx and AFE81xx families of RF integrated circuits include several features to help designers achieve mMIMO requirements.

Using single-shot sysref mode

The default mode of operation in most systems is continuous sysref mode, where sysref is a periodic low-frequency signal. But it is possible to achieve multidevice synchronization using the "single-shot" system reference clock (sysref) mode in the AFE8092, AFE8030, AFE8128, AFE8190, AFE8192. In single-shot mode, the sysref signal is a single pulse, which is given simultaneously to all analog front ends on the board. When all of the analog front ends receive sysref at exactly the same instant with regards to the reference clock, they naturally become phase-synchronized.

One of the challenges in implementing this method is how to achieve differential routing of the sysref and reference clock to multiple devices on the board. At the

radio level within the printed circuit board, you need to preserve the timing of sysref and reference clock routing to the picosecond level with respect to the reference clock.

As shown in **Figure 3**, single-shot sysref mode using the AFE8092, AFE8030, AFE8128, AFE8190, and AFE8192 require a specific sequencing.

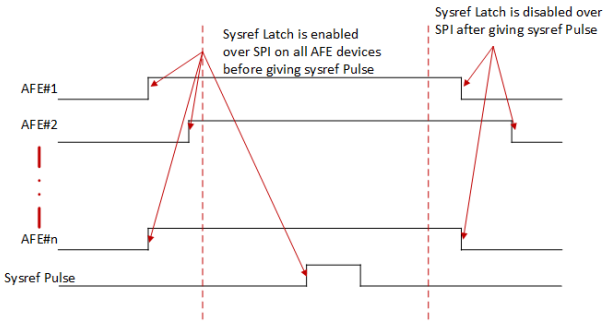


Figure 3. *Timing diagram for single-shot sysref mode.*

Using a common time-stamp signal through GPIO to time-align the RF integrated circuit

It is also possible to use general-purpose input/output (GPIO)-based control to enable sysref latch. In this mode, the sysref can operate in continuous sysref mode. All analog front-end devices will latch to the first reference clock rising edge after receiving a GPIO-based latch enable signal. All subsequent pulses will be ignored.

This approach only requires routing a CMOS GPIO signal to all of the analog front ends, which makes this method relatively simpler to implement compared to the single-shot sysref method, as it can be challenging to route a differential signal to multiple analog front-end devices on the board with matched lengths. At the same time, this approach requires synchronizing one GPIO per device from the host's ASIC. The method is not suitable if the host ASIC or FPGA does not have enough GPIOs.

As shown in **Figure 4**, using GPIO-based control to enable sysref latch with the AFE8092, AFE8030, AFE8128 AFE8190, AFE8192 require a specific sequencing.

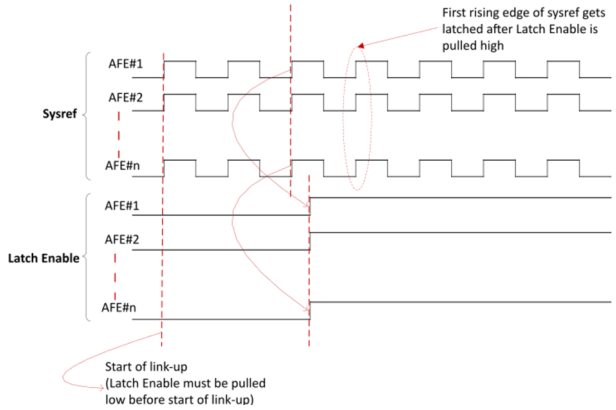


Figure 4. *Timing diagram of using GPIO-based control to enable sysref latch mode.*

NCO selection

The simplest way to achieve phase synchronization is to choose transmitter and receiver NCOs that are integer multiples of the sysref frequency. This method works even for continuous sysref modes, as it does not need any extra mechanism to synchronize the NCOs for transmit and receive across multiple analog front-end devices.

This method is most suitable if the restriction put on NCO frequency is acceptable for the end application, as you can achieve phase synchronization with no change to existing hardware. You will need to follow a specific software sequence in the case of a relink or power cycle of the analog front-end devices. **Figure 5** shows how in this mode, it would not matter even if all analog front ends latched to different sysref edges.

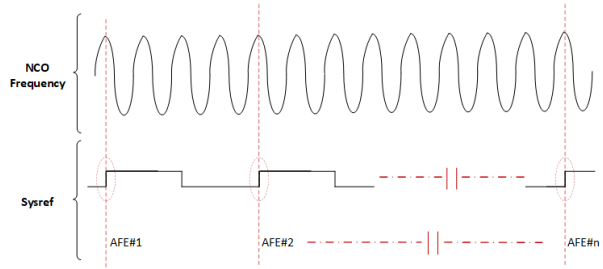


Figure 5. *Example illustrating how the NCO frequency equals four times the sysref frequency.*

Conclusion

The integration of mMIMO and beamforming technologies is pivotal to unlocking the full potential

of 5G networks, enabling unprecedented data rates and ultra-low latency. By leveraging large antenna arrays and precise spatial filtering, these technologies overcome the challenges of high-frequency signal propagation, ensuring reliable and high-throughput communication in diverse scenarios. As outlined in the 3GPP specifications, 5G's enhanced capabilities in eMBB, CC, URLLC, mIOT and flexible network operations are largely attributed to the synergistic effects of mMIMO and beamforming.

TI's AFE8092, AFE8030, AFE8128 and AFE8190, AFE8192 transceivers can help network operators support a range of wireless applications, from augmented and virtual reality and IIoT to autonomous systems and beyond.

About the Author

Bhavesh Rathod is an applications engineer at Texas Instruments, specializing in RF applications and wireless infrastructure solutions. Bhavesh brings hands-on expertise in post-silicon validation and embedded systems to support the development of cutting-edge wireless infrastructure technologies. He received an M.S. in electrical and computer engineering from Purdue University, and a bachelor's degree in electrical engineering from the College of Engineering Pune. Bhavesh was recognized with the Gandhian Young Technological Innovation Award in 2017 for his work on Swayam, a passively stabilized communication satellite.

Selecting precision op amps as ADC drivers

Soufiane Bendaoud, senior business development manager
Texas Instruments

Selecting an operational amplifier (op amp) to drive an analog-to-digital converter (ADC) is not a trivial task. Usually dictated by the end equipment, the choice of ADC is based on trade-offs of several parameters. Even within the same sector or market segment, ADC requirements can differ. For example, in test and measurement you will find a mix between successive approximation register (SAR) and delta-sigma ADCs. SAR ADCs tend to be popular in parametric measurement units, memory testers and battery cell formation testers.

Delta-sigma ADCs are typically used for vibration analysis, data acquisition and scientific instrumentation. Some applications can be common to both, depending on the overall system requirements. Highly accurate weigh scales benefit more from delta-sigma ADCs given their higher resolution, whereas consumer and low-end models rely on the SAR topology to minimize power consumption.

Likewise, datacom optical modules tend to use SAR ADCs whereas telecom optical modules often rely on delta-sigma ADCs even though both applications are part of the same sector, namely data centers.

Paying careful attention to the DC and AC specifications of the op amp (or analog front end) can help avoid ADC performance degradation and minimize errors.

Circuit configuration vs. bandwidth and other errors

An inverting circuit configuration provides the advantage of avoiding common-mode modulation errors and therefore does not require a high common-mode rejection ratio. It lowers the input impedance to the parallel combinations of input and feedback resistors, however, and induces gain error with the feedback resistor in place. A noninverting configuration typically provides much higher input impedance. The closed-loop bandwidth or effective bandwidth of the op amp is a function of the noise gain (or noninverting gain), not the signal gain.

In **Figure 1**, TI's OPA325 has a gain bandwidth product of 10MHz. In a positive unity gain (buffer) configuration, the bandwidth is 18MHz. The excess bandwidth is attributed to the gain peaking, accounted for in the TINA-TI™ macromodel by the input capacitance and open-loop output impedance. In this case, the signal gain is –1 and the noise gain is 1.

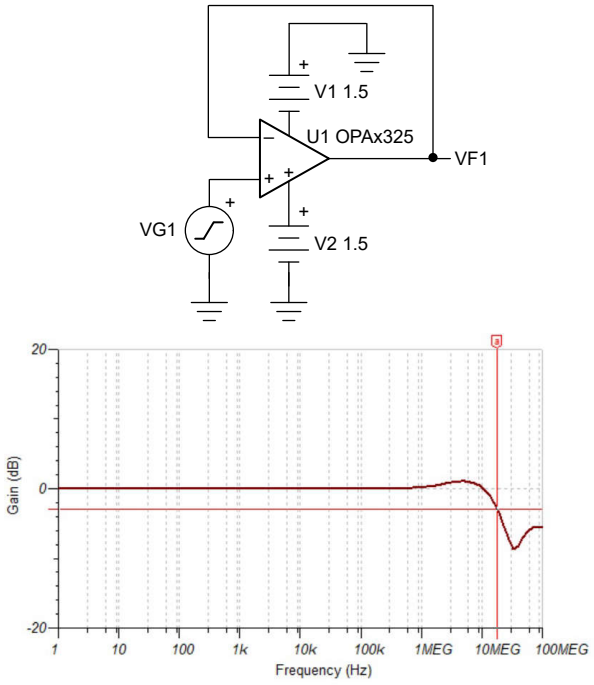


Figure 1. *The OPA325 in a buffer configuration*

On the other hand, the circuit shown in **Figure 2** exhibits a bandwidth of 6.7MHz, nearly one-third the bandwidth of the buffer in **Figure 1**. In **Figure 2**, the signal gain is –1 but the noise gain is 2. Notice that the gain peaking isn't nearly as noticeable in the inverting configuration, even with a gain of just 2. The higher the gain, the lower the gain peaking.

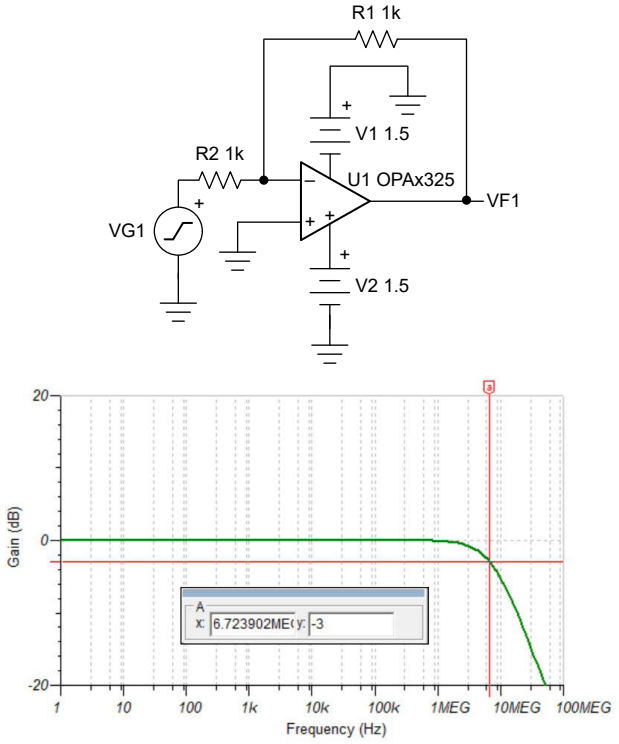


Figure 2. *The OPA325 with a noise gain of 2*

DC gain error

Open-loop gain (Aol) plays a major role in DC gain accuracy. If you consider the inverting circuit in Figure 2 in a 12-bit system, the Aol must be at least 78dB or 8,192; that is, 212 × 2. Almost all modern general-purpose op amps can achieve 78dB of Aol. If you require 16 bits of accuracy (at a noise gain of 2), the minimum Aol must be 102dB, which requires a precision device in most cases. Remember that Aol is also a function of the output load, since the gain of the last stage is a function of gm × RL. In the case of the inverting circuit, the feedback resistor (R1 in Figure 2) is the load.

Output limitations and linearity

Op-amp specification tables list the output swing, typically in the range of 10mV to 20mV for complementary metal-oxide semiconductors (CMOS) from the power supply, commonly known as the slam test. To ensure that the op amp stays within the linear region, look at the conditions of the Aol specification to determine the allowable maximum voltage swing. Since ADCs have a high input impedance, look at the highest-value load condition.

For example, the OPA328 has a voltage output swing of ±100mV with a 10kΩ load. When paired with the ADS8860 using a single-supply 3.3V, the linear range of the OPA328 is from 0.1V to 3.2V, whereas the ADS8860 has an input range of 0V to 3.3V. Clearly, you're not using the full dynamic range, thus resulting in a waste of codes. Using the LM7705 negative bias generator (–0.23V) and increasing the positive power supply to 3.5V will overcome this issue. With the OPA328 output limitation of ±100mV and the LM7705 in place, the valid output range is now –0.1V to 3.4V, which covers the ADS8860 input range without violating its absolute maximum ratings (–0.3V to 3.6V).

Noise and ENOB

When it comes to driving high-resolution ADCs, op-amp noise plays a crucial role. A low-noise amplifier will help achieve a higher effective number of bits (ENOB) for the total system. In other words, the lower the op-amp noise, the smaller the degradation of the ENOB, and the higher the accuracy. Remember that low-noise amplifiers typically require a higher quiescent current, which in turn is proportional to bandwidth expressed as:

$$\mathrm{BW} = \frac{\mathrm{gm}}{2\pi \mathrm{Cc}} \quad (1)$$

For the same amount of current, a bipolar op amp achieves wider bandwidths (or in other words, is more efficient).

Equation 2 expresses the total noise calculation, including the voltage reference, as:

$$V_{ntotal} = \sqrt{V_{nADC}{}^2 + V_{nopa}{}^2 + V_{nref}{}^2} \quad (2)$$

Starting with the ADS8860, converting the full-scale range (5V) to root mean square (RMS) values using 5 / (2 × √2) yields 1.76V. **Equation 3** computes the rms noise of the ADS8860 as:

$$V_{nADC} = \frac{V_{FSR\_rms}}{10\left(\frac{SNR_{ADC}}{20}\right)} = \frac{1.76}{10\left(\frac{93dB}{20}\right)} = 39.6\mu Vrms \quad (3)$$

Simulating the OPA328 in a positive unity gain yields a total noise of 47µVrms and about 83µVrms in an inverting gain of 2 (noise gain). **Figure 3** and **Figure 4** show the respective simulation results.

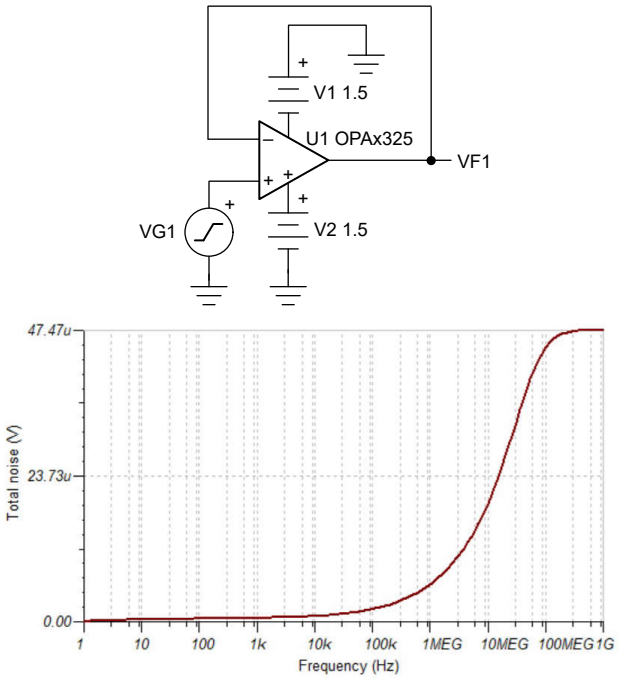


Figure 3. *The OPA328's RMS noise in a positive unity gain*

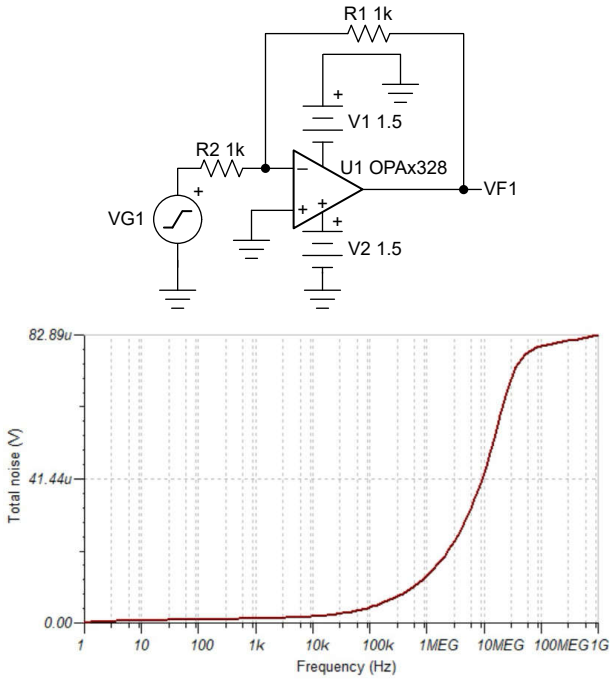


Figure 4. *The OPA328's RMS noise in an inverting configuration*

Using the OPA325 in the same circuits yields 39µVrms and 55µVrms, respectively.

While it may seem a natural choice to select the lowest noise op amp, you must remember that a low-noise amplifier is only as good as its bandwidth in terms of noise. In other words, the OPA328 with 6nV/√Hz exhibits about 20% higher noise than the OPA325, which has 9n/√Hz of broadband voltage noise density. OPA328 has four times the bandwidth of the OPA325.

Simulating the total noise (RMS) is a crucial piece of your analysis and an easy way to achieve a better ENOB for the system.

For example, in the noise plot of **Figure 5** to reduce the noise to the one-half least significant bit (LSB) of the 39µV from the ADS8660, you need to limit the bandwidth to about 2MHz.

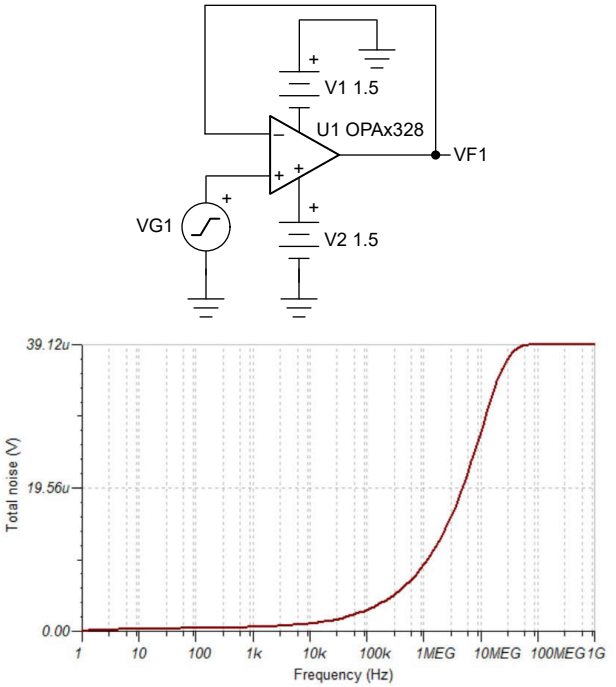


Figure 5. *The OPA325 RMS noise in a positive unity gain*

Figure 6 shows the rms noise simulation of the OPA325 in an inverting configuration.

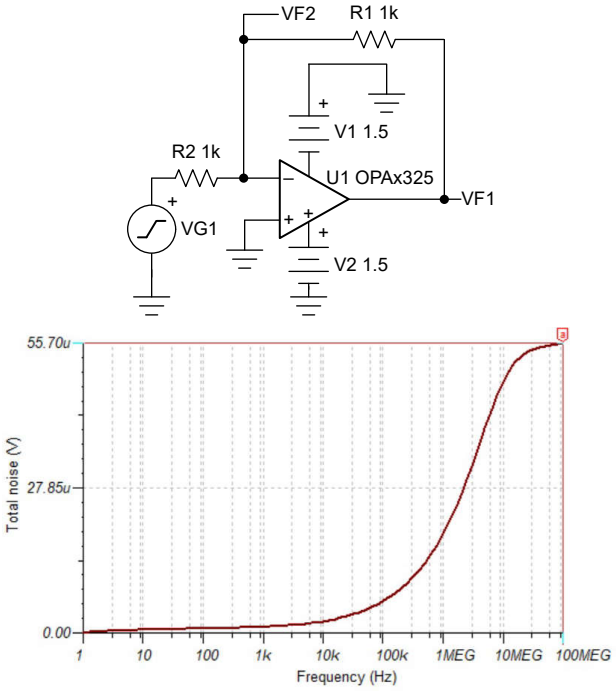


Figure 6. *The OPA325 RMS noise in an inverting configuration*

Figure 7 shows the REF7050 total noise (RMS) of about 2.2µV and has very little impact on the total system noise. Including it in **Equation 2** yields a total noise of 55.7µV. If you neglect the voltage reference noise, Equation 1 gives you 55.6µV. If you limit the OPA325 bandwidth to 2MHz, the noise is about 18µV and the total system noise is 43µV, clearly dominated by ADS8860 noise.

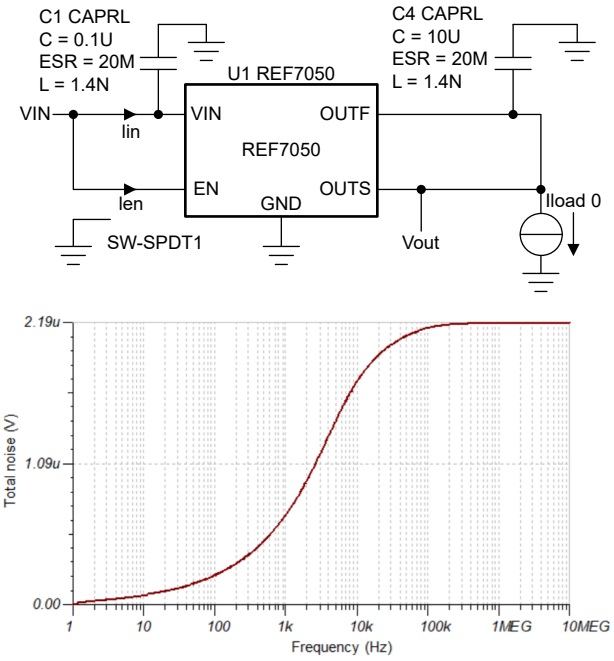


Figure 7. *REF7050 RMS noise*

Equation 4 expresses the total signal-to-noise ratio (SNR) of the system as:

$$\mathrm{SNR_{total}} = 20\ \log\left(\frac{\mathrm{V_{FSR_{rms}}}}{\mathrm{V_{ntotal}}}\right) \quad (4)$$

With a total noise of 55.6µV, the total SNR is 90dB. With the OPA325 bandwidth filtered to 2MHz, the total SNR is 92.2dB, a degradation of less than 1dB from the original SNR of the ADS8860, 93dB.

Input offset voltage and drift

The offset voltage of the op amp is a source of error and affects system accuracy. With a 5V full-scale voltage range, the quantization error for the ADS8860 (16 bits) is $5/(2^{16} + 1)$, which is 76µV. To avoid quantization errors and maintain system accuracy, target one-half LSB, or 38µV. While you can calibrate the input offset voltage out,

offset drift involves more complex calibration methods. Applications such as automotive and downhole drilling require much higher temperatures than lab and field instrumentation, test and measurement, and medical instrumentation. Modern high-precision op amps using techniques such as zero drift or e-trim™ offer the advantage of very low offset voltage and drift, well below the desirable LSB size, and help achieve higher system accuracy.

Table 1 lists a few precision op amps from TI with various technologies.

Devices	Technology	Vs (V)	Vos max (µV)	TCVos, typical (µV/°C)	Bandwidth (MHz)	Broadband voltage noise (nV/√Hz)
OPA392	e-trim™	1.7-5.5	10	0.18	13	4.4
OPA325	Laser trim, zero crossover	2.2-5.5	150	2	10	9
OPA328	e-trim™, zero crossover	2.2-5.5	50	0.15	40	6.1
OPA383	Zero drift	2.7-5.5	5	0.025	2.5	32
OPA192	e-trim™, multiplexer friendly	4.5-36	25	0.1	10	5.5

Table 1. *Low noise precision op amps for driving high resolution ADC'S*

Settling time

A wide bandwidth amplifier with a high slew rate, low output impedance and high phase margin settles faster. When driving the ADC, select an op amp with a settling time to the required resolution that matches the ADC acquisition time. Remember that the acquisition time is the sampling time minus the conversion time. Slowing the sampling rate down helps you relax the op-amp settling-time requirement.

Ideally, the op amp should settle within one-half LSB of the ADC to avoid errors. However, very few op-amp datasheets specify settling time up to 16 bits (0.0015%). One often-overlooked specification is the open-loop output impedance. A low open-loop output impedance means a higher phase margin, which in turn means a faster settling time. Furthermore, the shape of the open-loop output impedance affects circuit stability. A flat (resistive) open-loop output impedance op amp is much easier to compensate. A charge bucket resistor-capacitor filter at the output of the op amp creates a pole and degrades the phase margin but minimizes output voltage droop during the sampling time. Depending on the pole location, you may see excessive ringing (overshoot), which affects the settling time.

Figure 8 shows a circuit using the OPA328 to drive the ADS8860. The sampling rate is set at 500kSPS. The acquisition period of the ADS8860 is Tacq = 2µs – 710ns = 1,290ns.

Lowering the sampling rate to 500kSPS allows the circuit to settle much faster at 425ns, well below one-half LSB.

Figure 9 shows the OPA328 paired to the ADS8860 and uses the circuit to simulate the settling time (**Figure 10**).

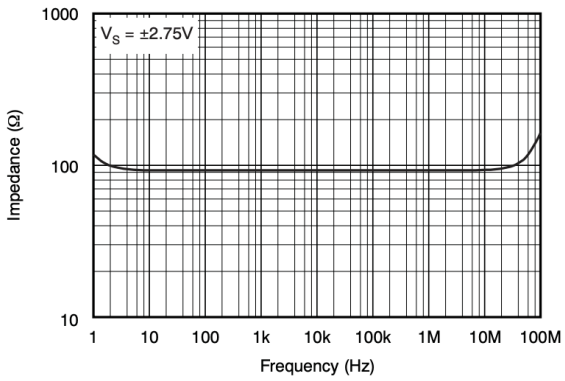


Figure 8. *OPA320 open loop output impedance vs. frequency*

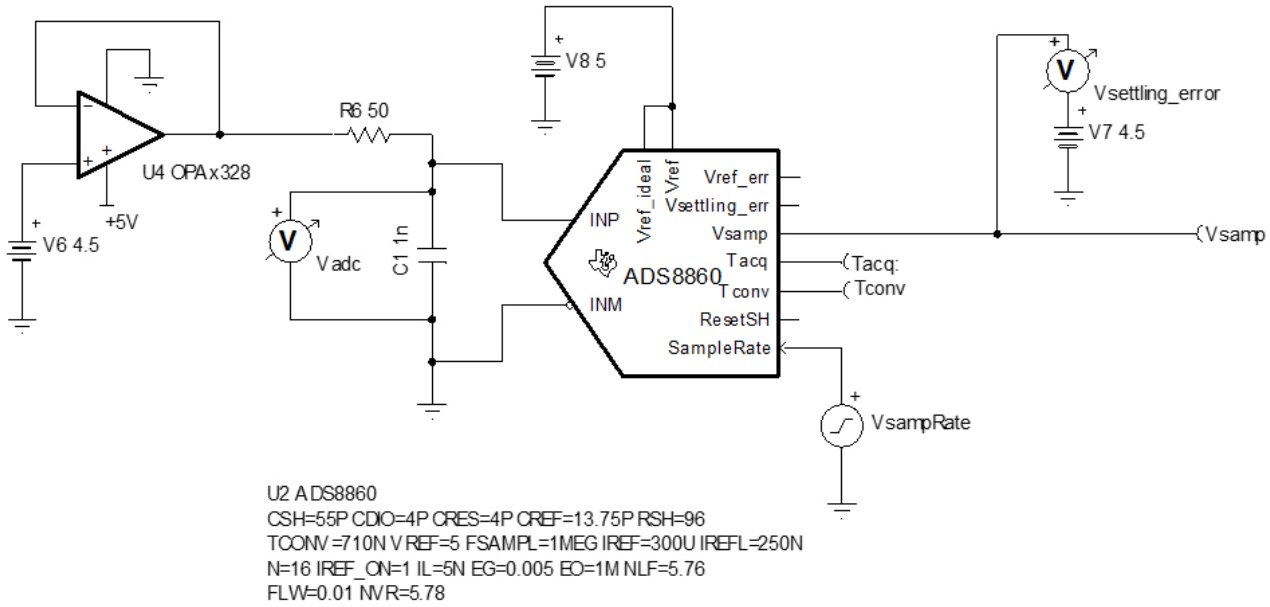


Figure 9. *OPA328 driving the ADS8860*

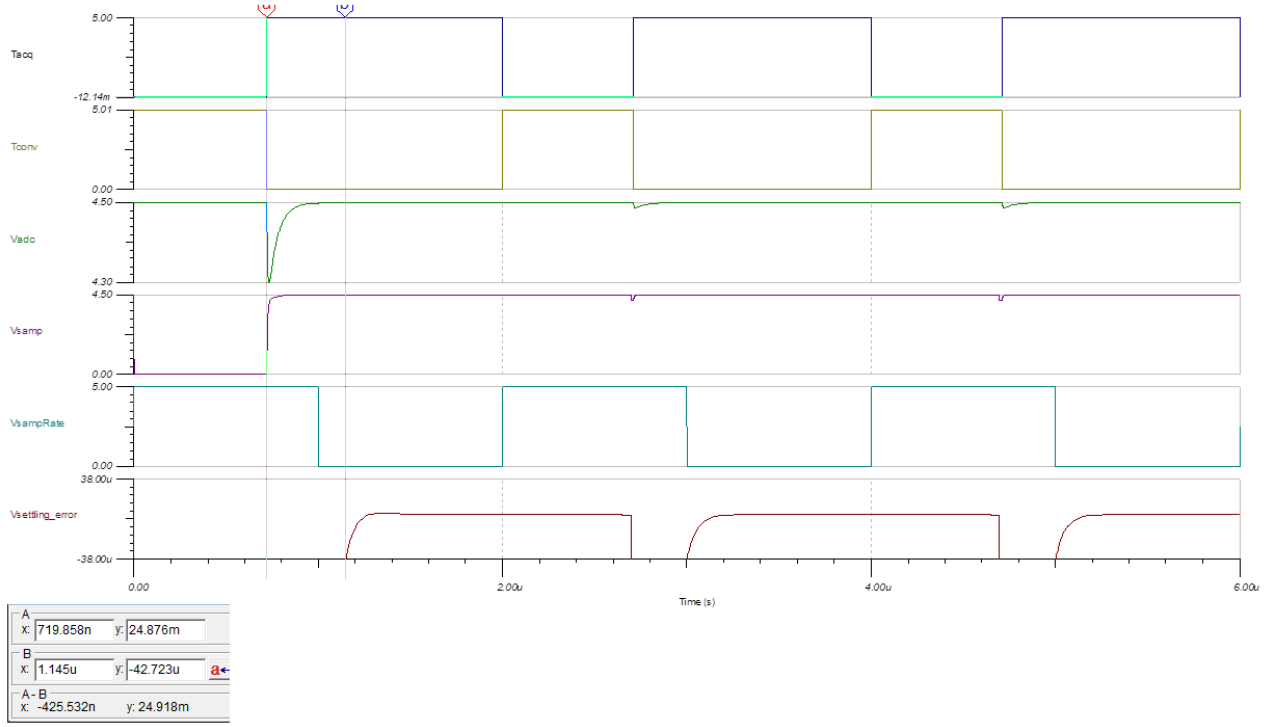


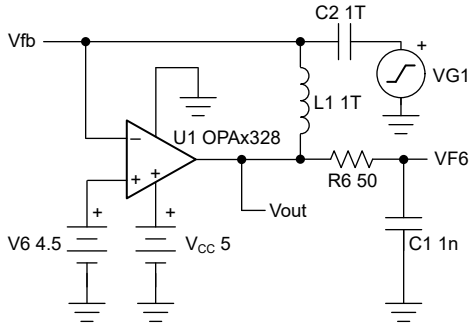
Figure 10. *OPA328 settling time driving the ADS8860*

Stability

Optimizing the circuit for settling time and noise performance must not come at the expense of stability. The op amps discussed throughout this article have a low, flat open-loop output impedance, which makes compensation much simpler.

Figure 11 shows the OPA328 driving a 1nF capacitor with an isolation resistor outside the feedback loop of 50Ω, the same one used to drive the ADS8860. The phase margin is 61 degrees, guaranteeing stability for a reliable design.

Op-amp stability is paramount. If the op amp is unstable or on the verge of becoming unstable, with severe ringing and overshoot, nothing else matters.



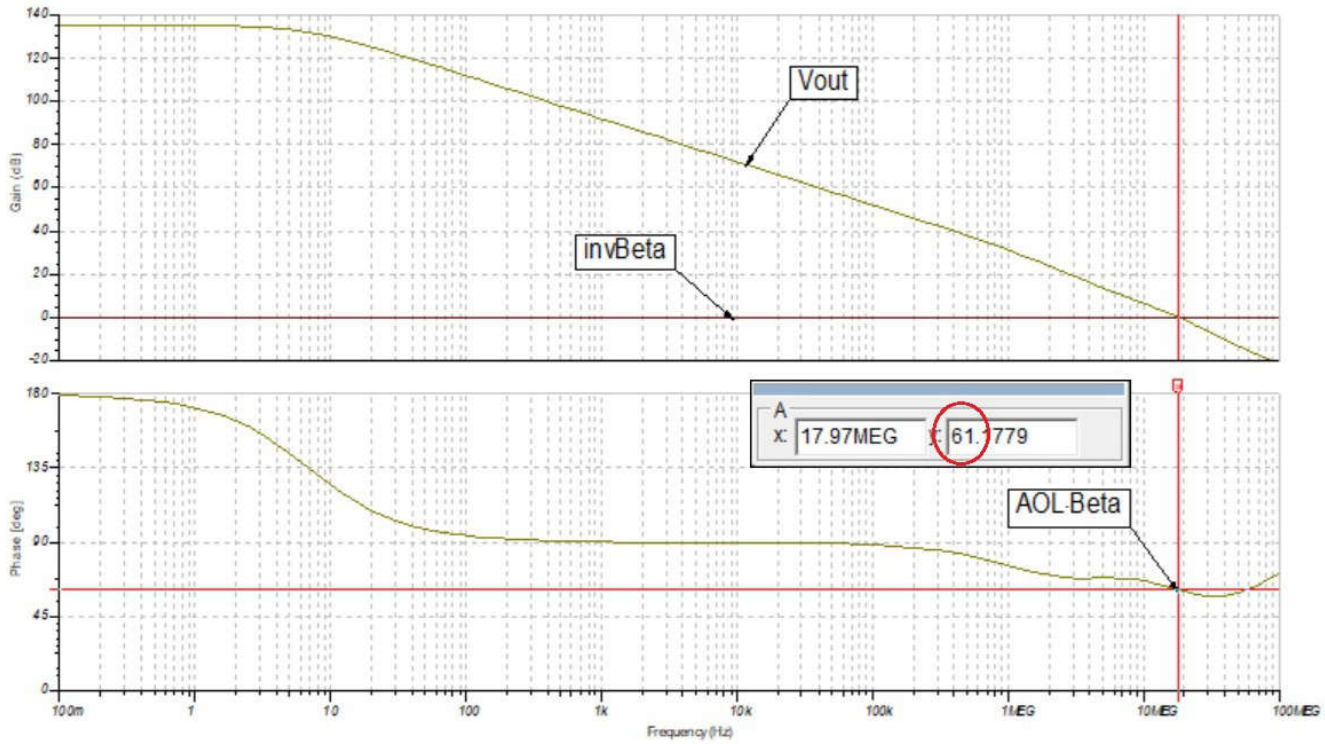


Figure 11. *OPA328 open loop gain and phase margin with a heavy capacitive load*

Conclusion

The choice of op amp as an ADC driver starts with the application. Portable equipment for test and measurement, medical apparatuses and barcode scanners all rely on low power consumption, whereas gas exploration, displacement measurement and semiconductor test equipment require higher resolution and therefore low-noise precision op amps. There is no panacea when it comes to op-amp selection for a given ADC; rather, there are optimization schemes for one aspect over others.

About the author

Soufiane Bendaoud is business development manager for precision amplifiers at Texas Instruments, with more than 25 years of analog signal chain expertise. He has authored more than 60 technical articles, application notes and papers, and regularly provides technical training to engineers around the world.

How to cut PLC output power dissipation in half using an adaptive supply

Ahmed Noeman, systems engineer, precision amplifiers

The 4-20 mA current loop is a common signaling scheme for control systems. Field transmitters send sensor readings as 4-20 mA signals, and programmable logic controller (PLC) 4-20 mA outputs control many actuators. Increased channel count for PLC modules is a major industrial trend but creates a challenge for PLC current output modules because of power dissipation.

The output stage of the PLC current output channel shown in **Figure 1** is powered by a supply voltage (VS) and connected to an external load (RL). If the maximum RL specified is 800Ω and the assumed headroom voltage (VH) is 4V, for driving 20mA, Vs needs to be ≥20V.

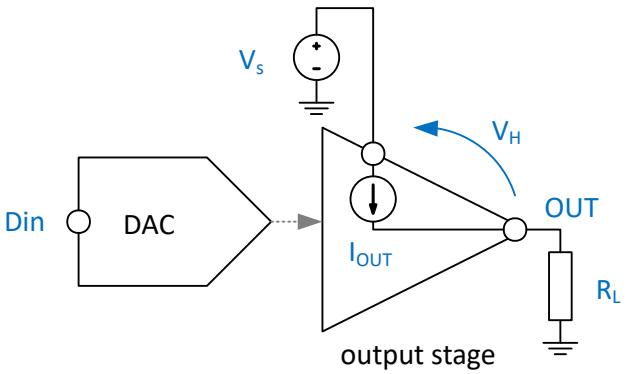


Figure 1. *Power losses at the output stage.*

If you connect the same module to a small load or short circuit, the power loss within the channel will be VH × 20mA = 0.4W. This is quite high. Many modules limit the maximum load to 600Ω to reduce overall power losses. Derating the module output is another approach that manufacturers use, where the ambient temperature determines how many channels the user can enable, and the maximum current in each.

Equation 1 calculates power loss in the output stage.

$$P_{loss} = I_{OUT}(V_s - R_L I_{OUT}) \quad (1)$$

Note

The most convenient approach to adaptive power is to use a DAC that intrinsically supports adaptive power and integrates the output stage. TI's one-channel DAC8771 and four-channel DAC8775 integrate a buck-boost converter per channel with VS between 12V and 36V, generating both negative and positive variable supplies (with a maximum span of 36V) using a single external inductor per channel.

Choosing the right DC/DC

Finding the proper DC/DC converter for adaptive power is challenging because of these requirements, which are contradictory:

- High efficiency at low loads (4-20 mA). Because this is generally possible in pulse frequency modulation (PFM), the DC/DC has to support this mode. Expect an approximate 50% efficiency improvement vs. forced pulse-width modulation (PWM) mode.
- Relatively high peak current (>0.5A) for fast settling. The peak current divided by the decoupling capacitances determines the output maximum voltage rate of change.
- VOUT within 4V to 24V, achieved by either a buck or boost converter based on the input voltage.
- A relatively small inductor to reduce solution size. A high switching frequency (≥300kHz) is required.
- Available in a small package.

Some parts that fulfill these requirements are:

LMR516xx: 65V input, PFM versions at 400kHz/1.1MHz, 0.6A/1A output current

LMR544xx: 36V input, PFM at 1.1MHz, 0.6A/1A output

LMR3650x: 3V-65V input, adjustable 200kHz-2.2MHz, 0.1A/0.15A output (if fast settling is not critical)

Controlling the DC/DC output

Nonfixed DC/DC converters use a feedback node kept at a constant reference voltage level through a high gain amplifier. By connecting a resistive potential divider between the converter output voltage and the feedback node, you can control the output voltage, as shown in **Figure 3**.

Because the converter keeps VREF fixed, you can calculate VS using **Equation 2**.

$$V_S = V_{REF}(1 + R_B/R_T) \quad (2)$$

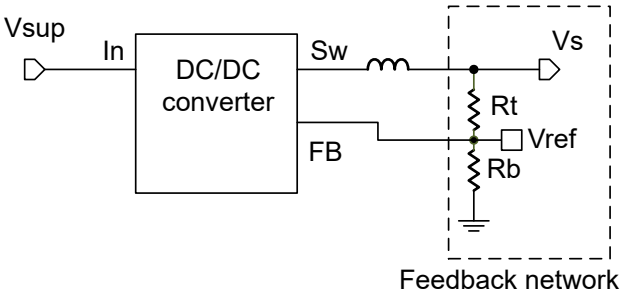


Figure 2. *Feedback network for a DC/DC converter.*

The change of output voltage requires changing the feedback divider. **Figure 3** shows three different ways to change the divider: variable sourcing current (a), variable sinking current (b), or using a variable voltage source and resistor (c). **Figure 3** also shows the transfer function (control variable, current or voltage vs. VS).

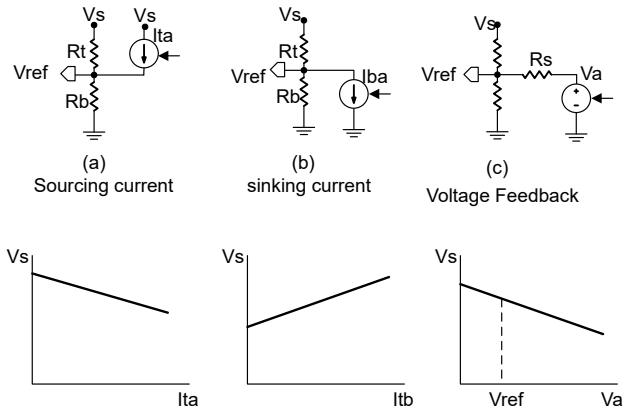


Figure 3. *Adaptive control circuits and their transfer functions.*

Applying Kirchoff's current law on the VREF node in each case yields the transfer function for case a:

$$I_{ta} + (V_S - V_{REF})/R_t = V_{REF}/R_b \quad (3)$$

Rearranging **Equation 3** results in **Equation 4**:

$$V_S = (1 + R_t/R_b)V_{REF} - I_{ta}R_t \quad (4)$$

Equation 5 shows similar calculation for case b:

$$V_S = (1 + R_t/R_b)V_{REF} + I_{ba}R_t \quad (5)$$

Equation 6 calculates case c:

$$V_S = (1 + R_t/R_b + R_t/R_s)V_{REF} - R_t/R_sV_a \quad (6)$$

A simple calculation can find the proper range of the control variable to achieve the required VS range given the reference voltage level present on the feedback pin and the chosen resistor values.

Example circuit using sourcing current

Figure 4 shows the construction of a high-side current source using an operational amplifier, PMOS transistor M1, and a resistor. Equation 8 calculates the current generated as:

$$I_{ta} = (V_S - V_{OUT})/R_c \quad (7)$$

You will need to consider the input/output and supply range of the operational amplifier and the maximum gate-to-source voltage (VGS) of M1. Further simplifying

the circuit by removing the operational amplifier, **Equation 8** calculates the current generated as:

$$I_{ta} = (V_S - V_{OUT} + V_{th})/R_c \quad (8)$$

This saves power, cost and area, with some inaccuracy of current from the variation in threshold voltage (Vth).

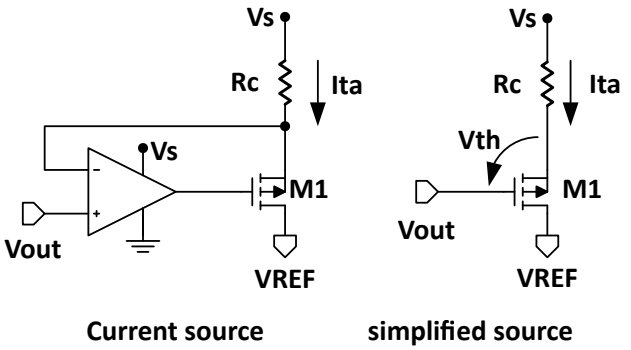


Figure 4. *Current source feedback circuit.*

The TI XTR200 is a 4-20 mA current transmitter with V_S from 8V to 60V and V_H of 3V. If the load is up to 800Ω, V_{OUT} goes up to 16V with 20mA of current. This V_S has to track the output. At V_{OUT} = 0V, V_S = 8V, and at V_{OUT} = 16V, V_S = 19V. Use **Equation 8** and **Equation 5** to calculate resistors Rt, Rb and Rc. You will find that it is not possible to maintain V_H >3V without increasing the headroom for the low V_{OUT}.

Values Rt = 80kΩ, Rb = 3kΩ and Rc = 60kΩ produce the output-supply curve shown in **Figure 5**. Headroom is dependent on the output because this simple design uses only Rc as design variable. More complex circuits can overcome this limitation. But even with this simple circuit, the maximum power dissipation drops to half or less compared to the nonadaptive case. Any low-power rail-to-rail operational amplifier such as the OPA2990 will work in place of U2, as shown in **Figure 6**.

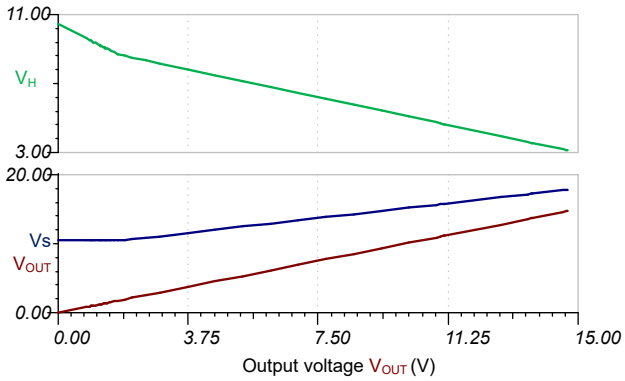


Figure 5. *V_S-V_{OUT}, V_H-V_{OUT} relation.*

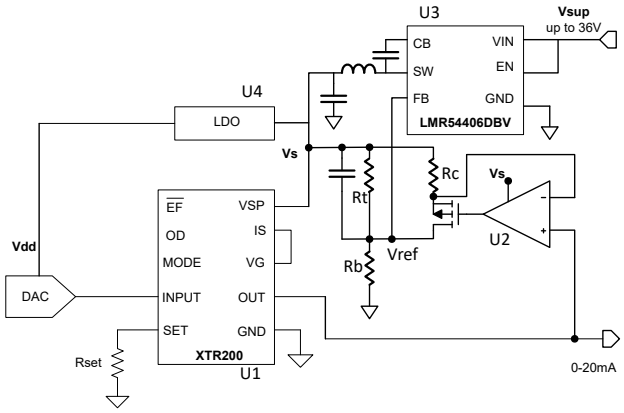


Figure 6. *Output stage using the XTR200 with an adaptive supply.*

Note

Simulation: The switching regulator simulation is quite long. Replacing the DC/DC with a low-dropout regulator (LDO) that has a similar VREF and similar input and output ranges can speed up DC simulation and enable easy creation of the transfer function graph. If the LDO has a different VREF, insert a voltage-controlled voltage source (VCVS) between the feedback node and the LDO's actual feedback node. For example, if VREF = 1.2V, and you want to design for the TI LMR54406 buck converter, which has a VREF = 0.8V, you can add a VCVS with gain of 1.5 to convert the 0.8V into 1.2V.

Example circuit using voltage feedback

For lower VS applications, use the output stage shown in my application note, "**Protected, Low-Noise, Combined V-I Output Stage as Analog Output Building Block**," working down to 5V.

The LMR51606 DC/DC simplified circuit shown in **Figure 7** omits the input capacitance and electromagnetic interference protection filters. The buck converter uses a small inductor (L1 = 15µH) and output capacitance (22µF) optimized to provide low ripple and enable fast supply ramping.

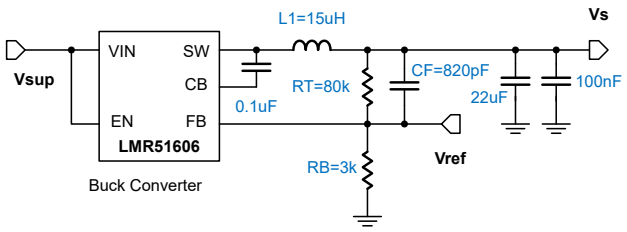


Figure 7. *DC/DC circuit.*

Use **Equation 2** to calculate the values of Rt and Rb so that Vs = 20.8V when no current is injected into the feedback node so that these values set the maximum supply level.

To achieve better efficiency, the difference amplifier shown in **Figure 8** senses the output headroom, where $V_H = V_S - V_{OUT}$. The difference amplifier has a gain of 0.33V/V so that the steady-state headroom is between 3V and 2.7V based on V_S. The 1MΩ input impedance reduces error on the output current to <0.1%. It is possible to compensate for this error during calibration.

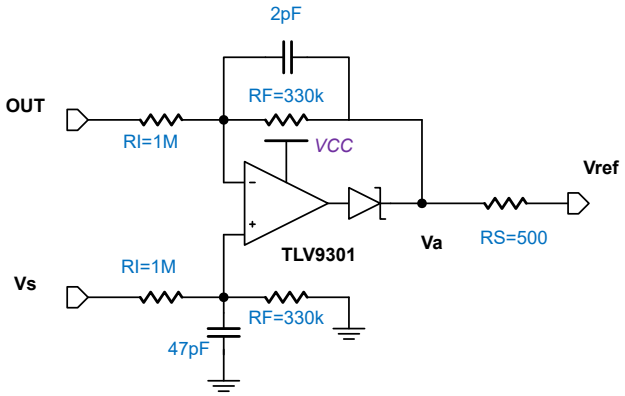


Figure 8. *Difference amplifier.*

The diode at the operational amplifier output prevents turning sourcing current into sinking, so if the operational amplifier output has a lower voltage than the feedback node, the loop will break. This keeps the upper limit of the VS set by Rt and Rb. The capacitors in the feedback path are essential for dynamic stability of the larger loop, including the DC/DC.

Figure 9 is a simplified overall circuit.

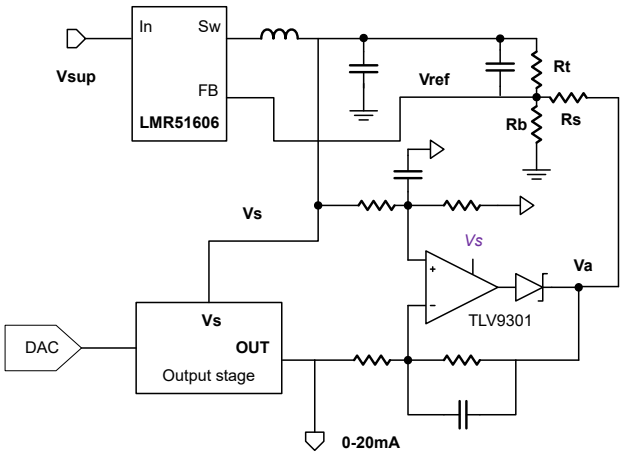


Figure 9. *Simplified schematic for adaptive power with a difference amplifier.*

Note

Dynamic performance: The output stage response to a DAC output change is typically fast. In contrast, the DC/DC is much slower, and the V_S cannot follow the output at the same pace. Limiting the difference amplifier bandwidth helps smooth this change and allows the converter to ramp properly. In addition, it is necessary to limit the slew rate of the DAC output if it doesn't inherently support slew-rate control. You will have to divide large DAC code changes into smaller changes over a longer period, creating a staircase DAC output that allows the DC/DC converter to settle without overshoot or oscillation.

Measurements and performance

Figure 10 shows the power losses for different output currents as well as various loads. Power losses are calculated as the input power to the DC/DC converter minus the output power to the load. The power losses never exceed 180mW, which translates to >50% of power savings.

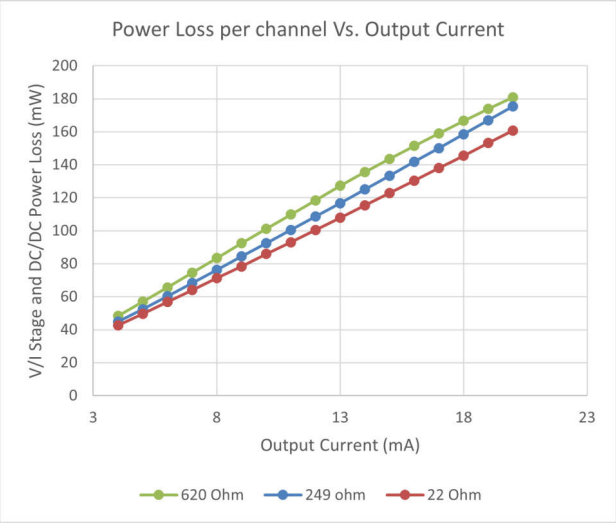


Figure 10. *Power losses vs. output current.*

Figure 11 shows the efficiency for different currents and loads. The efficiency of the DC/DC converter is calculated as the output power from the converter divided by the input power. The efficiency ranges between 75% and 90%.

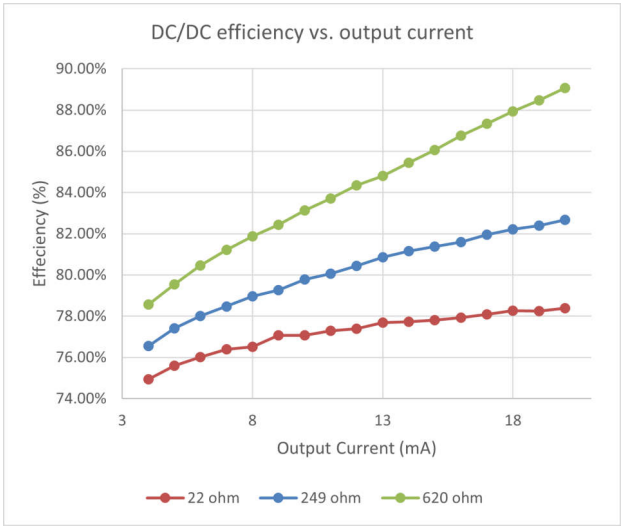


Figure 11. *DC/DC efficiency vs. output current.*

Precision and noise

A high-resolution analog-to-digital converter measures the effect of the DC/DC ripples on the output, converting 16,000 samples with a 640Ω load at 4 mA and 20 mA, respectively.

Table 1 summarizes the noise calculation and corresponding precision.

Output	4mA	20mA	Unit
Mean	4.019	20.17	mA
Root mean square (RMS) noise	325	530	nA
Peak-to-peak noise	2.78	3.51	µA
RMS resolution	18.2	17.5	Bits

Table 1. *Noise performance of the adaptive circuit.*

The results show that adaptive power doesn't affect the output stage performance, and can support 16-bit output resolution.

Settling time and dynamic performance

Settling time and the stability of the adaptive power loop are of great importance. **Figure 12** shows that input ramping to full-scale in 200µs results in a stable output with simple stepping of the input of the output stage.

Figure 12 shows a 10V step over a 560Ω load, with the full-scale input voltage to the output stage ramped over seven steps to the full scale of 2.5V. The figure also shows a settling time <200µs.

The falling edge is slow because the decoupling and output capacitors need to discharge through the circuit and external load. This doesn't affect performance and is not critical.

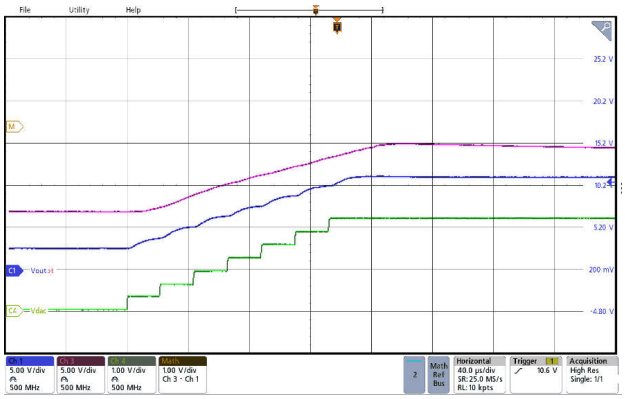


Figure 12. *Settling performance of the output stage and adaptive supply.*

Conclusion

The measurement results demonstrate that adaptive supply techniques deliver tangible benefit by achieving over 50% power savings compared to fixed-supply implementation. The 17.5 to 18.2 bits of RMS resolution prove that thermal management improvements don't come at the expense of signal quality. As PLC modules continue to pack more channels into smaller footprints, the techniques presented here transition from optimization strategies to practical necessities for next-generation industrial automation systems.

Additional resources

- See the TI Developer Conference presentation, "**System Power Savings Using Dynamic Voltage Scaling**."
- Check out the **Less Than 1-W, Quad-Channel, Analog Output Module With Adaptive Power Management Reference Design**.
- For more insight into the role of the feedforward capacitor to enhance dynamic performance, read the application report, "**Optimizing Transient Response of Internally Compensated DC/DC Converters With Feedforward Capacitor**."

About the author

Ahmed Noeman is a systems engineer at Texas Instruments, specializing in defining integrated solutions for industrial applications. Ahmed has more than 20 years of semiconductor experience in areas including system design, IC design and IC verification. Ahmed received an M.S. and B.S. in electrical engineering from Ain Shams University in Egypt.

A novel CCM-TCM multimode control method for totem-pole bridgeless PFC

Bosheng Sun
Systems Engineer, Texas Instruments

Introduction

Power-supply units (PSUs) in data centers must have high efficiency and high power density. The 80 Plus Ruby certification, announced last year, sets the highest efficiency standards for data center PSUs yet. As you can see in **Table 1**, 80 Plus Ruby efficiency is not only higher than 80 Plus Titanium at each load condition, but also requires 90% efficiency at a 5% load, which has never been specified before.

80 PLUS Certification	230V Internal Redundant				
Percentage of rated load	5%	10%	20%	50%	100%
80 Plus Titanium		90%	94%	96%	91%
80 Plus Ruby	90%	91%	95%	96.5%	92%

Table 1. *80 Plus certification levels*

In the meantime, limited server rack space and increasing power demands have led to high power density. The most recent Modular Hardware System – Common Redundant Power Supply targets 3.6kW power in a 185mm-by-39mm-by-73.5mm form factor which translates to 111W/in^3 power density while other PSU products are still at the 80W/in^3 to 90W/in^3 level.

Server PSU consists of a totem-pole bridgeless power factor correction (PFC) and a DC/DC converter. Traditional control methods used in totem-pole bridgeless PFC are either continuous conduction mode (CCM) or triangular conduction mode (TCM); each method has limitations, however. CCM totem-pole bridgeless PFC can achieve high power density, while its efficiency is limited because of hard switching, especially at light loads where switching losses become dominant. TCM totem-pole bridgeless PFC can achieve excellent efficiency across the entire load range because of zero voltage switching (ZVS), but requires two or more phases interleaved together to reduce the high inductor current ripple, resulting in low power density and high costs. **Table 2** compares the two methods.

	CCM operation	TCM operation
Pros	• Low peak-to-peak inductor current ripple • Simple control	• ZVS
Cons	• Hard switching, high switching losses	• High peak-to-peak inductor current ripple • Requires multiphase interleaving to reduce current ripple for high power applications, resulting in low power density and high cost • Complex control

Table 2. *Comparing CCM and TCM for totem-pole PFC*

To achieve both high efficiency and high power density, totem-pole bridgeless PFC could operate in multimode, as shown in **Figure 1**. At heavy loads or at the peak of an AC half cycle, the desired PFC input current is high and PFC operates in CCM. When the load reduces or at around the AC zero-crossing area where the desired PFC input current is low, PFC switches to TCM and operates with ZVS.

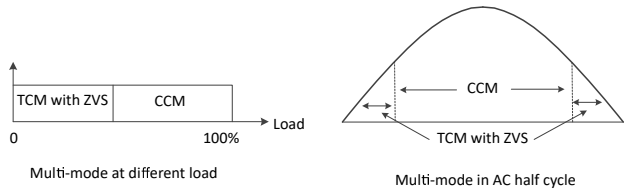


Figure 1. *CCM_TCM multimode operation*

Compared to pure CCM, multimode control has better efficiency at light loads, attributable to ZVS; compared to pure TCM, there is no need to use multiphase interleaved operation because the inductor current ripple is much lower, significantly reducing both size and system costs. Combining the advantages of both CCM and TCM makes it possible to meet both high-efficiency and high-power-density requirements.

How to let PFC enter TCM at light loads

TCM operation requires that the inductor current drop to zero at the end of the switching cycle. In CCM PFC, however, the inductor current is almost always greater than zero in the entire AC half cycle because of the high boost inductance. To let the inductor current drop to zero, one way is to choose a boost inductance lower than what CCM PFC uses, but higher than what TCM PFC uses.

Because lower inductance results in higher current ripple, it is important to design the inductor such that the efficiency gained from multimode operation is more than the extra inductor core loss caused by the higher current ripple. The electromagnetic interference filter also needs redesigning, since the inductor current ripple is higher than in CCM.

Another option is to keep the same CCM inductor but use a switching frequency fold-back profile, as shown in **Figure 2**. The switching frequency is the highest (equal to the nominal switching frequency in CCM operation) at the AC peak, and gradually reduces toward AC zero crossing.

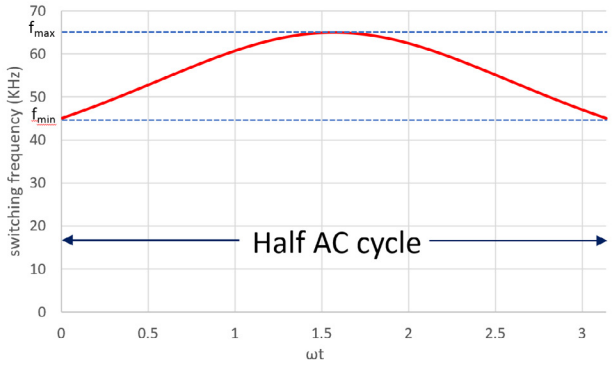


Figure 2. *Switching frequency profile in an AC half cycle*

Equation 1 calculates the switching frequency across the AC half cycle:

$$f = \frac{1}{\frac{1}{f_{min}} - \left(\frac{1}{f_{min}} - \frac{1}{f_{max}}\right)\sin(\omega t)} \quad (1)$$

where f_{max} is the switching frequency as used in traditional CCM operation, f_{min} is the minimum switching frequency, and ωt is the angular frequency of the AC input voltage.

With the reduced switching frequency, the inductor current will drop to zero at the end of the switching cycle, making TCM control possible. Then the PFC can be controlled to operate in CCM at the AC peak, and switch to TCM with ZVS around the AC zero-crossing area. Further reducing the minimum switching frequency can expand the TCM region but at the cost of reduced loop bandwidth, possibly resulting in poor total harmonic distortion (THD) or even loop instability.

How to detect zero current

For TCM control, adding a zero current detection (ZCD) circuit by placing a resistor on the PFC ground return path or adding a second winding on the boost inductor will detect the instant that the inductor current drops to zero. Some devices, such as TI's LMG3427R030 gallium nitride (GaN) field-effect transistor (FET), have a built-in ZCD circuit, generating a ZCD signal when the current goes to zero, as shown in **Figure 3**. Using this device as a high-frequency switch can significantly

simplify the design process. The ZCD signal is sent to a microcontroller (MCU) for further processing.

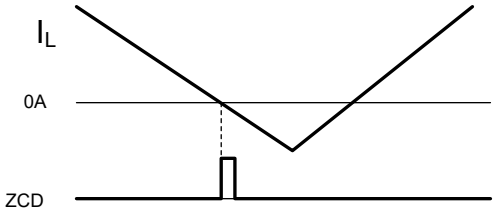


Figure 3. *ZCD signal generation*

How to achieve ZVS at TCM

To achieve ZVS operation at TCM, the inductor current needs to go to negative to discharge the switch-node voltage. Upon receiving the ZCD signal, the MCU adds a time delay to this ZCD signal and then uses that delayed ZCD signal to turn off pulse-width modulation (PWM) and reset the PWM counter, as shown in **Figure 4**. After reset, the next switching period starts and the boost switch turns on. The time delay makes the inductor current go negative because the synchronous switch is still on after the inductor current drops to zero. Appropriately adjusting the delay time will adjust the amount of negative current such that the switch-node voltage will discharge to zero, turning on the boost switch at that moment and achieving ZVS.

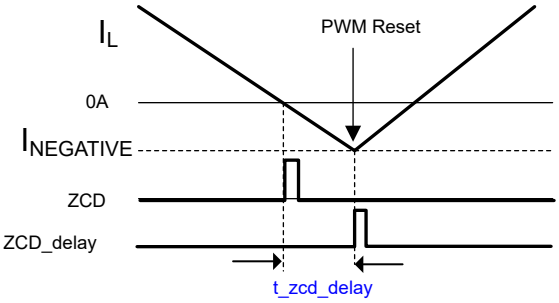


Figure 4. *Adding a ZCD delay to reset PWM*

For a given dead-time Δt from when the synchronous switch turns off to when the boost switch turns on, **Equation 2** calculates the required minimum negative current necessary to fully discharge the switch-node voltage:

$$I_{NEGATIVE} = -\frac{2 \times C_{OSS} \times V_{out}}{\Delta t} \quad (2)$$

where C_{OSS} is the output capacitance of the switch and V_{out} is the PFC output voltage.

Equation 3 then calculates the required minimum ZCD delay time:

$$t\_zcd\_delay = \frac{L \times |I_{NEGATIVE}|}{V_{out} - V_{in}} \quad (3)$$

where L is the boost inductance and V_{in} is the PFC input voltage.

In **Equation 3**, when V_{in} is close to V_{out}, the calculated delay time may be too long such that the delayed ZCD signal falls into the next switching period, as shown in **Figure 5**. Resetting PWM here is wrong. To prevent this, generate an ENABLE window that starts at the beginning of the ZCD signal and ends at the end of the current switching period, as shown in **Figure 5**. The MCU uses this ENABLE window to AND with the delayed ZCD signal to generate a RESET signal, and then uses that RESET signal to reset PWM. This ensures that the PWM reset can only occur within the same switching cycle.

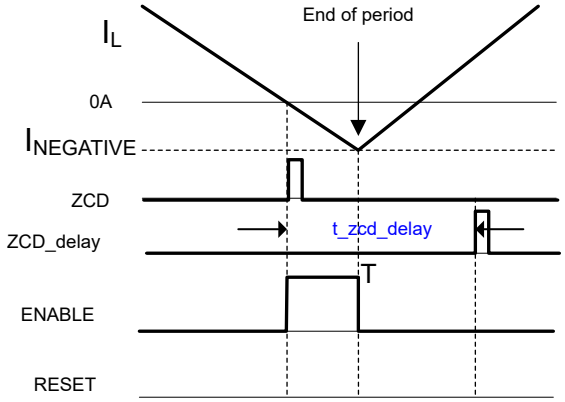


Figure 5. *ENABLE window and RESET signal*

Transitioning between CCM and TCM

The transition between CCM and TCM is automatic. At the AC peak or heavy loads, the inductor current is high. It does not drop to zero, and because no ZCD signal is generated, there is no RESET signal. The PWM counter naturally resets at the end of its nominal switching period. And since the switching frequency equals the

nominal switching frequency, PFC operates the same as a traditional CCM PFC, as shown in **Figure 6**.

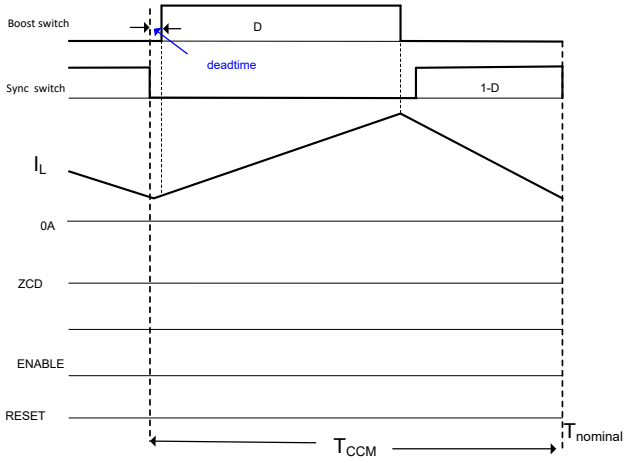


Figure 6. *CCM operation at the AC peak*

When the AC toward zero crossing, both the inductor current and switching frequency drop, while the inductor current drops to zero before the end of the switching period. The GaN device generates a ZCD signal. Using the time delay calculated by **Equation 3** and ANDing with the ENABLE window – generates a RESET signal. The RESET signal resets the PWM. The synchronous switch turns off before the end of the nominal switching period and the next switching period begins. The actual switching frequency is less than the nominal switching frequency. PFC operates as TCM PFC, as shown in **Figure 7**.

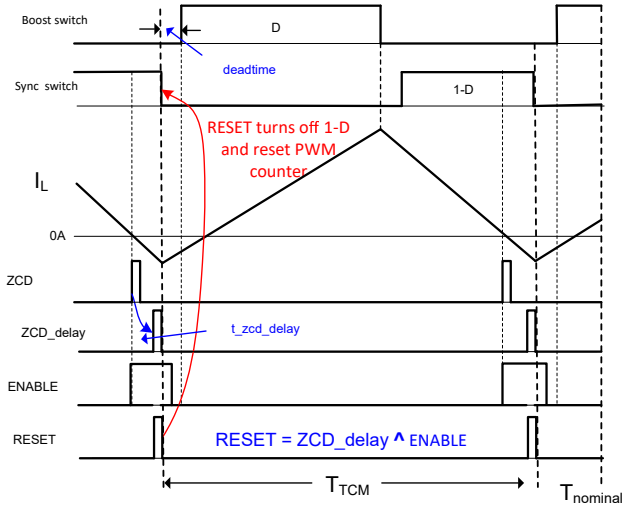


Figure 7. *TCM operation around AC zero crossing*

Dynamic dead time

In CCM, keeping the dead time to a minimum – the time between when the synchronous switch turns off and the boost switch turns on – will reduce the body-diode conduction time of the boost switch. In TCM, when the synchronous switch turns off, it takes time to discharge or charge the switch-node voltage. Therefore, the dead time needs to be longer. Using a dynamic dead time between CCM and TCM optimizes efficiency.

Control law and PWM generation

In traditional TCM operation, there is only a voltage loop – no current loop. The boost switch turns on time is determined by a constant Ton control manner. In the multimode control method, the traditional average current-mode controller, as shown in **Figure 8**, generates the PWM duty cycle for both TCM and CCM operations. The controller contains an outer voltage loop (G_V) and an inner current loop (G_I). The output of G_V is modulated by the sensed input voltage to be the current command for the current loop. Since the same compensator generates the PWM duty cycle for both CCM and TCM, the mode transition is smooth, with no current distortion during the mode transition.

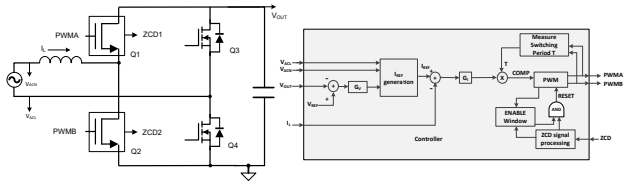


Figure 8. *Block diagram for proposed CCM_TCM control*

In the MCU, comparing a COMP value to a RAMP signal generates the PWM signal, where COMP is calculated in **Equation 4** by multiplying current loop G_i output with switching period T:

$$\mathrm{COMP} = G_i \times T \qquad (4)$$

In traditional CCM operation, the switching period T is constant. However, in TCM operation, the RESET signal determines the actual switching period; it is shorter than T. Using **Equation 4** results in a PWM pulse width longer

than needed, causing G_I to work harder to compensate. Pushing G_I to a higher bandwidth can help, but may cause loop instability.

To resolve this issue, let the controller keep measuring the actual switching period. Calculate the COMP value by multiplying the G_I output with the measured switching period from the previous switching cycle, as shown in **Equation 5** and **Figure 9**. **Equation 5** is valid because the PWM period is almost the same in two consecutive cycles.

$$COMP_N = G_i \times T_{N-1} \quad (5)$$

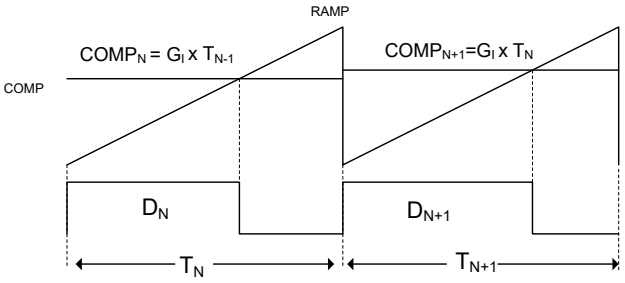


Figure 9. *PWM generation*

Test results

This control method was implemented in a 3.6KW totem pole bridgeless PFC [1]. Its maximum switching frequency is 65KHz, the minimum switching frequency is set at 45KHz. The controller uses TI's TMS320F280039C real-time MCU. High-frequency switches use the LMG3427R030 GaN FET, which has a built-in ZCD circuit. A 65KHz interrupt service routine 1 (ISR1) implements the current loop and ZCD delay-time calculation, while a 10KHz interrupt service routine 2 (ISR2) implements the voltage loop. The ZCD delay, ENABLE window, AND logic, and actual switching period measurement are implemented through the TMS320F280039C's configurable logic block (CLB). After configuration, the CLB runs independently without involving the CPU.

The design achieved >180W/in^3 power density and has excellent light-load efficiency. **Figure 10** and **Figure 11** show the efficiency comparison (tested on the same board) between this proposed control method and traditional CCM control, with light-load efficiency improving by as much as 2%.

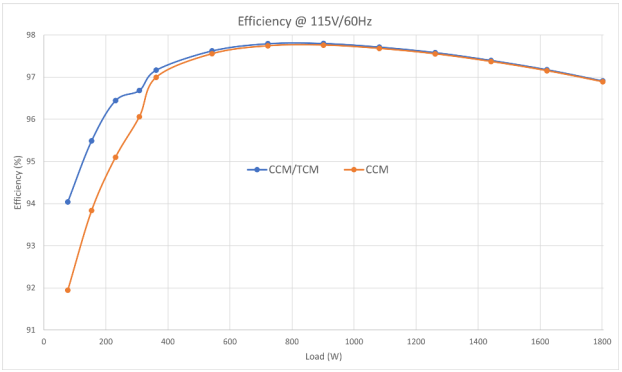


Figure 10. *Efficiency comparison at low line*

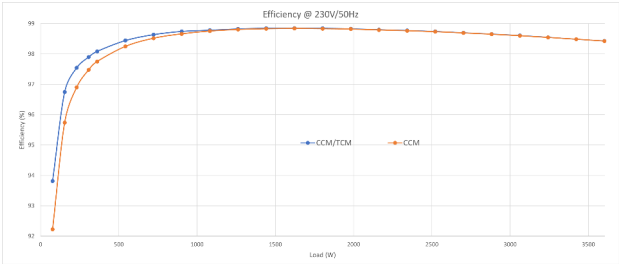


Figure 11. *Efficiency comparison at high line*

Figure 12 shows the input current waveform at a 50% load, with no current distortion observed during the mode transition.

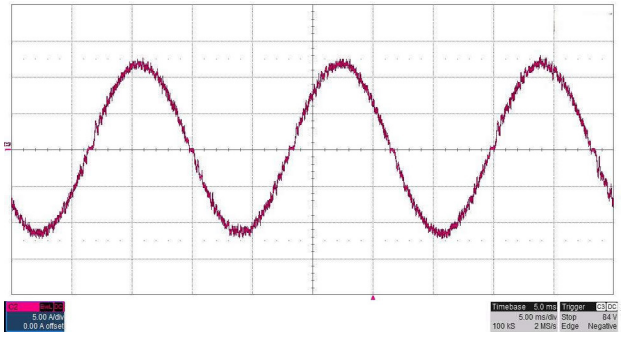


Figure 12. *Input current waveform at a 50% load*

Conclusion

Totem-pole bridgeless PFC can achieve both high efficiency and high power density through CCM-TCM multimode operation by letting PFC operate at CCM at heavy loads or at the AC peak, and switching to TCM

with ZVS at light loads or around the AC zero-crossing area. CCM-TCM multimode greatly improves light-load efficiency, with no input current distortion during mode transition. This is very helpful for applications requiring 80 Plus Ruby efficiency.

References

1. Texas Instruments. n.d. "**3.6kW CCM-TCM Multimode-Controlled Totem-Pole Bridgeless PFC Reference Design**." Texas Instruments reference design No. PMP23537. Accessed Feb. 16, 2025.

About the author

Bosheng Sun is a systems engineer at Texas Instruments, where he focuses on developing digitally controlled, high-performance AC/DC solutions for server and industrial applications. He earned an M.S. in electrical engineering from Cleveland State University in 2003 and a B.S. in electrical engineering from Tsinghua University in Beijing in 1995. He holds six U.S. patents.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Last updated 10/2025