Analog Engineer's Circuit

Current Limiting with Comparator Circuit

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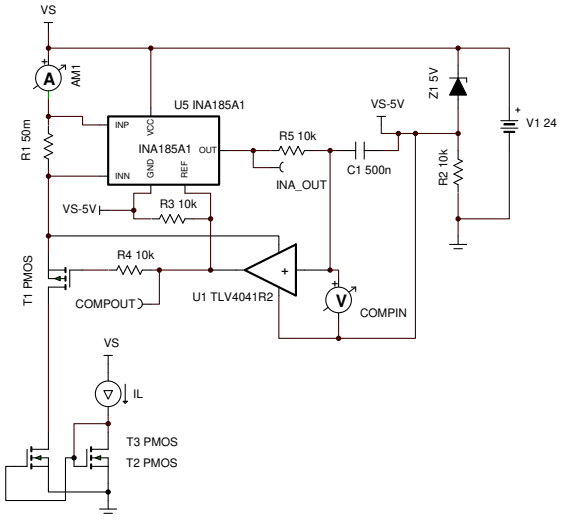
Design Goals

LOAD CURRENT (I_L)	SYSTEM SUPPLY (V_S)	CURRENT SENSE AMP	COMPARATOR OUTPUT STATUS	
Over Current (I_{OC})	Typical	Gain	Over Current	Normal Operation
200mA	24V	20V/V	$V_{OH} = V_S$	$V_{OL} = V_S$ - 5V

Design Description

This high-side, current sensing solution uses a current sense amplifier, a comparator with an integrated reference, and a P-channel MOSFET to create an over-current latch circuit. When a load current greater than 200mA is detected, the circuit disconnects the system from its power source. Since the comparator drives the gate of the P-channel MOSFET and feeds the signal back into the reference pin of the current sense amplifier, the comparator output will latch (hold the gate source voltage of the P-channel MOSFET to 0V) until power to the circuit is cycled.



Design Notes

1. Select a precision, current sense amplifier (INA) with an external reference pin so its output voltage can be adjusted.
2. Select a comparator with a rail-to-rail input so its output will be valid over the entire operating voltage range of the current sense amplifier.
3. Select a comparator with a push-pull output stage that can drive the gate of a MOSFET and an integrated reference to optimize circuit accuracy.
4. Create a floating 5V supply that can power the INA and comparator.

Design Steps

1. Select the value of R_1 so V_{SHUNT} is at least 100x greater than the current sense amplifier input offset voltage (V_{OS}). Note that making R_6 very large will improve OC detection accuracy but will reduce supply headroom and power dissipation.

$$V_{SHUNT} = (I_{OC} \times R_1) \geq 100 \times V_{OS}$$

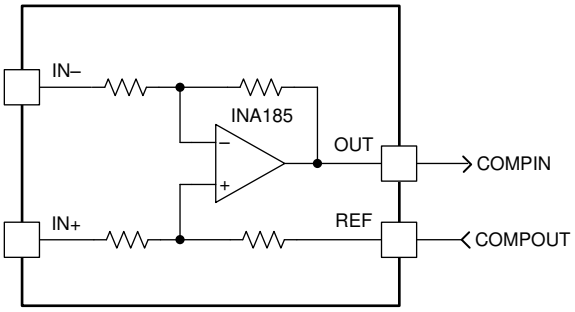
$$\text{Set} \quad R_1 \geq \frac{100 \times V_{OS}}{I_{OC}} = 50\text{m}\Omega \quad \text{for} \quad I_{OC} = 200\text{mA} \quad \& \quad V_{OS} = 100\mu V$$

2. Determine the desired gain (A_V) option for the INA based on the switching threshold of the comparator. When the load current (I_L) reaches the over-current threshold (I_{OC}), the INA output must cross the switching threshold (V_{TH}) of the comparator.

$$V_{TH} = (I_{OC} \times R_1) \times A_V = 0.2\text{V}$$

$$\text{Set} \quad A_V = \frac{V_{TH}}{I_{OC} \times R_1} = \frac{0.2}{0.2 \times 0.05} = 20\text{V/V} \quad \text{for} \quad R_1 = 50\text{m}\Omega$$

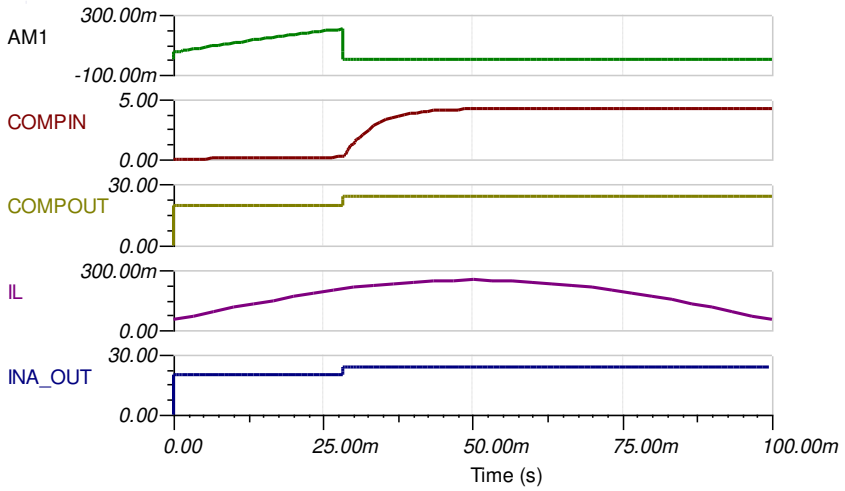
3. Since many INA's and comparators have 5V operating voltage ranges, a 5V supply voltage needs to be derived from the system supply V_S. In addition, the 5V supply needs to float below V_S so the comparator output can drive the source-gate voltage of the P-channel MOSFET to 0V when an over-current condition occurs and 5V when the load current is less than I_{OC}. The method used in this circuit is a 5V zener diode with a 10 kΩ bias resistor (R_2). Other options such as shunt regulators can also be utilized as long as proper bias current through the device is maintained.
4. A low pass filter is added between the INA output and the comparator input to attenuate any high frequency current spikes. It is more important to trigger the over-current latch with a delay than to falsely disconnect the system from the supply voltage. The low pass filter is derived from R_5 and C_1. Since the switching threshold of the comparator is 0.2V, the delay is less than 1 time constant ($R_5 \times C_1$=5ms).
5. A current limiting resistor R_4 is inserted between the comparator output and the gate of the P-channel MOSFET. Setting R_4 to 10 kΩ reduces current spikes on the supply when the comparator output needs to charge the MOSFET gate-source capacitance as a compromise to increasing the charge time. Inserting R_4 also serves the purpose of protecting the comparator output from any supply transients that can be present on the supply line.
6. The output of the comparator is directly connected to the REF pin of the INA in order to apply an offset to the INA's output voltage. When $I_L < I_{OC}$, the comparator output is low (equal to V_S-5V) and no offset is added to the INA. However, when $I_L > I_{OC}$, the comparator output goes high (equal to V_S) and a 5V offset is added to the INA. This offset causes the INA output to saturate at a level equal to V_S. Since an INA output level of V_S is higher than the V_{TH} of the comparator, the comparator output will remain high. This condition is referred to as a *latched* output state since the circuit will remain in this state until power to the circuit is cycled.



7. R_3 is added between the INA reference pin (REF) and GND (V_S-5V) to ensure a proper ground path as the 5V supply ramps up to the comparator minimum operating voltage.
8. If a latching feature is not preferred, the comparator output can be disconnected from the current sense amplifier reference pin and R_3 can be replaced with a short. In this configuration, the circuit will behave as a 200mA current limiter.

Design Simulations

Transient Simulation Results



Design References

Texas Instruments, SBVM944 simulation file, circuit software

Design Featured Comparator

TLV4041R2	
V_S	1.6V to 5.5V
V_{inCM}	Rail-to-rail
V_{OUT}	Push-Pull
Integrated Reference	200mV ± 3mV
I_Q	2µA
t_{PD}	360ns
TLV4041R2	

Design Featured Current Sense Amplifier

INA185	
V_S	2.7V to 5.5V
V_{inCM}	-0.2V to 26V
Gain Options	20V/V, 50V/V, 100V/V, 200V/V
Gain Error	0.2 %
V_{OS}	100µV (A1), 25µV (A2, A3, and A4)
I_Q	200µA
INA185	

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