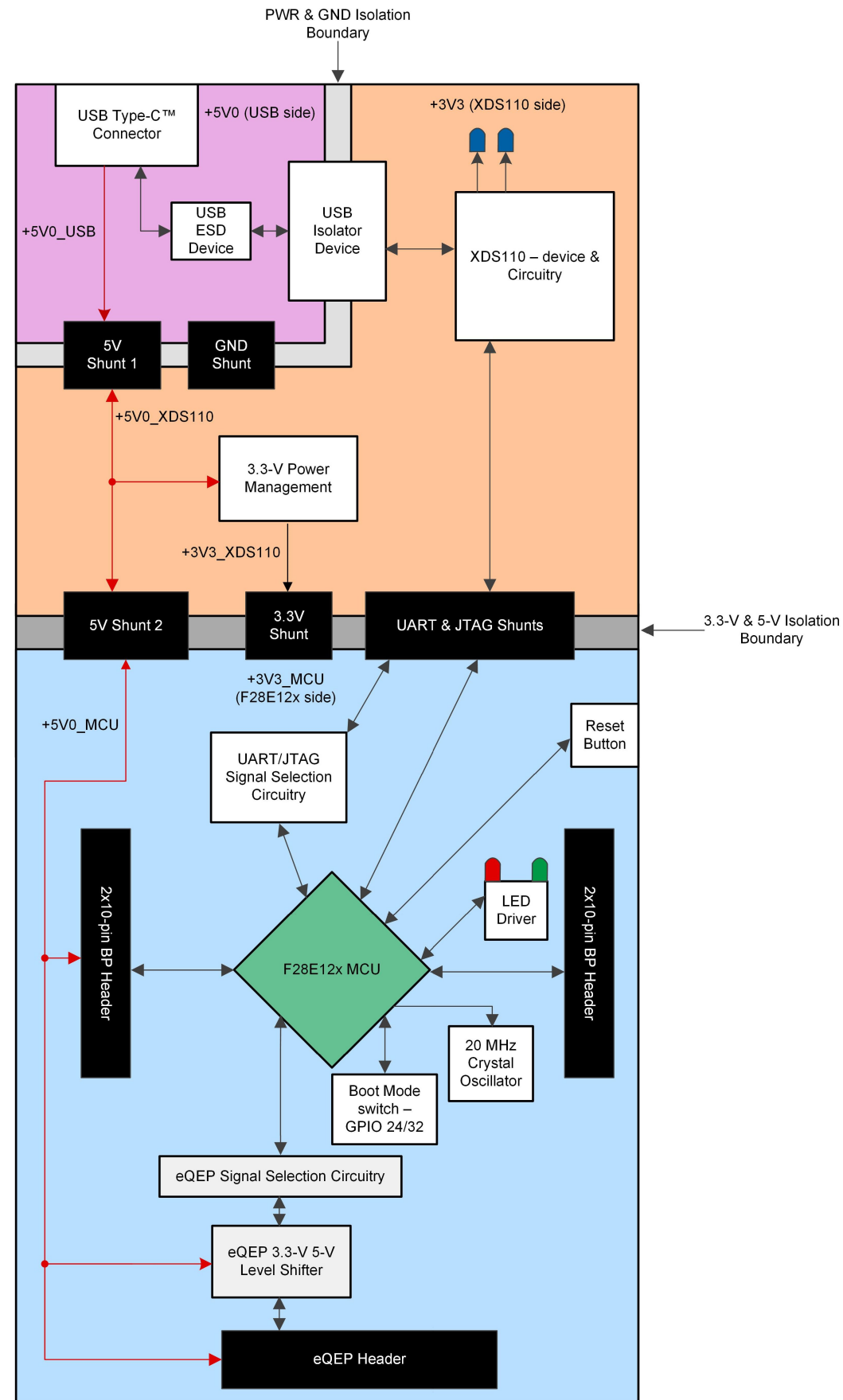
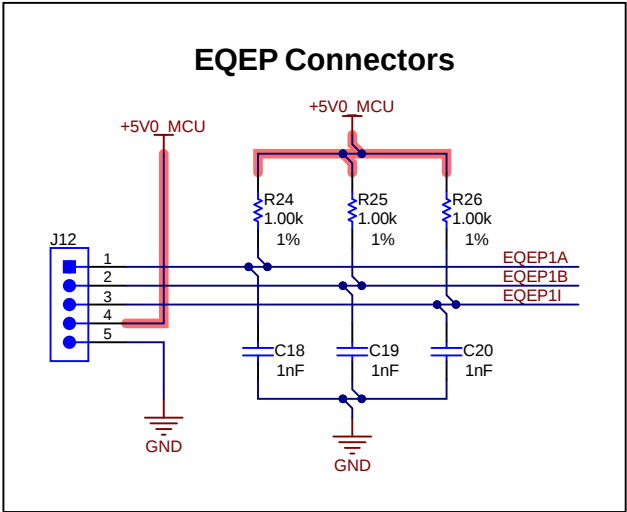
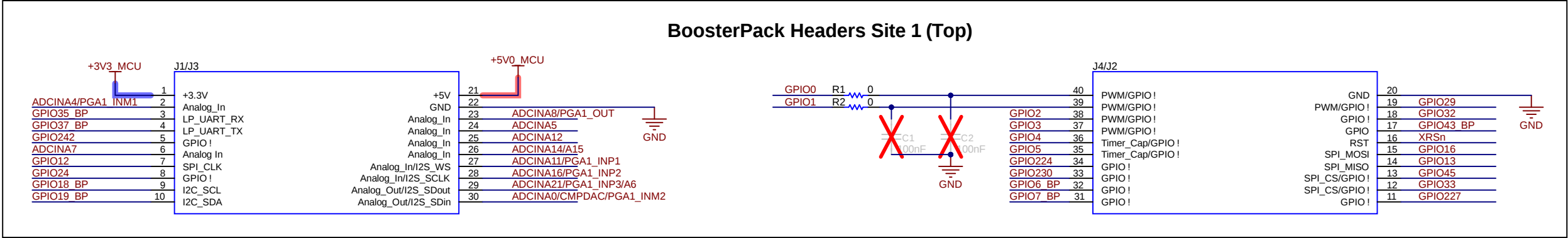


Revision History				
Rev	ECN #	Approved Date	Approved by	Notes
E1	N/A	Feb 6, 2025	PL	Original engineering release
E2	N/A	Mar 4, 2025	PL	Minor changes to silkscreen Changed U14 to TPS7A8033
A	N/A	Jul 21, 2025	PL	Updated version of F28E120SC device



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Orderable: LAUNCHXL-F28E12X	Designed for: Public Release	Mod. Date: 7/21/2025	
TID #:	Project Title: LAUNCHXL-F28E12X		
Number: MCU152	Rev: A	Sheet Title:	
SVN Rev: Version control disabled	Assembly Variant: 001	Sheet: 1 of 8	
Drawn By: Peter Luong	File: MCU152A Block Diagram SchDoc	Size: B	http://www.ti.com
Engineer: Peter Luong	Contact: http://www.ti.com/support		© Texas Instruments 2025



A

B

C

D

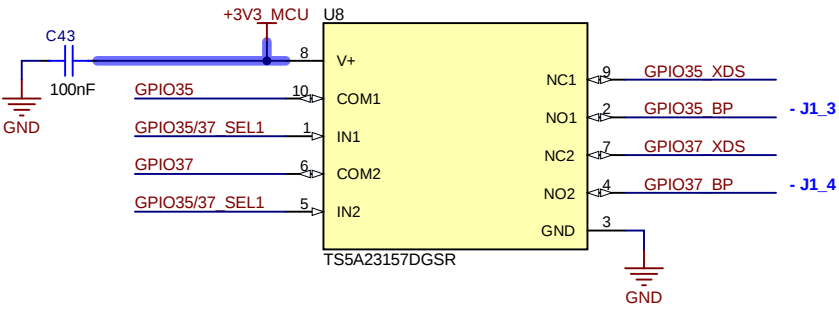
A

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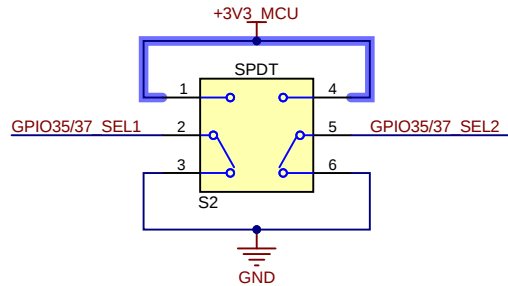
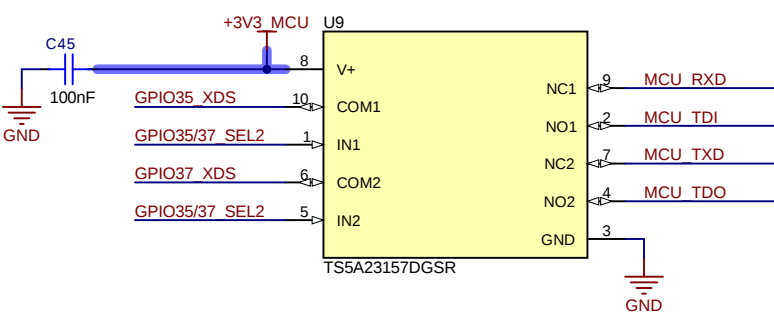
D

GPIO35/37 Routing (BoosterPack, JTAG, SCI/UART)

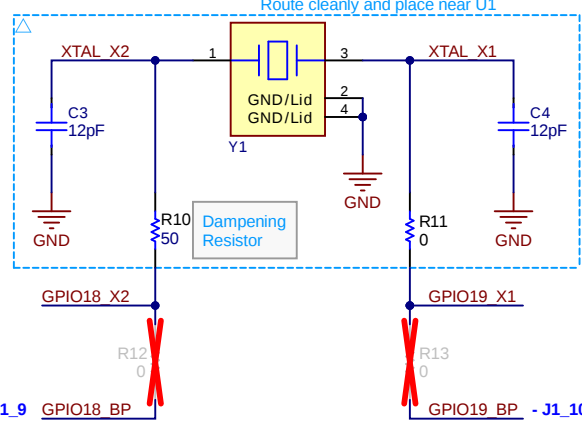


GPIO35/37_SEL1	GPIO35/37_SEL2	GPIO35/37 Route
0	0	XDS110: UART RXD/TXD
0	1	XDS110: JTAG TDI/TDO
1	x	BoosterPack

- DEFAULT



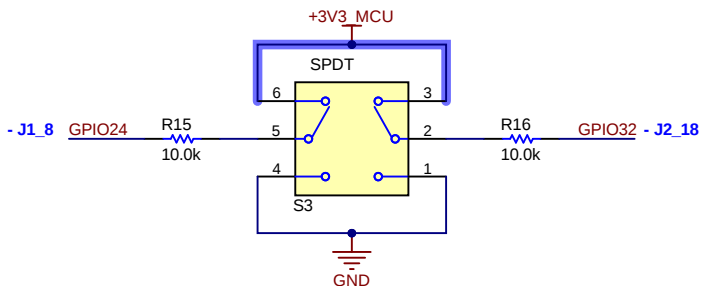
Oscillator



By default:
- Crystal Y2 is connected between GPIO18_X2 and GPIO19_X1.
- GPIO18_BP AND GPIO19_BP are connected to the BoosterPack headers.

If GPIO18 and GPIO19 are needed at the Boosterpack Headers:
- Remove R10 and R11, populate R12 and R13 with 0 ohm resistors
- The F28E12x device's internal oscillator will need to be used

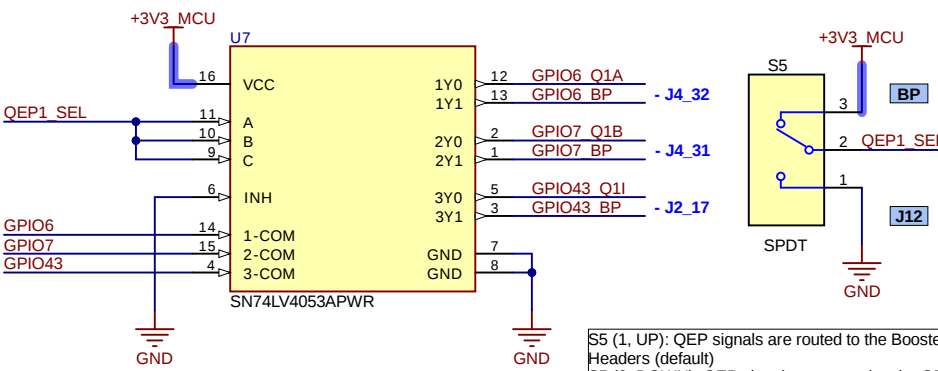
Boot Mode Select



Selected Boot Mode Chart

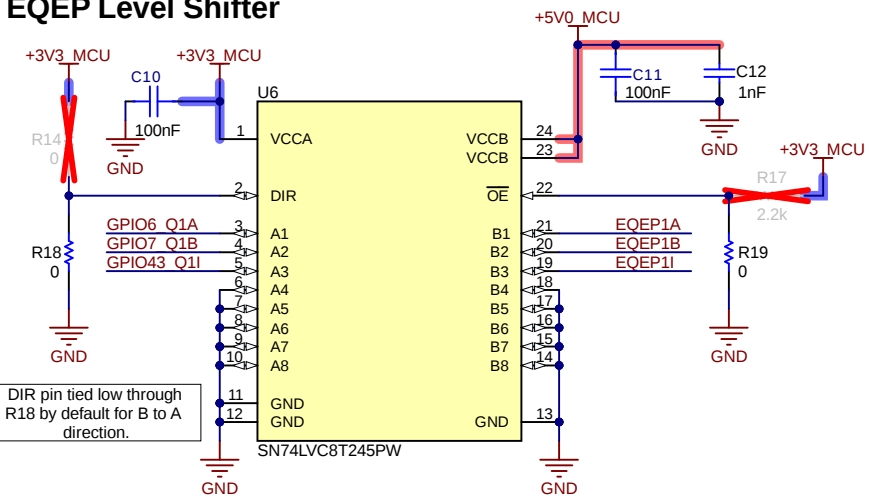
Mode #	GPIO24	GPIO32	Boot Mode
00	0	0	Boot from Parallel GPIO
01	0	1	Boot from SCI / Wait Mode
02	1	0	Boot from CAN
03	1	1	Boot from Flash

EQEP Routing



S5 (1, UP): QEP signals are routed to the BoosterPac k Headers (default)
S5 (0, DOWN): QEP signals are routed to the QEP Headers

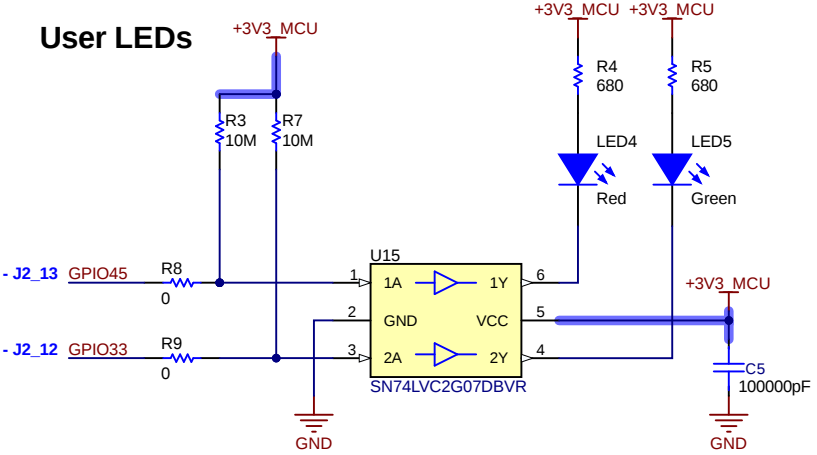
EQEP Level Shifter



DIR pin tied low through R18 by default for B to A direction.

To disable the Level Shifter:
1. De-populate R19
2. Place a 2.2k ohm resistor on R17 to pull-up OE

User LEDs



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A

A

B

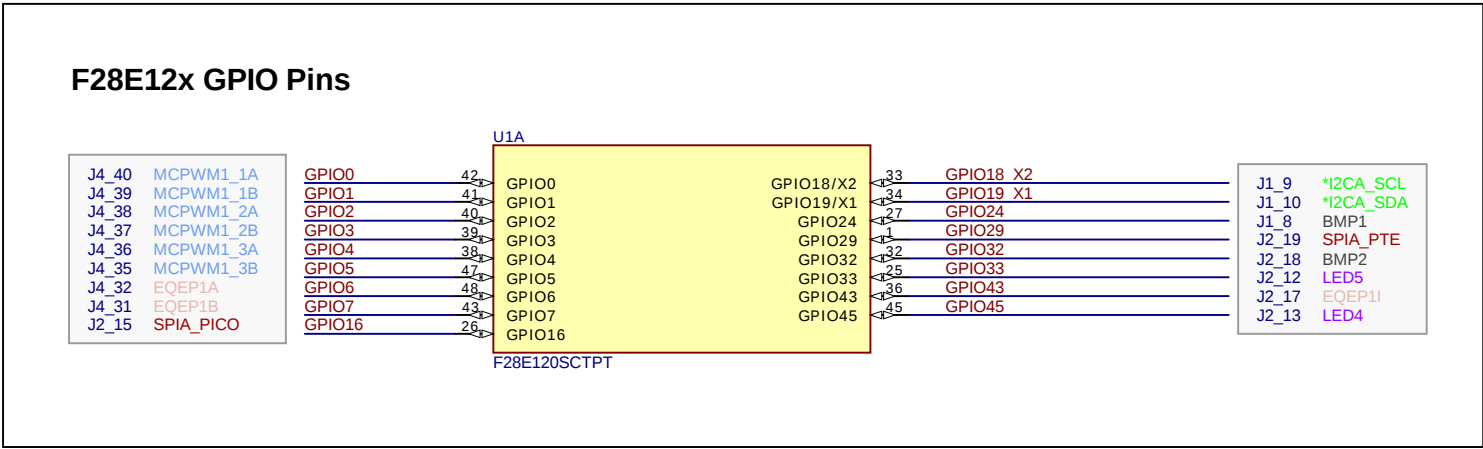
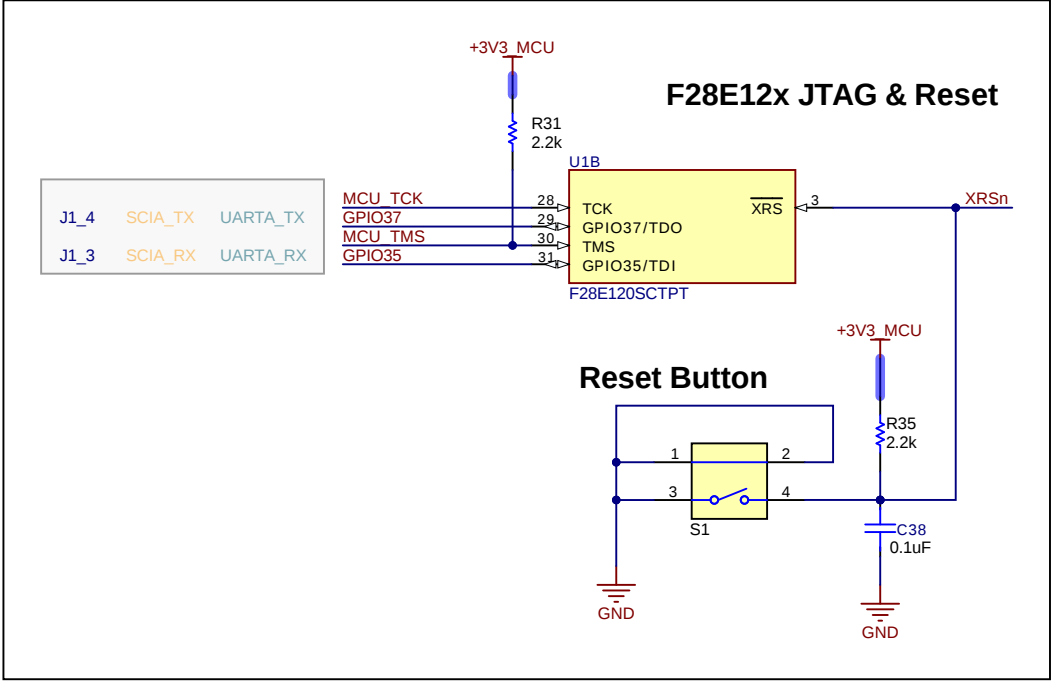
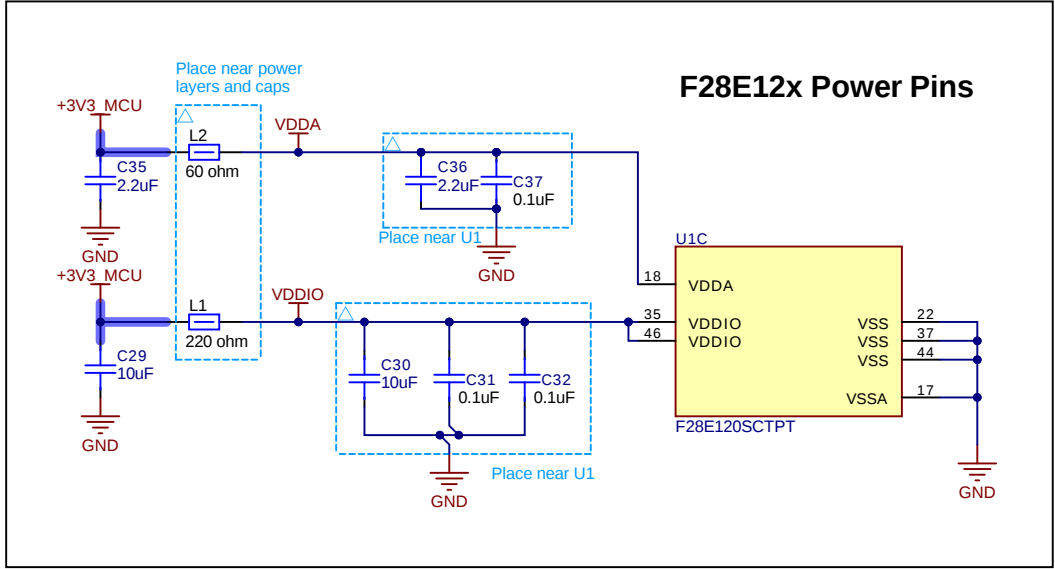
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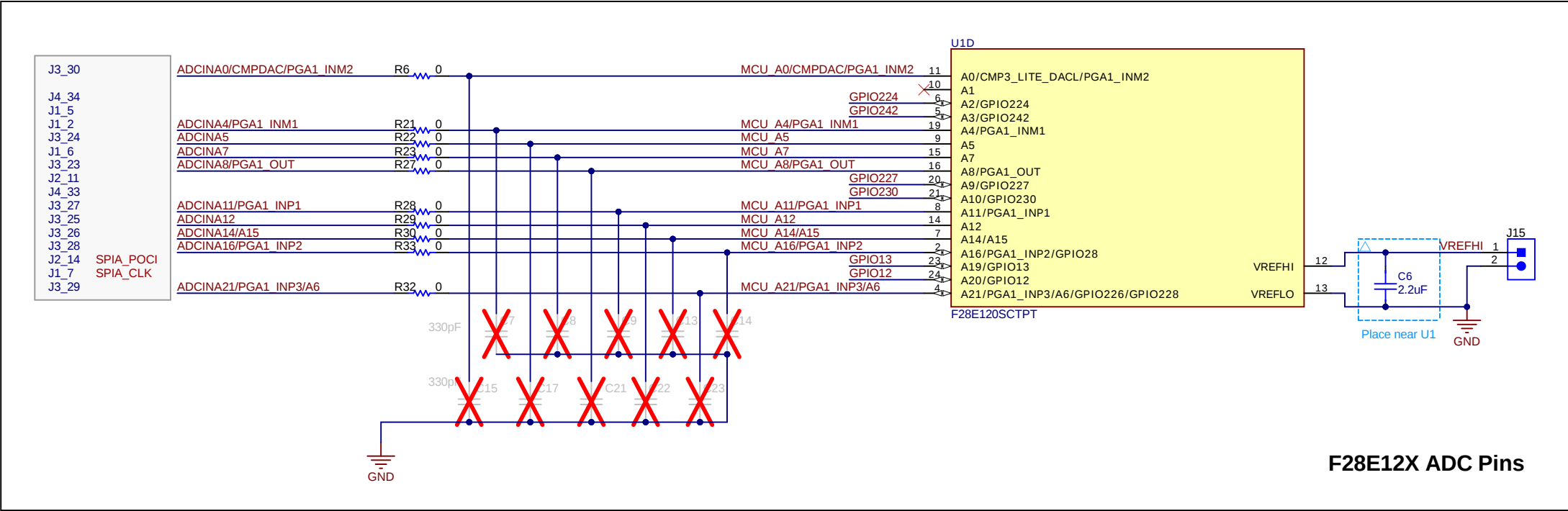
C

C

D

D

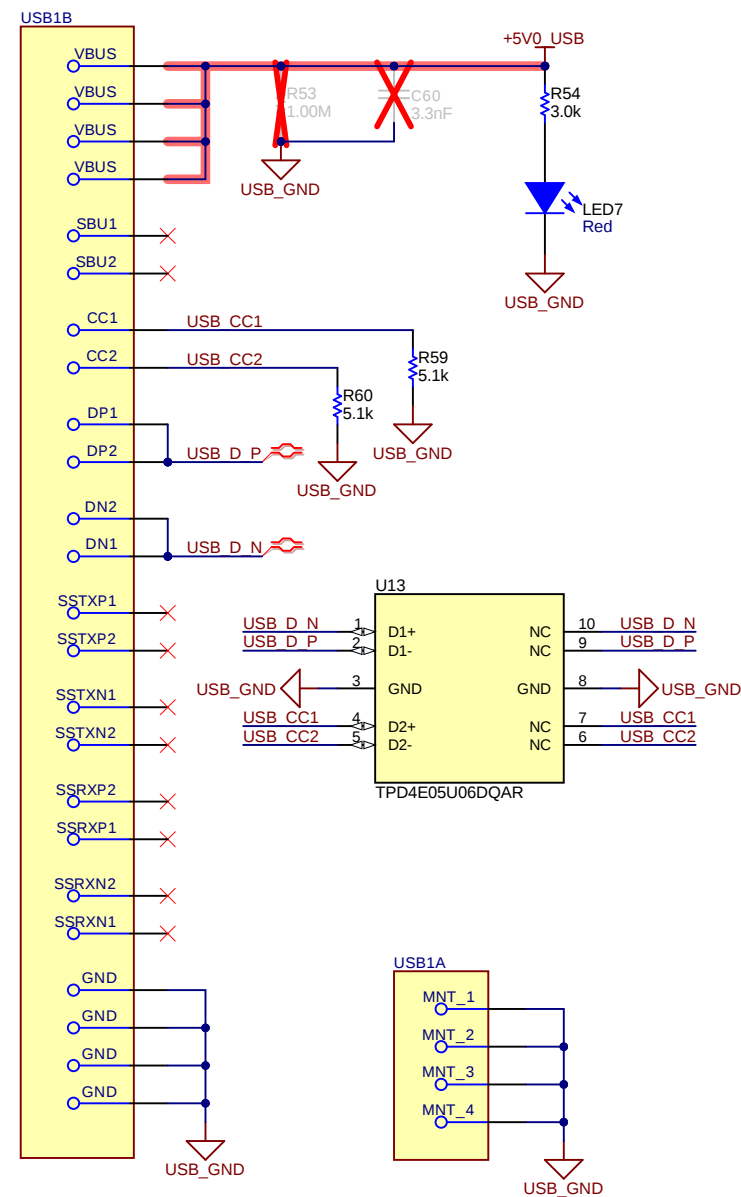




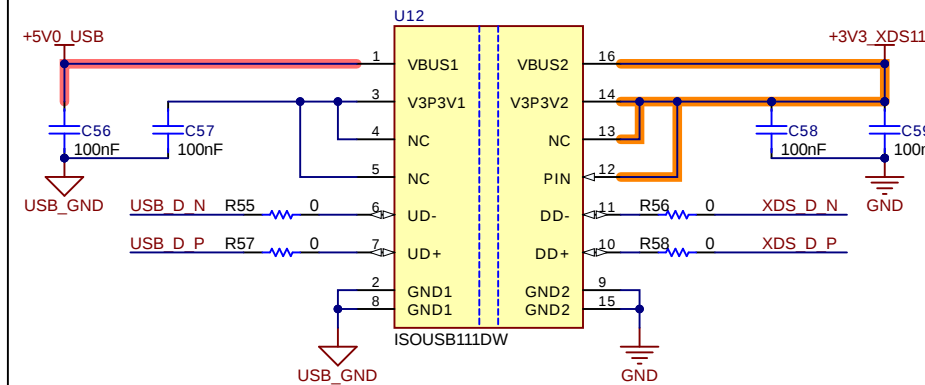
F28E12X ADC Pins

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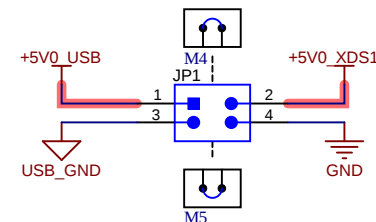
USB-C Connector



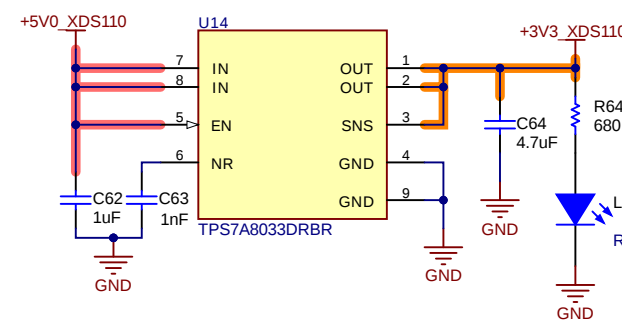
USB Isolation



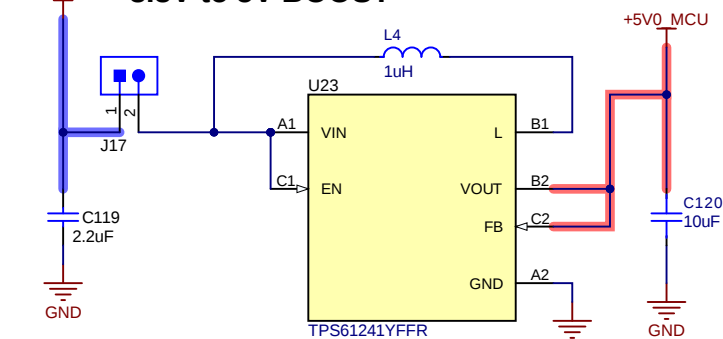
PWR & GND Isolation Boundary



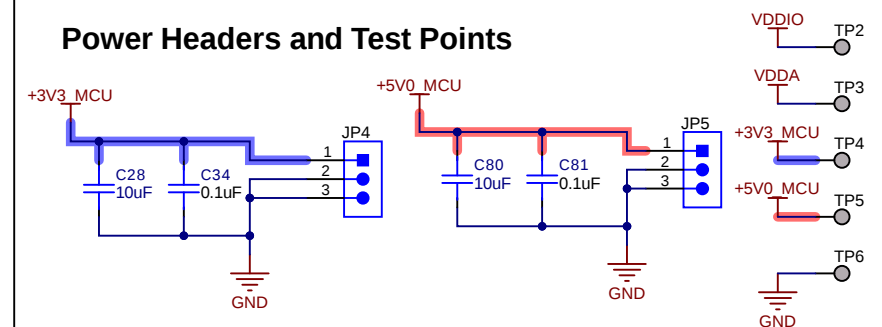
5V to 3.3V



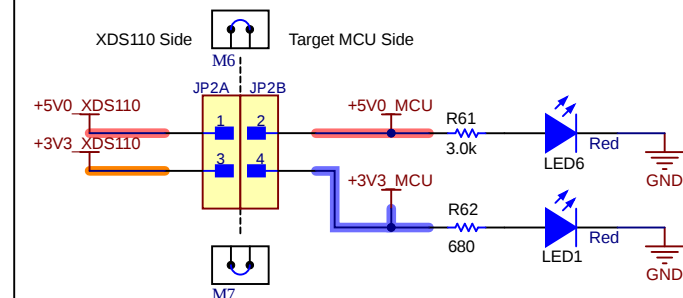
3.3V to 5V BOOST



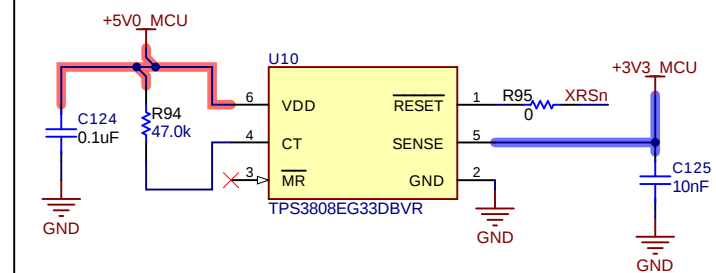
Power Headers and Test Points



5V & 3.3V Isolation Boundary



System Supervisory Circuit



A

B

C

D

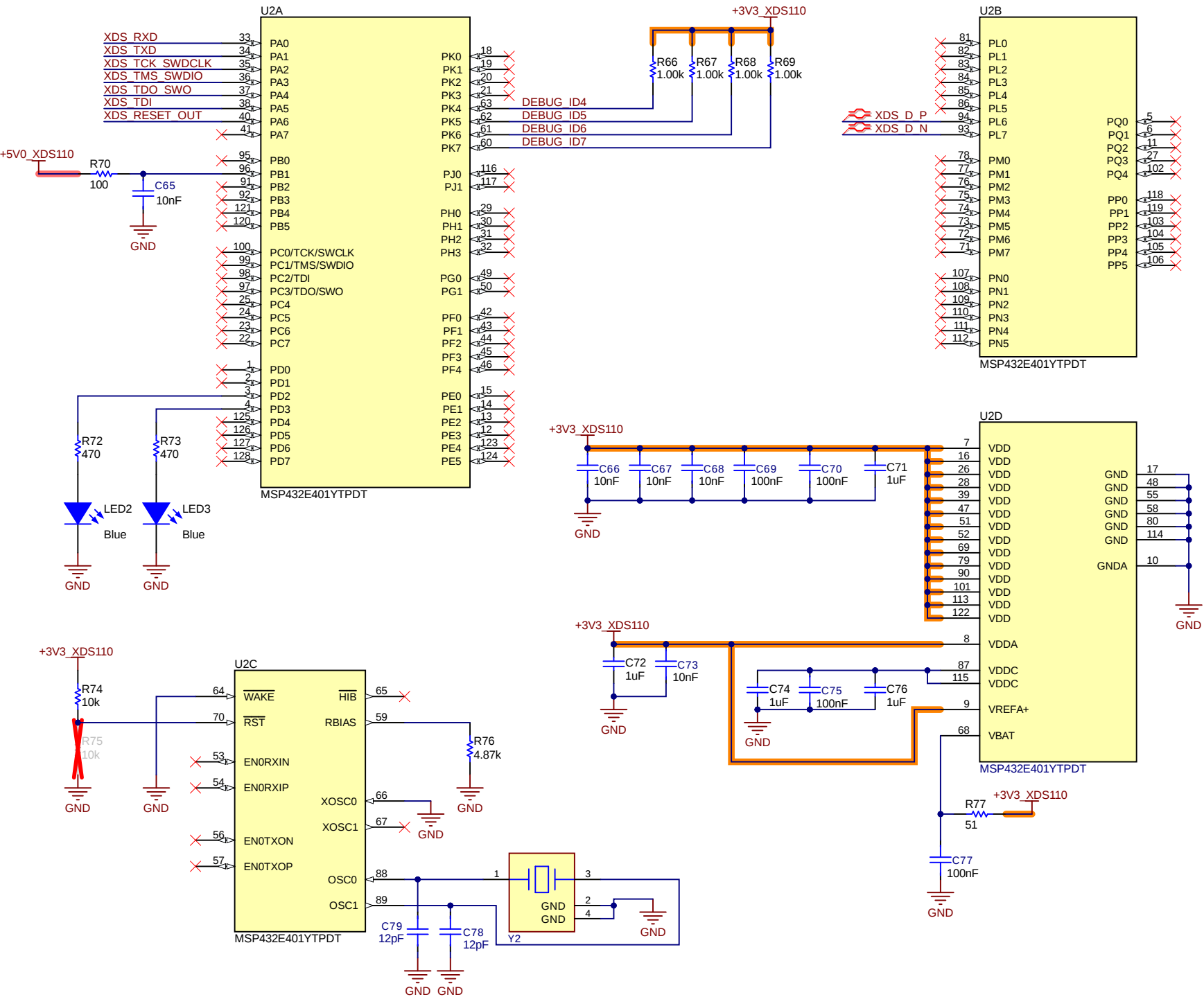
A

B

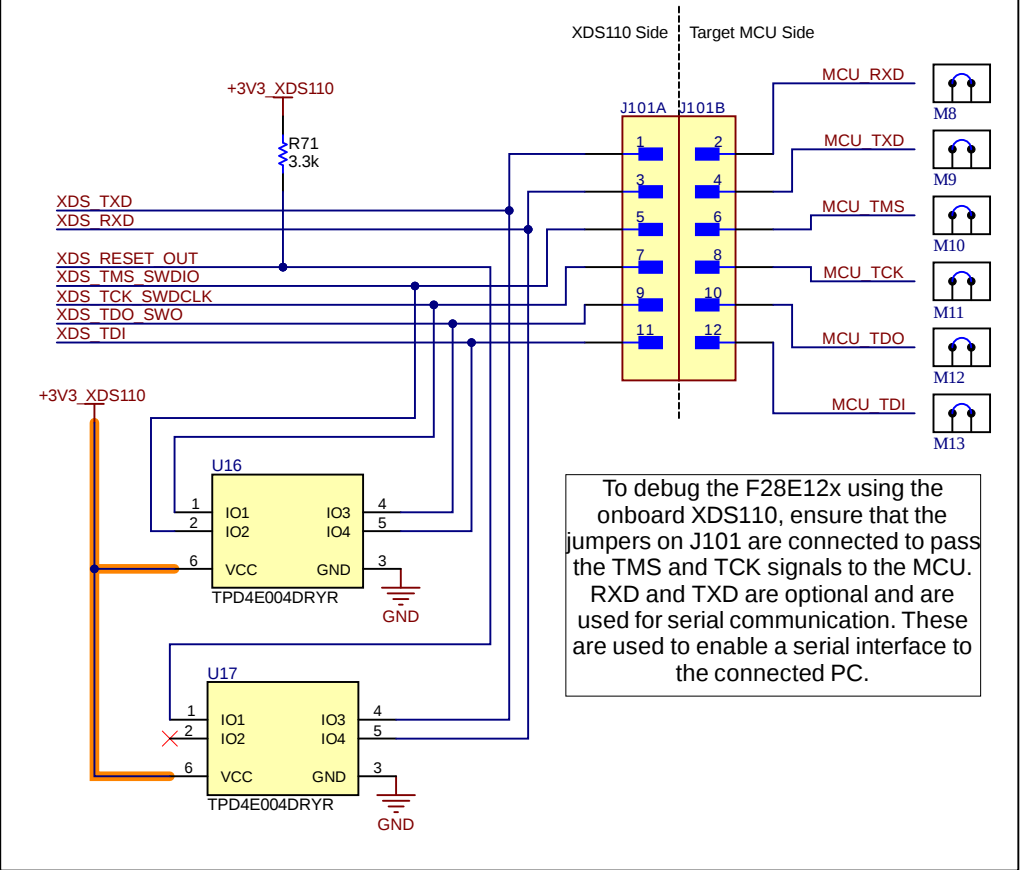
C

D

XDS110 Device



XDS110 Target Interface



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MH1 MH2

MH3 MH4

H1
MAE-10

H2
MAE-10

PCB Number: MCU152
PCB Rev: A

Logo1
PCB
LOGO
Texas Instruments



Logo2
PCB
LOGO
FCC disclaimer

Logo3
PCB
LOGO
WEEE logo

Logo4
PCB
LOGO
Texas Instruments

ZZ1

Assembly Note

These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ2

Assembly Note

These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ3

Assembly Note

These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Orderable: LAUNCHXL-F28E12X	Designed for: Public Release	Mod. Date: 2/5/2025	
TID #:	Project Title: LAUNCHXL-F28E12X		
Number: MCU152	Rev: A	Sheet Title:	
SVN Rev: Version control disabled	Assembly Variant: 001	Sheet: 8 of 8	
Drawn By: Peter Luong	File: MCU152A_Hardware_SchDoc	Size: B	http://www.ti.com
Engineer: Peter Luong	Contact: http://www.ti.com/support		© Texas Instruments 2025



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