The Offset DAC

ABSTRACT

Several of TI's high-resolution delta-sigma Analog-to-Digital Converters [1] (ADCs) include an analog offset Digital-to-Analog Converter (DAC) for helping extend the input range. This application note provides additional insight into how the offset DAC works, discusses its performance, and also shows how to use it as a signal generator for a self-test.

Contents

List of Figures

List of Tables

[1] ADS1216, ADS1217, ADS1218, ADS1240, ADS1241, ADS1242, ADS1243, MSC1210.

1 How It Works

Figure 1 shows the block diagram for the offset DAC and associated circuitry. Conceptually, the offset DAC is a programmable voltage source. The input voltage, after being amplified by the Programmable Gain Amplifier (PGA), sums with the offset DAC voltage. The resultant voltage is measured by the delta-sigma ADC.

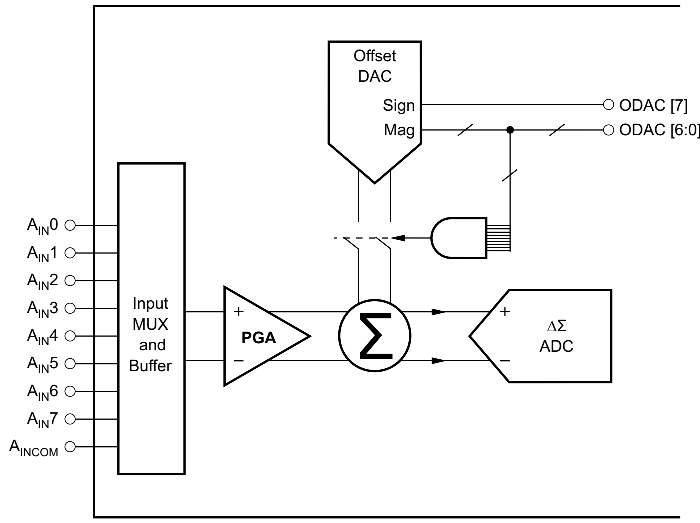

Figure 1. Offset Block Diagram

The offset DAC ODAC register sets the value of the offset DAC voltage. Bit 8 of the ODAC register sets the sign, whether the output voltage is negative or positive. The lower 7 bits set the magnitude as a percentage of the full-scale input range. When the magnitude is set to 0, the offset DAC is disabled. When the magnitude is set to all ones (127), the offset DAC outputs a value of 50% of the full-scale input range. Table 1 shows the offset DAC output for different ODAC values.

Table 1. Offset DAC Output

ODAC REGISTER VALUE	OFFSET DAC OUTPUT[(1)] (% OF FS INPUT)
0 000000 (00_H)	0%
0 000001 (01_H)	0.4%
0 111111 ($0F_H$)	50%
1 000000 (80_H)	0%
1 000001 (81_H)	–0.4%
1 111111 (FF_H)	–50%

(1) For the ADS1240, ADS1241, ADS1242, and ADS1243, the output voltage of the offset DAC has a different magnitude when the RANGE bit within the ACR register = 1 and PGA = 128. See Table 3 and Table 4 for the values in this case.

To refer the offset DAC output voltage back to the input, use the full-scale input range. Table 2 shows the “input-referred” offset DAC voltages for full-scale input ranges of 2.5 V, 0.625 V and 156 mV. It doesn’t matter how the full-scale input range is set. For example, the offset DAC will produce the same input-referred voltages for an ADS1216 with (V_{REF} = 2.5V, PGA = 1) or (V_{REF} = 1.25V, PGA = 2).

Table 2. Offset DAC Output, Input-Referred

ODAC REGISTER VALUE	OFFSET DAC VOLTAGE, INPUT-REFERRED		
	FS INPUT = 2.5 V	FS INPUT = 0.625 V	FS INPUT = 156 mV
0 000000 (00_H)	0	0	0
0 000001 (01_H)	0.0098	0.002461	0.615
0 111111 ($0F_H$)	1.25	0.3125	78.125

Table 2. Offset DAC Output, Input-Referred (continued)

ODAC REGISTER VALUE	OFFSET DAC VOLTAGE, INPUT-REFERRED		
	FS INPUT = 2.5 V	FS INPUT = 0.625 V	FS INPUT = 156 mV
1 000000 (80_H)	0	0	0
1 000001 (81_H)	–0.0098	–0.002461	–0.615
1 111111 (FF_H)	–1.25	–0.3125	–78.125

Table 3. Offset DAC Output for ADS1240, ADS1243 with RANGE Bit = 1 and PGA = 128

ODAC REGISTER VALUE	OFFSET DAC OUTPUT (% OF FS INPUT)
0 000000 (00_H)	0%
0 000001 (01_H)	0.8%
0 111111 ($0F_H$)	100%
1 000000 (80_H)	0%
1 000001 (81_H)	–0.8%
1 111111 (FF_H)	–100%

Table 4. Offset DAC Output, Input-Referred for ADS1240, ADS1243 with RANGE Bit = 1 and PGA = 128

ODAC REGISTER VALUE	OFFSET DAC VOLTAGE, INPUT-REFERRED	
	FS INPUT = 19.5 mV	FS INPUT = 9.77 mV
0 000000 (00_H)	0	0
0 000001 (01_H)	0.154	0.077
0 111111 ($0F_H$)	19.531	9.765
1 000000 (80_H)	0	0
1 000001 (81_H)	–0.154	–0.077
1 111111 (FF_H)	–19.531	–9.765

2 Use And Performance

The offset DAC can correct positive or negative input offsets up to 50% of the full-scale input range. To see its benefit, consider the following application: Using an ADS1216 with a reference voltage of 2.5 V, measure a 0 to 50 mV signal. With a 2.5-V reference, the ADS1216 has a full-scale input range of ±78 mV for PGA = 32, or ±39 mV for PGA = 64. Without the offset DAC, the PGA must be set to 32 or lower to avoid overloading the ADC. However, by using the offset DAC set to –20 mV, the input shifts from 0 to 50 mV down to –20 mV to 30 mV. A PGA of 64 can now be used, allowing a higher resolution measurement.

System- or self-calibration commands do not affect the offset DAC. When doing self-calibrations (SELFCAL, SELFOCAL, or SELFGCAL), be sure to turn off the offset DAC by setting ODAC = 00_H . Otherwise, the calibration will be affected by the offset DAC output voltage.

Figure 2 shows the rms noise in ppm of full-scale versus offset DAC setting. The noise gets markedly better when using the offset DAC. The noise is lowest when the offset DAC's output is maximum. The ADC's integral nonlinearity error, when is unaffected by the offset DAC and the gain error drift of the offset DAC output voltage, is typically 1ppm/°C.

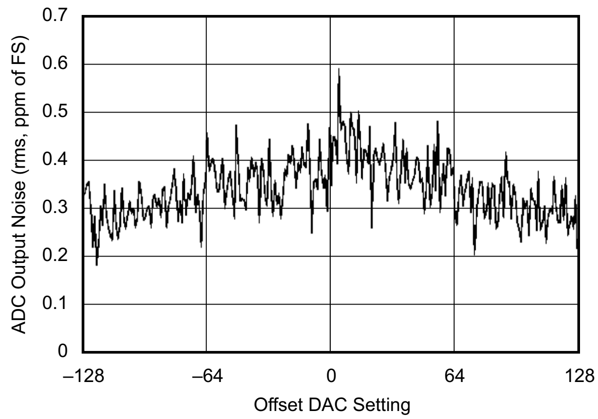

Figure 2. ADC Output Noise vs Offset DAC Setting

3 Self-Test

The offset DAC is basically a second input source to the ADC. As a result, it can also serve as a signal generator for a self-test function. To do this, program the MUX so as to disconnect the normal inputs and sweep the ADC's input using the offset DAC. The host controlling the ADC will then collect this data and perform the necessary checks to insure proper functionality.

Figure 3 shows ADC data collected with the normal inputs disconnected and the offset DAC stepped from its most negative to its most positive setting. The inputs were disconnected by setting the MUX register to 88_H; this connects both MUX outputs to A_{INCOM}. Then, the ODAC register was decremented from FF_H to 00_H, collecting data at each step. At 00_H, ODAC was incremented up to $7F_H$, again collecting data after each step.

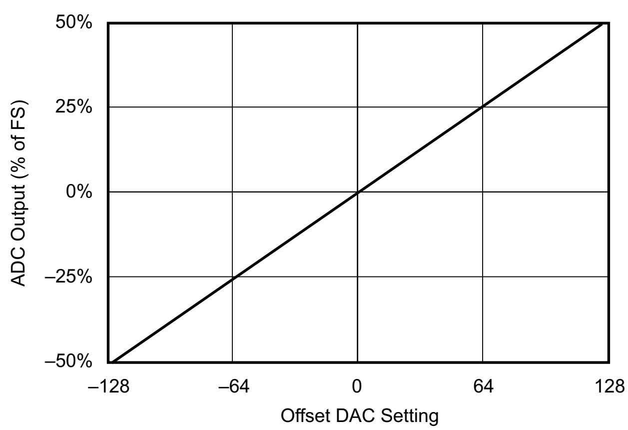

Figure 3. ADC Output vs Offset DAC Setting

To measure the quality of the offset DAC as an input source, the data in Figure 3 was fit with a line going through the end points. The differential nonlinearity (DNL) and integral nonlinearity (INL) of intermediate points were then measured in units of offset DAC LSBs against this line. Figure 4 shows the DNL error versus offset DAC setting. Figure 5 shows the INL error versus offset DAC setting.

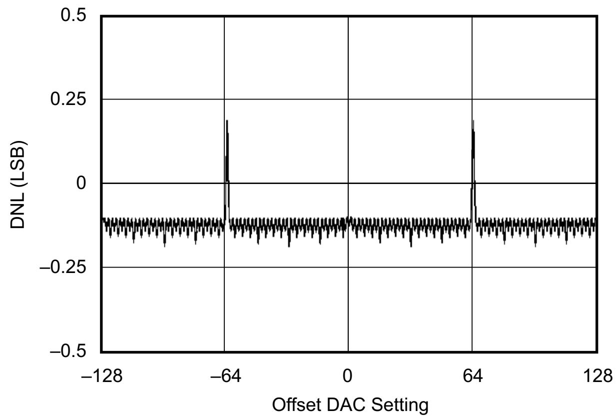

Figure 4. DNL vs Offset DAC Setting

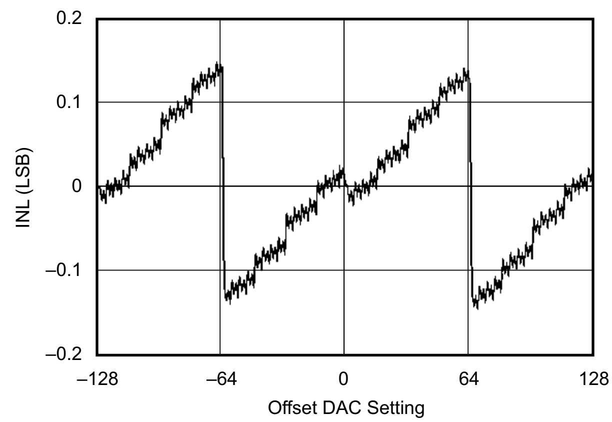

Figure 5. INL vs Offset DAC Setting

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