

Calibration Routines and Register Value Generation for the ADS1216, ADS1217 and ADS1218

Joseph Wu
Data Acquisition Group

ABSTRACT

In order to achieve the best possible performance, offset and gain can be often be calibrated in high-resolution analog-to-digital converters (ADCs). Changes in temperature, PGA gain, power supply voltage, or most importantly, decimation ratio can influence the accuracy of measurement. This application note explains how the calibration routines work and how to generate values for the full-scale register (FSR) and the offset calibration register (OCR) in the ADS1216, ADS1217, and ADS1218 family of ADCs.

These delta-sigma ($\Delta\Sigma$) ADCs rely on five different codes to perform two different types of calibration. First, there are three self-calibration routines: SELFOCAL, SELFGCAL, and SELFCAL. There are also system calibration routines: SYSOCAL and SYSGCAL. Each of these calibrations will have an effect on the FSR, OCR, or both. Delta-sigma ADCs use oversampling as a means to obtain high resolution. These 24-bit, 8-channel components offer precision and a wide dynamic range operating from 2.7V to 5.25V supplies. Internal buffers create high-impedance inputs, allowing for direct connections to transducers or low-level voltage signals.

The first product in this family is the ADS1216, which has an input range of $\pm V_{REF}$ (in PGA gain = 1). The ADS1218 features an additional 4kBytes of FLASH memory. The ADS1217 is similar to the ADS1216, except the input range is doubled to $\pm 2V_{REF}$ (in PGA gain = 1).

This application note also applies to the MSC1210, MSC1211, and MSC1212, which incorporate a similar 8-channel ADC.

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1 Calibration

Calibration can be influenced by changes in the operation of the ADS1216, ADS1217, and ADS1218. Variations in temperature, PGA gain, reference voltage, or decimation ratio can affect the expected values in the Offset Calibration Register (OCR) and Full Scale Register (FSR). The output of the digital filter is modified by both values before sending the data to the Data Output Register (DOR).

The ADS1216, ADS1217, and ADS1218 each have two groups of calibration codes, self-calibration and system calibration. There are five separate calibration codes for this family of devices. These codes are detailed in Sections 1.1 and 1.2.

1.1 Self Calibration

The first type of calibration in the ADS1216, ADS1217 or ADS1218 is an internal or self-calibration. There are three self-cal codes. Note that some of these comments are taken directly from the relevant datasheets. (See *References* for complete information.)

SELFOCAL – In the self-offset calibration, both inputs to the converter are internally tied to the AINCOM line. The input is thus zeroed. The OCR then records the output of the digital filter. Future readings subtract the contents of this register from the digital filter output. This calibrates for internal inherent offset errors in the part.

SELFGCAL – The self-gain calibration is used to calibrate for the gain in the part. The converter inputs are internally tied to the V_{REF+} and V_{REF-} lines, and the converter assumes the inputs to be the positive full-scale for the ADS1216 and ADS1218 (for the ADS1217 it is assumed to be 1/2 of the positive full-scale because of its larger input range). SELFGCAL compensates for gain errors that come from the digital filter and updates the FSR. In PGA gain other than 1, circuitry compensates to scale the reference.

SELFCAL – The self-calibration routine runs a SELFOCAL and then a SELFGCAL. This updates both the OCR and FSR.

1.2 System Calibration

The other type of calibration is an external or system calibration. In these calibration routines, the appropriate signal must be put onto the selected inputs.

SYSOCAL – In the system offset calibration, the user must select the input channels, zero the inputs and then run the SYSOCAL command. This allows the user to calibrate out any offset errors associated with the entire system. This command updates the OCR.

SYSGCAL – For system gain calibration, the user must select the input channels, supply the positive full-scale input, and then run the SYSGCAL command. This command updates the FSR.

2 Digital Filter and Calibration Register Details

ADS1216, ADS1217, and ADS1218 all have a digital filter that can run in one of four modes selectable in the Mode and Decimation Register. Each mode is based on a $\sin(x)/x$ or a sinc filter. The fast settling filter (FS) settles in one t_{data} period. The sinc^2 filter (S2) has lower noise and settles in two t_{data} periods. The sinc^3 filter (S3) has even lower noise but settles in three t_{data} periods. The final mode of operation is the auto mode. In this mode, the output of the digital filter is such that the first two data reads come from FS, the third comes from S2, and the fourth and subsequent reads come from S3. For more on these modes of operation, see the respective datasheets. Calibration for first two modes of digital filtering will be noisier and result in less accurate values in the OCR and FSR.

The digital filter is the key to all calibrations. The digital filter gain changes as the decimation ratio changes. The OCR zeroes the offset of the input circuitry and modulator up to the digital filter while the FSR calibrates for full-scale changes that come from changes in the decimation ratio. Calibration for either offset or gain requires $7t_{data}$ periods (a SELFCAL which does both an offset and gain calibration will therefore take $14t_{data}$ periods). This is because in both cases, the input is sampling either the zeroed offset or the V_{REF} . To get the best values for the register, seven samples are taken from the filter. The first three are discarded and the latter four are averaged. The digital filter and the implementation of the OCR and FSR registers are shown in Figure 1.

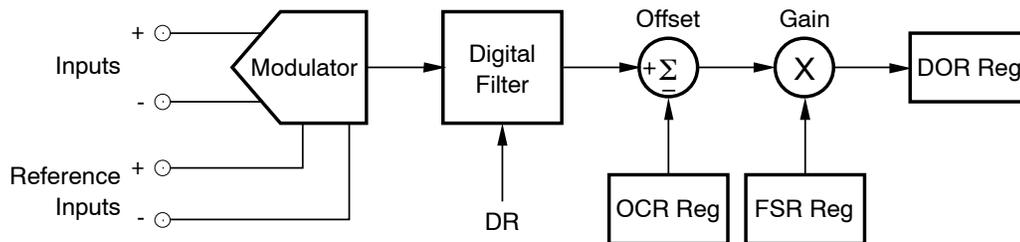


Figure 1. Digital Filter and Calibration Registers of the ADS1216, ADS1217, and ADS1218

The output of the modulator is sent to the digital filter where it is scaled by a function of the decimation ratio (DR). The value of the OCR register is then subtracted from the output of the digital filter. FSR is then multiplied to get the DOR.

First, the digital filter gain is applied to the modulator output. The digital filter gain (DFG) is a function of decimation ratio and is given by the equation below.

$$DFG = \frac{3}{4}(DR^3 \cdot 2^A) \quad (1)$$

In addition to the decimation ratio, the digital filter gain is also affected by a scale factor to align the digits of the digital filter for low decimation ratios. This is given in the above equation as A . The factor A is an integer number that is also determined by the decimation ratio listed in Table 1. Given a decimation ratio, the table shows what value of A to use. Decimation ratios not given in the table must be rounded up to get A (for example, DR of 1000 rounds to 1023 and uses $A = -7$).

TABLE 1. Digital Filter Gain for a Given Decimation Ratio

DR	A	DFG (multiply by DR ³)
20	10	768
25	9	384
31	8	192
40	7	96
50	6	48
63	5	24
80	4	12
101	3	6
127	2	3
161	1	1.5
203	0	0.75
255	-1	0.375
322	-2	0.1875
406	-3	0.09375
511	-4	0.046875
645	-5	0.0234375
812	-6	0.01171875
1,023	-7	0.005859375
1,290	-8	0.002929688
1,625	-9	0.001464844
2,047	-10	0.000732422

After the digital filter, the value of the OCR is subtracted. In a calibration, the OCR is generated during an offset calibration cycle, where the inputs are tied to what is expected to be a zero offset. The output of the digital filter is recorded into the OCR register. This offset value is then subtracted from subsequent readings. Figure 2 illustrates the offset calibration process.

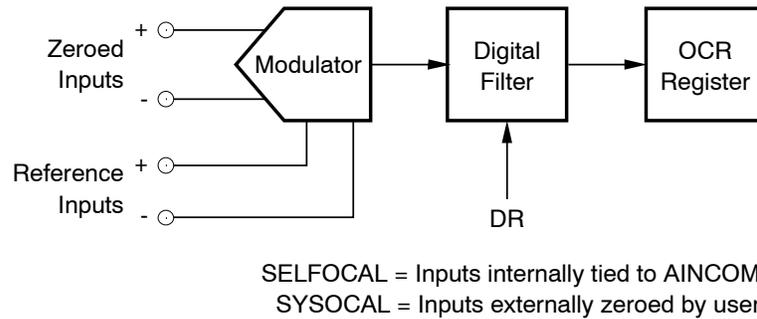
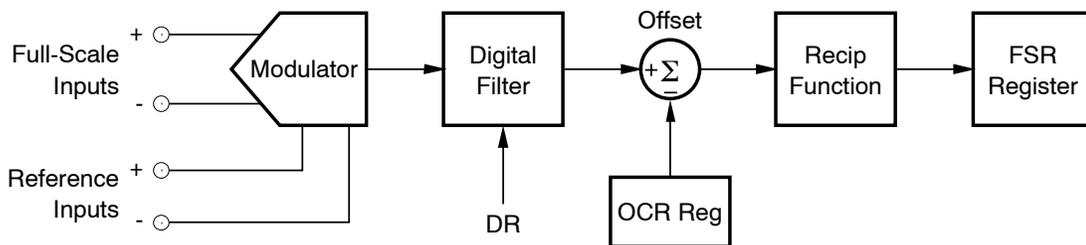


Figure 2. Generation of the OCR Register Value in Calibration

After the OCR is subtracted, the FSR is multiplied to get the output data. The FSR aligns the full scale to the reference voltage. During a gain calibration, the inputs are set to the reference voltage (for the ADS1216 and ADS1218, this is the positive full scale; for the ADS1217, this is 1/2 of the positive full scale). The output of the digital filter during a gain calibration has the OCR subtracted, and this value is used to calibrate the output to a positive full scale. By using a reciprocal function, the FSR is calculated. Mathematically, the output of the digital filter, with the OCR subtracted out, is divided from h1FFFFFFFFFFFF. This process is given in the equation below and is illustrated by the diagram in Figure 3.

$$FSR = \frac{h1FFFFFFFFFFFF}{DigitalFilterOutput - OCR} \quad (2)$$



SELFGCAL = Inputs internally tied to scale of V_{REF} .
SYSGCAL = Inputs externally tied to a positive full-scale.

Figure 3. Generation of the FSR Register Value in Calibration

For different PGA gains, note that in a self-gain calibration, the inputs are internally set to a scale of V_{REF} . In a system gain calibration, the inputs should be set to the proper positive full scale, depending on PGA gain and reference voltage.

In the offset calibration, the input is set to zero and the OCR is found with whatever V_{in} the modulator sees. The FSR is independent of offset calibration. In gain calibrations, the modulator inputs are set to V_{REF+} and V_{REF-} , FSR is calculated to ensure that the output reads positive full scale (the DOR reads h7FFFFFFF).

Now, with some understanding of how the OCR and FSR registers are calculated and used, the equations for the DOR can be found. For the ADS 1216 and ADS1218 they are:

$$DOR = \left[\left(\frac{V_{in}}{V_{REF}} \cdot DFG \right) - OCR \right] \cdot \frac{FSR}{2^{22}} \quad \text{in bipolar mode and} \quad (3)$$

$$DOR = \left[\left(\frac{V_{in}}{V_{REF}} \cdot DFG \right) - OCR \right] \cdot \frac{FSR}{2^{21}} \quad \text{in unipolar mode.} \quad (4)$$

For the ADS1217 it is:

$$DOR = \left[\left(\frac{V_{in}}{2 \cdot V_{REF}} \cdot DFG \right) - OCR \right] \cdot \frac{FSR}{2^{22}} \quad \text{in bipolar mode and} \quad (5)$$

$$DOR = \left[\left(\frac{V_{in}}{2 \cdot V_{REF}} \cdot DFG \right) - OCR \right] \cdot \frac{FSR}{2^{21}} \quad \text{in unipolar mode} \quad (6)$$

3 Examples

Here are a few examples to illustrate how the OCR and FSR are determined.

Example 1

An ADS1217 is running in bipolar mode with a reference input of 2.5V, an offset of 0V, and a decimation ratio of 625. A SELFCAL is run (which is the same as running a SELFOCAL and then a SELFGCAL in sequence).

With the inputs at 0V, OCR is determined to be ideally h000000. The FSR, however, is calculated by working backward from the reciprocal function:

$$FSR = (h1FFFFFFFFFFFF) / (DFG - OCR) \quad (7)$$

The FSR = [(h1FFFFFFFFFFFF)/((.75*625³*2⁻⁵)-h000000)] = h5DD332.

Example 2

An ADS1216 is running in unipolar mode with a reference input of 1.25V and a decimation ratio of 200. However, the user accidentally puts in an input of 0.5V across channels AIN0 and AIN1, selects those channels, and runs a SYSOCAL and then a SELFGCAL. The large error in the offset causes an error in the gain calibration.

$$OCR = \frac{V_{in}}{V_{REF}} \cdot DFG \quad (8)$$

Here the OCR = (0.5/1.25)*(0.75*200³*2⁰) = 2400000 = h249F00.

The FSR = [(h1FFFFFFFF)/((.75*200³*2⁰)-h249F00)] = h95217C.

This was meant to illustrate that an error in the OCR can cause an error in the calculation of the FSR.

Example 3

Realizing the mistake in Example 2, the user properly zeroes the input (but has a system offset of 5mV), and then runs the same SYSOCAL and SELFGCAL.

Using Equation 8, the OCR = (0.005/1.25)*(0.75*200³*2⁰) = d24000 = h005DC0.

Then the SELFGCAL internally switches in the reference and calibrates the gain. Using Equation 7, the FSR = [(245-1)/(.75*200³*20)] = h1FFFFFFFF/h5B8D80 = h597A7E.

4 Conclusion

For most cases, the user should not have to bother with details of how and why calibration works. These parts were designed to have a simple calibration through a few select commands. However, it is important to understand where these calibration coefficients come from when things are not working as expected. Calculations deriving the OCR and FSR register contents can help debug problems as they arise. Also included with this Applications Note are a few general notes on calibration that the user should consider when using these parts, as well as a glossary of important terms used in this document.

5 Calibration Notes

Here are a few notes on calibration that may be helpful in using the ADS1216, ADS1217 or ADS1218.

1. Calibration must be done to account for changes in the decimation ratio. The gain of the digital filter varies with the decimation ratio. Therefore, if the decimation ratio changes, the digital filter gain changes. The FSR value is then off from the last calibration, yielding the wrong gain. Similarly, the offset is affected by changes in the calibration.
2. PGA changes require a calibration. This change benefits offset calibrations more. In higher gains, the FSR value from a gain calibration may be subject to more noise. See the appropriate datasheet for noise in measurement in different PGA gains.
3. Temperature changes may require a calibration. This becomes important if the drift performance is important. The input offset, reference voltage, and gain error can all be influenced by the temperature.
4. Power supply changes may require a calibration. This is likely to change the same parameters that temperature does.
5. Calibration for either offset or gain requires $7t_{\text{data}}$ periods. This is for either a self or a system calibration. A SELFCAL command will require the part to go through a SELFOCAL and a SELFGCAL, requiring $14t_{\text{data}}$ periods.
6. The input buffer can affect a system gain calibration. Since the system calibrations use the same lines as the analog inputs, this is subject to the same restrictions. If the input buffer is on, and V_{REF} is sampled for the SYSGCAL, the signal should be within the input operating range of the buffers. That is, V_{REF} should be between $\text{AGND}+0.05\text{V}$ to $\text{AVDD}-1.5\text{V}$.
7. Using the auto mode or sinc³ filter is best for calibration. Calibration will take time, regardless of whatever filter is used. Since the sinc³ filter is the least noisy, it is best to use that for calibration; once you get the best values for the OCR and FSR, then switch back to whatever filter you decide to use for reading data.
8. The PGA Offset DAC (ODAC) can affect calibration. The ODAC shifts the input to the PGA by as much as half of the full scale input range. This input shift can affect the calibration of the part by appearing as an offset error, and should be set after calibration.

6 Glossary

A – Exponential factor used to calculate the DFG

DFG – Digital Filter Gain

DOR – Data Output Register

DR – Decimation Ratio

FSR – Full Scale Register

MSB – Most Significant Bit

OCR – Offset Calibration Register

ODAC – Offset DAC

SELFCAL – Self-Calibration in which a SELFOCAL is run and then a SELFGCAL is run

SELFGCAL – Self-Gain Calibration

SELFOCAL – Self-Offset Calibration

SYSGCAL – System Gain Calibration

SYSOCAL – System Offset Calibration

7 References

ADS1216 Product Data Sheet (SBAS171B)

ADS1217 Product Data Sheet (SBAS260)

ADS1218 Product Data Sheet (SBAS187)

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