

LVDS Outputs on the ADS527x

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ABSTRACT

The ADS527x are a family of high-performance analog-to-digital converters (ADCs) that feature serialized low-voltage differential signaling (LVDS) outputs. Data in each channel are serialized and sent out on a pair of pins in LVDS format. In addition to reducing the pincount and package size of the multi-channel ADC, serialization also eases the routing of ADC outputs of the multiple channels to the receiver. The LVDS architecture offers multiple advantages, such as reduced effects of digital noise coupling to the internal analog circuit of the device. The serializer that provides data to the LVDS buffer also generates a 1x clock and a 6x clock, which are used for frame and bit identification, respectively. This application note describes the implementation of LVDS timings inside the ADS527x. The generation of the data and clock outputs from an internal 12x clock are detailed. It also discusses a method of specifying the LVDS timings from the standpoint of the receiver. Unless otherwise noted, this report refers to the ADS5270, ADS5271, ADS5272 and ADS5273 as the ADS527x.

LVDS Implementation

The ADS5270 uses an integrated internal PLL that generates a 12x sampling clock. The edges of this 12x clock are used to serialize the ADC data bits. The 12x sampling clock also generates the LVDS bit clock and the LVDS frame clock, which are output synchronously with the serialized data. The edges of the 12x clock are used as shown in Figure 1.

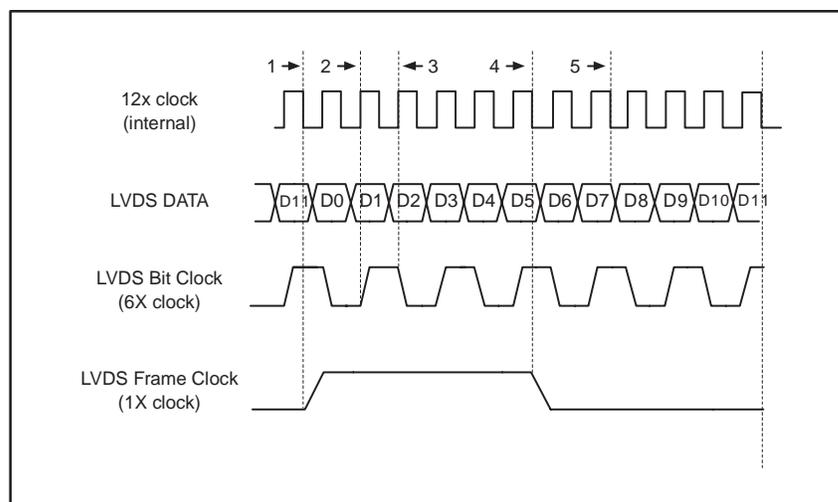


Figure 1. Generation of LVDS Data and Clocks from the Edges of the Internal 12x Sample Clock

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Both the rising and the falling edges of the internal 12x clock are used for generating the LVDS bit clock (6x clock) and the LVDS frame clock (1x clock). The rising edges of the 12x clock are used to generate both the rising as well as falling edges of LVDS bit clock (arrows 2 and 3, respectively). The falling edges of the 12X clock are used to generate the switching instances of the data (arrow 5), as well as the rising and falling edges of the LVDS frame clock (arrows 1 and 4, respectively). The logic delays used in generating the transitions of all the data and clocks are closely matched. As a result of the matching design, the transition of the LVDS bit clock edge is expected to occur very close to the middle of the open eye of the data.

Setup and Hold Times

The setup and hold times are defined with respect to the transitions between the data and the LVDS bit clock (6x clock). Since the data is to be captured using both edges of the LVDS bit clock, one setup and hold time period can be defined with respect to the rising edge of the LVDS bit clock while another period can be defined with respect to the falling edge. There could be slight differences between the timings related to the two edges because of the slight differences in the rise and fall times during the generation of the logic for the LVDS bit clock. Such a difference would be on the order of 50ps. To simplify the timing specification, a single set of setup and hold times are indicated in the product data sheet, reflecting the lower value of the setup and hold times for either the rising or falling edge.

Figure 2 illustrates the method of measuring the setup and hold times from the differential waveforms of the LVDS bit clock and data.

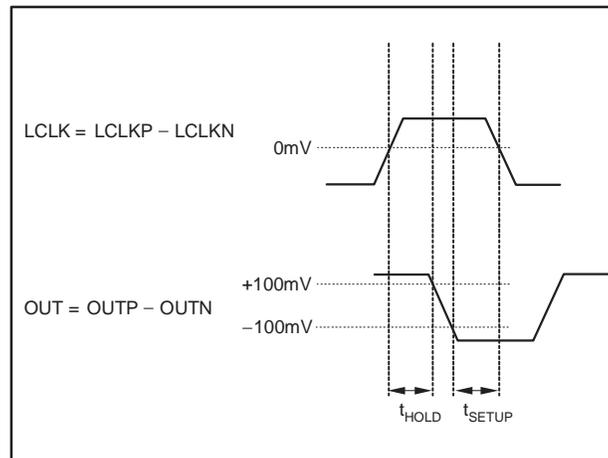


Figure 2. Setup and Hold Times

The rise and fall instances of the LVDS data are referenced to $\pm 100\text{mV}$, since these are the typical thresholds required for the receiver to identify them as logic levels. The rising time of the LVDS data waveform is measured as the time taken to swing from -100mV to $+100\text{mV}$ (and vice-versa for the falling time).

Jitter

A typical eye pattern of the LVDS waveforms is shown in Figure 3. The waveforms in Figure 3 are plotted using a high bandwidth oscilloscope in infinite persistence mode. The time for which the eye is *open* is a measure of the available setup and hold times available to the receiver. Typically, the LCLK rising and falling edges occur in the middle of the eye pattern of the data, thereby producing roughly equal setup and hold times.

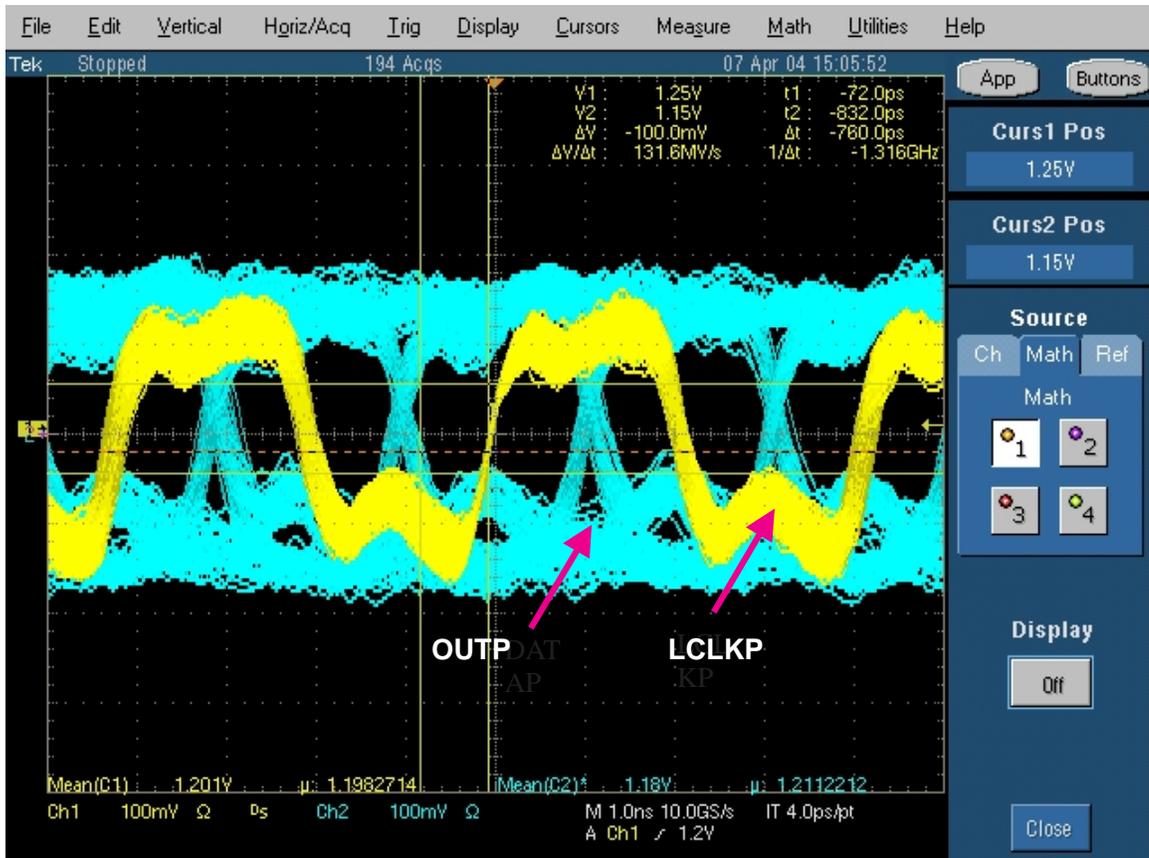


Figure 3. Eye Pattern of the LVDS Clock and Data

The jitter effectively reduces the timing margins available to the receiver and can result in bit errors. The timing numbers for the setup and hold times as mentioned in the datasheet are representative of the actual timing margins available to the receiver, and take into account the effect of jitter. The setup and hold time values can be improved by increasing the LVDS current setting to 4.5mA or 6mA. This current setting increase produces faster rise and fall times, thus increasing the open time of the eye pattern.

References

ADS5270 Datasheet (SBAS293D)

ADS5271 Datasheet (SBAS313)

ADS5272 Datasheet (SBAS324)

ADS5273 Datasheet (SBAS305B)

To obtain a copy of the referenced documents, visit the Texas Instruments web site at www.ti.com. x indicates the current revision letter for each document.

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