Single-ended-to-differential circuit using an op amp and fully-differential amplifier (FDA) for bipolar signals

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### Design Description

This design is intended to demonstrate how to convert a bipolar, single-ended signal into a unipolar, fully-differential signal and drive a differential ADC (for more information on these and other signal types, please refer to the TI Precision Labs training titled **SAR ADC Input Types**). Compared to a single-ended device, a fully-differential ADC has twice the dynamic range which improves the AC performance of the converter. Many common systems, for example **Sonar Receivers**, **Flow Meters**, and **Motor Controls**, benefit from the higher performance of a differential ADC. The equations and explanation of component selection in this design can be customized based on system specifications and needs. For more information on a similar design using a unipolar input signal, see the cookbook circuit titled **Single-Ended to Differential Signal Conversion for Unipolar Inputs**.
Specifications

<table>
<thead>
<tr>
<th>Specification</th>
<th>Calculated</th>
<th>Simulated</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transient ADC Input Settling (at 250ksps)</td>
<td>&lt; 0.5 • LSB = 201µV</td>
<td>134.7µV</td>
</tr>
<tr>
<td>Conditioned Signal Range (at 250ksps)</td>
<td>&gt; 99% ADC FSR = &gt; 6.53V</td>
<td>6.60V</td>
</tr>
<tr>
<td>Noise</td>
<td>43.8µV / √Hz</td>
<td>44.3µV / √Hz</td>
</tr>
</tbody>
</table>

Design Notes

1. The ADS7057 was selected because of its throughput (2.5Msps), size (2.25mm²) and low-latency (successive approximation register, or SAR, architecture).
2. Determine the linear range of the fully-differential amplifier (ADC driver) based on common mode, output swing, and linear open-loop gain specification. This is covered in the component selection section.
3. Determine the linear range of the op amp (signal conditioning) based on common mode, output swing, and linear open-loop gain specification. This is covered in the component selection section.
4. Select COG (NPO) capacitors for $C_{\text{filt}}$, to minimize distortion.
5. For best performance, consider using a 0.1% 20ppm/°C film resistor, or better, to minimize distortion.
6. The TI Precision Labs - ADCs training video series covers methods for selecting the charge bucket circuit $R_{\text{filt}}$ and $C_{\text{filt}}$. These component values are dependent on the amplifier bandwidth, data converter sampling rate, and data converter design. The values shown here will give good settling and AC performance for the amplifier and data converter in this example. If the design is modified, a different RC filter must be selected. Refer to Introduction to SAR ADC Front-end Component Selection (a TI Precision Labs training video) for an explanation of how to select the RC filter for best settling and AC performance.
Component Selection

1. Select a fully-differential amplifier capable of driving the ADC:
   THS4551 – Low noise, precision, 150MHz, fully-differential amplifier
   - Wide input common-mode voltage:
     \[ V_{\text{in}} - 0.1\,V < V_{\text{cm}} < V_{\text{in}} + 1.3\,V \]
   - Linear output (requirement: 0V to 3.3V at each output):
     \[ V_{\text{out}} < V_{\text{out}} < V_{\text{in}} - 0.22\,V \]

2. Select a wide bandwidth operational amplifier:
   OPA320 – Precision, zero-crossover, 20MHz, RRIO, operational amplifier
   - Gain bandwidth product > 12.5MHz (> 5 times the sampling rate)
   - Input common-mode voltage (requirement: ±1.65V):
     \[ V_{\text{in}} - 0.1V < V_{\text{cm}} < V_{\text{in}} + 0.1V \]
   - Linear output:
     \[ V_{\text{out}} + 0.03V < V_{\text{out}} < V_{\text{in}} - 0.03V \]
     \[ V_{\text{out}} + 0.2V < V_{\text{out}} < V_{\text{in}} - 0.2V \]
   - Combined worst-case linear range (calculated from supplies used with OPA320):
     \[ -2.3V < V_{\text{out}} < 2.3V \]

   **NOTE:** The operational amplifier is used to protect the sensor from any charge kickbacks that occur when the ADC connects or disconnects the sampling capacitor. This amplifier may not be needed if the sensor has a high output impedance. A negative rail is used for both the OPA320 and THS4551 based on the assumption that the sensor is operating with a negative rail. This also ensures the highest performance from the ADC by providing the full scale input range.

3. Select \( R_{\text{fx}} \) and \( R_{\text{gx}} \)
   - The combination of \( R_{\text{fx}} \) and \( R_{\text{gx}} \) sets the gain of the system. With an input range of ±1.65V and an ADC full scale of ±3.3V, a gain of 2 was selected for this system.
   - The values of \( R_{\text{fx}} = 2k \) and \( R_{\text{gx}} = 1k \) were selected to both provide the desired gain as well as limit the current through the feedback network, thus minimizing power consumption of the system.

4. Select \( R_{\text{sx}} \)
   - It is important to connect small resistors at the output of the amplifier, in this case 10Ω, to flatten the output impedance and improve stability of the system.

5. Select \( R_{\text{f}} \) and \( C_{\text{f}} \) values for settling of 250-kHz input signal and sample rate of 2.5Msps:
   - **Refine the \( R_{\text{f}} \) and \( C_{\text{f}} \) Values** is a TI Precision Labs video showing the methodology for selecting \( R_{\text{f}} \) and \( C_{\text{f}} \). The final value of 18.2Ω and 330pF proved to settle to well below \( \frac{1}{2} \) of a least significant bit (LSB) within the acquisition window.
DC Transfer Characteristics

The following graph shows the simulated output for a ±1.65-V input. The analog front end has a linear output of ±3.3V which matches the full-scale range (FSR) of the ADC (with AVDD = 3.3V).

![DC Transfer Characteristics Graph]

AC Transfer Characteristics

The bandwidth of the analog front end is simulated to be 4.12MHz at the gain of 0dB which is a linear gain of 1. This bandwidth will allow the inputs of the ADC to adequately settle for a 250-ksp signal.
Transient ADC Input Settling Simulation

The following simulation shows the ADC sample and hold capacitor settling for a 3.3-V DC input signal. This simulation shows that the analog front end is able to drive the ADC with a large step input (from 0V to 3.3V) so it settles to within ¼ of an LSB (approximately 200µV) in the allotted acquisition time (95ns). Refer to *Introduction to SAR ADC Front-End Component Selection* for detailed theory on this subject, and follow the link at the end of this design to download these simulation files.
Noise Simulation

This section walks through a simplified noise calculation, providing a rough estimate to compare with the simulated result. The resistor noise is included in this calculation as it is a significant portion of the overall noise of the system. Note that the resistor noise can be reduced by using smaller value resistors, but at the expense of increased power consumption through the feedback network.

\[
\begin{align*}
    f_c &= \frac{1}{2 \pi \times R_j \times C_{j}} = \frac{1}{2 \pi \times 2k \Omega \times 30 \text{pF}} = 2.65 \text{MHz} \\
    E_n &= e_{\text{OPA320}} \times \sqrt{2 \times K_n \times f_c} = \left(7nV / \sqrt{\text{Hz}} \right) \times \sqrt{2 \times 1.57 \times 2.65 \text{MHz}} = 20.2 \mu V / \sqrt{\text{Hz}} \\
    E_{n, \text{THS4551}} &= e_{\text{THS4551}} \times \sqrt{2 \times K_n \times f_c} = \left(3.3nV / \sqrt{\text{Hz}} \right) \times \sqrt{2 \times 1.57 \times 2.65 \text{MHz}} = 9.52 \mu V / \sqrt{\text{Hz}} \\
    E_{R_f} &= \sqrt{4 \times k \times T \times R_f} \times \frac{R_i}{R_g} \times \sqrt{2} = \sqrt{4 \times 1.38 \times 10^{-23} \times (273.15 + 25) \times 1000} \times \frac{2000}{1000} \times \sqrt{2} = 11.47 \mu V / \sqrt{\text{Hz}} \\
    E_{R_g} &= \sqrt{4 \times k \times T \times R_g} \times \frac{R_i}{R_f} \times \sqrt{2} = \sqrt{4 \times 1.38 \times 10^{-23} \times (273.15 + 25) \times 2000} \times \sqrt{2} = 8.11 \mu V / \sqrt{\text{Hz}} \\
    \text{Total noise at output equation:} \\
    E_n &= \sqrt{E_{n, \text{OPA320}}^2 + E_{n, \text{THS4551}}^2 + E_{R_f}^2 + E_{R_g}^2} = \sqrt{40.4^2 + 9.52^2 + 11.47^2 + 8.11^2} = 43.8 \mu V / \sqrt{\text{Hz}}
\end{align*}
\]

Note that calculated and simulated match well. Refer to the TI Precision Labs - ADCs training video series for detailed theory on this subject.
Design Featured Devices

<table>
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<th>Device</th>
<th>Key Features</th>
<th>Link</th>
<th>Similar Devices</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADS7057</td>
<td>14 bit, 2.5 Msps, fully-differential input, SPI, 2.25mm² package</td>
<td><a href="http://www.ti.com/product/ADS7057">www.ti.com/product/ADS7057</a></td>
<td><a href="http://www.ti.com/adcs">www.ti.com/adcs</a></td>
</tr>
<tr>
<td>THS4551</td>
<td>150-MHz, 3.3-nV/√Hz input voltage noise, fully-differential amplifier</td>
<td><a href="http://www.ti.com/product/THS4551">www.ti.com/product/THS4551</a></td>
<td><a href="http://www.ti.com/opamp">www.ti.com/opamp</a></td>
</tr>
<tr>
<td>OPA320</td>
<td>Precision, zero-crossover, 20-MHz, 0.9-pA Ib, RRIO, operational amplifier</td>
<td><a href="http://www.ti.com/product/OPA320">www.ti.com/product/OPA320</a></td>
<td><a href="http://www.ti.com/opamp">www.ti.com/opamp</a></td>
</tr>
</tbody>
</table>

**NOTE:** The ADS7057 uses the AVDD as the reference input. Use a high-PSRR LDO, such as the TPS7A47, as the power supply.

Design References

See Analog Engineer's Circuit Cookbooks for TI's comprehensive circuit library.

**Link to key files (TINA):**

**Link to Related Cookbooks**
Single-Ended to Differential Signal Conversion for Unipolar Input

Revision History

<table>
<thead>
<tr>
<th>Revision</th>
<th>Date</th>
<th>Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>March 2019</td>
<td>Downstyle the title and changed title role to 'Data Converters'.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Added link to circuit cookbook landing page.</td>
</tr>
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