Circuit for driving high-voltage SAR ADCs for high-voltage, true differential signal acquisition

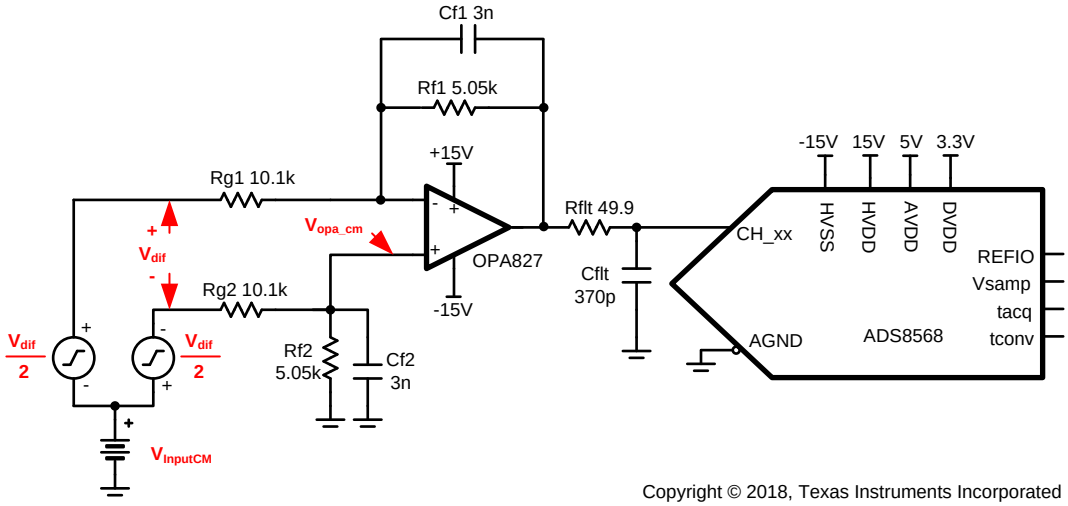
Dale Li

Input	ADC Input	Digital Output ADS7042
VinDiffMin = –20V	CH_x = +10V	7FFF $_{H}$, or 32767 $_{10}$
VinDiffMax = +20V	CH_x = –10V	8000 $_{H}$, or 32768 $_{10}$

Power Supplies			
AVDD	**DVDD**	**V_{CC} (HVDD)**	**V_{SS} (HVSS)**
5.0V	3.3V	+15V	–15V

Design Description

This design shows a solution to drive high-voltage SAR ADC to implement data capture for high-voltage fully differential signal which may have a wide common-mode voltage range depended on amplifier's power supply and input signal's amplitude. A general high-voltage precision amplifier performs the differential to single-ended conversion and drives high-voltage SAR ADC single-ended input scale of ±10V at highest throughput. This type of application is popular in end equipment such as: *Multi-Function Relays*, *AC Analog Input Modules*, and *Control Units for Rail Transport*. The values in the *component selection* section can be adjusted to allow for different level differential input signal, different ADC data throughput rates, and different bandwidth amplifiers.



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Specifications

Specification	OPA827 Calculated	OPA827 Simulated	OPA192 Calculated	OPA192 Simulated
Common Mode Input Range (with Vdif = ±20V)	±26V	±26V	±35V	±35V
Transient ADC Input Settling Error	< 1/2LSB (< 152µV)	0.002 LSB (0.568µV)	< 1/2LSB (< 152µV)	0.006 LSB (1.86µV)
Phase Margin of driver	> 45°	67.1°	> 45°	68.6°
Noise (at ADC Input)	14.128µVrms	15.88µVrms	5.699µVrms	6.44µVrms

Design Notes

1. Determine the amplifier gain based on the differential input signal level, the ADC's configuration for input range. This is covered in the *component selection* section.
2. Determine amplifier's linear range based on common mode voltage, input swing, and power supplies. This is covered in the *component selection* section.
3. In this design circuit, the common-mode voltage of the input signal can be any value in the range of $V_{InputCM}$. The derivation of this range is provided in the *component selection* section for the OPA827 and OPA192.
4. Select COG capacitors to minimize distortion.
5. Use 0.1% 20ppm/°C film resistors or better for good accuracy, low gain drift, and to minimize distortion. Review *Statistics Behind Error Analysis* for methods to minimize gain, offset, drift, and noise errors.
6. Refer to *Introduction to SAR ADC Front-End Component Selection* for an explanation of how to select Rfilt and Cfilt for best settling and AC performance. These component values are dependent on the amplifier bandwidth, data converter sampling rate, and data converter design. The values shown here provide good settling and AC performance for the amplifier and data converter in this example. If the design is modified, select a different RC filter.

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Component Selection

1. Find the gain based on differential input signal and ADC full-scale input range.

$$Gain_{OPA} = \frac{\pm V_{ADC(range)}}{\pm V_{DifIn(range)}} = \frac{\pm 10V}{\pm 20V} = 0.5V / V$$

2. Find standard resistor values for differential gain. Use the *Analog Engineer's Calculator* ("Amplifier and Comparator\Find Amplifier Gain" section) to find standard values for Rf/Rg ratio.

$$Gain_{OPA} = \frac{R_f}{R_g} = \frac{5.05k\Omega}{10.1k\Omega} = 0.5$$

3. Find the amplifier's maximum and minimum input for linear operation (that is, the common mode range of the amplifier, V_{cm_amp}). For this example, the OPA827 is used.

$V_- + 3V < V_{cm\_opa} < V_+ - 3V$ from the OPA827 common mode specification

$-12V < V_{cm\_opa} < 12V \quad for \quad \pm 15V \quad supplies$

4. Calculate the maximum common-mode voltage range based on amplifier's input range and previously shown configuration. Refer to the schematic diagram on the first page for better understanding of how V_{cm_opa}, $V_{InputCM}$, and V_{dif} relate to the circuit.

$$V_{cm\_opa} = \left(V_{InputCM} \pm \frac{V_{dif}}{2}\right) \cdot \left(\frac{R_f}{R_f + R_g}\right)$$

$$V_{cm\_opaMin} \cdot \left(\frac{R_f + R_g}{R_f}\right) + \frac{V_{dif}}{2} < V_{InputCM} < V_{cm\_opaMax} \cdot \left(\frac{R_f + R_g}{R_f}\right) - \frac{V_{dif}}{2}$$

5. Solve the equation for the input common-mode range $V_{InputCM}$ for the amplifier. For this example (OPA827), the common mode input can be ±26V with a ±20-V differential input. Using the same method on OPA192 shows a common mode range of ±35V with a ±20-V differential input. Exceeding this common-mode range will distort the signal. Note that this common-mode range was calculated using ±15-V power supplies. The common mode range could be extended by increasing the supply (maximum ±18V).

$$V_{cm\_opaMin} \cdot \left(\frac{R_f + R_g}{R_f}\right) + \frac{V_{dif}}{2} < V_{InputCM} < V_{cm\_opaMax} \cdot \left(\frac{R_f + R_g}{R_f}\right) - \frac{V_{dif}}{2}$$

$$(-12V) \cdot \left(\frac{5.05k\Omega + 10.1k\Omega}{5.05k\Omega}\right) + \frac{20V}{2} < V_{InputCM} < (12V) \cdot \left(\frac{5.05k\Omega + 10.1k\Omega}{5.05k\Omega}\right) - \frac{20V}{2}$$

$$-26V < V_{InputCM} < 26V$$

6. Find the value for Cf that will achieve the desired closed-loop bandwidth. In this example we want approximately 10-kHz bandwidth. Note: if you adjust the bandwidth you will need to verify the charge bucket filter settling (C_{filt} and R_{filt}) as the closed-loop bandwidth effects settling.

$$C_f = \frac{1}{2 \cdot \pi \cdot R_f \cdot f_c} = \frac{1}{2 \cdot \pi \cdot (5.05k\Omega) \cdot (10kHz)} = 3.1nF \quad or \quad 3nF \quad standard \quad value$$

7. Find the value for Cfilt and Rfilt using *TINA SPICE* and the methods described in *Introduction to SAR ADC Front-End Component Selection*. The value of Rfilt and Cfilt shown in this document will work for these circuits; however, if you use different amplifiers or different gain settings you must use TINA SPICE to find new values.

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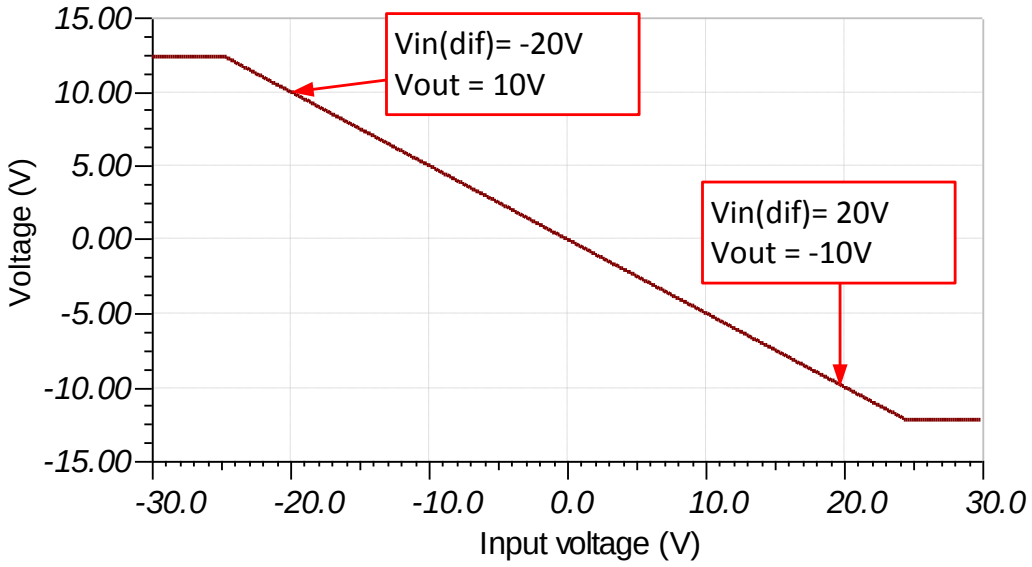
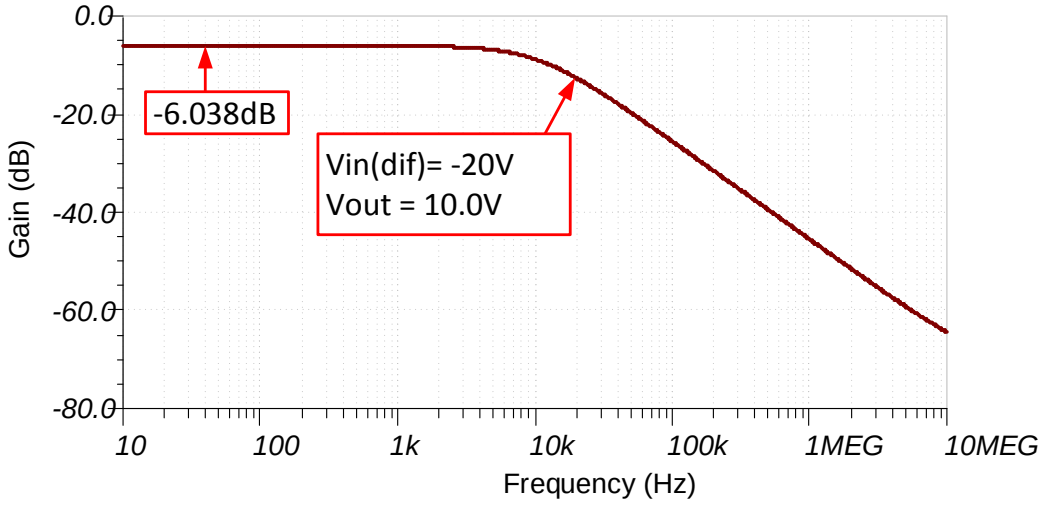
DC Transfer Characteristics

The following graph shows a linear output response for inputs from differential –20V to +20V. The full-scale range (FSR) of the ADC falls within the linear range of the op amp. Refer to *Determining a SAR ADC's Linear Range when using Operational Amplifiers* for detailed theory on this subject.



AC Transfer Characteristics

The bandwidth is simulated to be 10.58kHz and the gain is –6.038dB which is a linear gain of 0.5V/V. See the *Op Amps: Bandwidth 1* video for more details on this subject.



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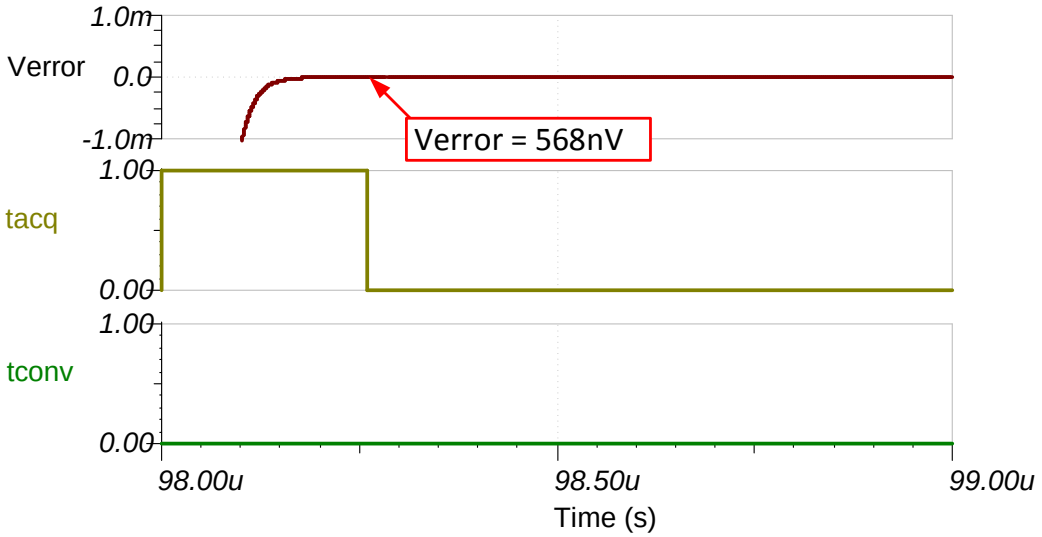
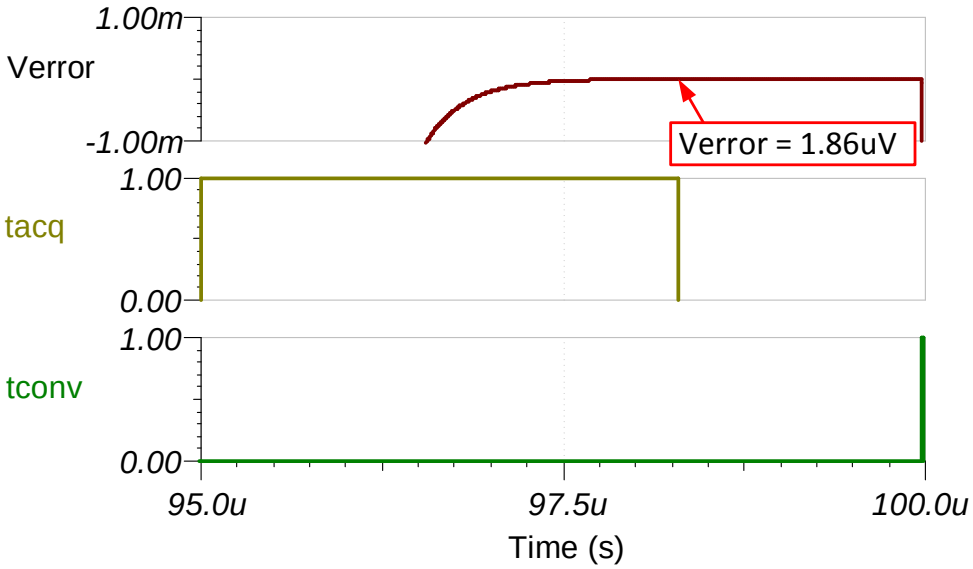
Transient ADC Input Settling Simulation Highest Sampling rate – 510ksps on ADS8568+OPA827

The following simulation shows settling to a 20-V DC input signal with OPA827. This type of simulation shows that the sample and hold kickback circuit is properly selected to within ½ of a LSB (152µV). Refer to *Introduction to SAR ADC Front-End Component Selection* for detailed theory on this subject.



Transient ADC Input Settling Simulation Lower Sampling rate – 200ksps on ADS8568+OPA192

The following simulation shows settling to a 20-V DC input signal with OPA192. This type of simulation shows that the sample and hold kickback circuit is properly selected to within ½ of a LSB (152µV).



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Noise Calculation

This section demonstrates a full-noise analysis including resistor noise. Also, we look at the noise below f_c (Noise Gain = 1.5), and the noise above f_c (noise Gain = 1). In this example, the noise is dominated by wide band amplifier noise so the resistors do not contribute significantly. However, in many cases the resistor noise may be important, so the full noise calculation is provided. Refer to *Calculating the Total Noise for ADC Systems* and *Op Amps: Noise 1* for more detailed theory on this subject.

Bandwidth for feedback loop:

$$f_c = \frac{1}{2 \cdot \pi \cdot R_f \cdot C_f} = \frac{1}{2 \cdot \pi \cdot (5.05k\Omega) \cdot (3nF)} = 10.6kHz$$

Noise from OPA827: 3.8nV/rtHz

$$E_{n\_amp1} = e_{n\_827} \cdot \sqrt{K_n \cdot f_c} = (3.8nV / \sqrt{Hz}) \cdot \sqrt{(1.57) \cdot (10.6kHz)} = 490nVrms$$

Thermal noise density from feedback loop (R_{f1} and R_{g1}) and RC non-inverting input (R_{f2} and R_{g2}):

$$R_{eq} = R_f || R_g = \frac{R_f \cdot R_g}{R_f + R_g} = \frac{(5.05k\Omega) \cdot (10.1k\Omega)}{5.05k\Omega + 10.1k\Omega} = 3.37k\Omega$$

$$e_{n\_feedback} = \sqrt{4 \cdot K_n \cdot T_K \cdot R_{eq}} = \sqrt{4 \cdot \left(1.38 \cdot 10^{-23}\right) \cdot \left(298\right) \cdot \left(3.37k\Omega\right)} = 7.4nV / \sqrt{Hz}$$

$$E_{n\_feedback} = e_{n\_feedback} \cdot \sqrt{K_n \cdot f_c} = (7.4nV / \sqrt{Hz}) \cdot \sqrt{(1.57) \cdot (10.6kHz)} = 0.955\mu Vrms$$

Noise from resistors on the non-inverting input is the same as noise from the feedback resistors.

$$E_{n\_input} = E_{n\_feedback} = 0.955\mu Vrms$$

Total noise (in gain) referred to output of amplifier:

$$E_{n\_below\_fc} = (G_n) \sqrt{{E_{n\_amp1}}^2 + {E_{n\_feedback}}^2 + {E_{n\_input}}^2}$$

$$E_{n\_below\_fc} = (1.5) \sqrt{(0.49\mu V)^2 + (0.995\mu V)^2 + (0.995\mu V)^2} = 2.155\mu Vrms$$

Noise above fc is limited by the output filter (cutoff given below):

$$f_{output} = \frac{1}{2 \cdot \pi \cdot R_{filt} \cdot C_{filt}} = \frac{1}{2 \cdot \pi \cdot (49.9\Omega) \cdot (370pF)} = 8.6MHz$$

$$E_{n\_above\_fc} = e_{n\_827} \cdot \sqrt{K_n \cdot f_{output}} = (2.8nV / \sqrt{Hz}) \cdot \sqrt{(1.57) \cdot (8.6MHz)} = 13.963\mu V$$

Total noise applied to input of the ADC:

$$E_{n\_total} = \sqrt{{E_{n\_below\_fc}}^2 + {E_{n\_above\_fc}}^2} = \sqrt{(2.155\mu V)^2 + (13.963\mu V)^2} = 14.128\mu Vrms$$

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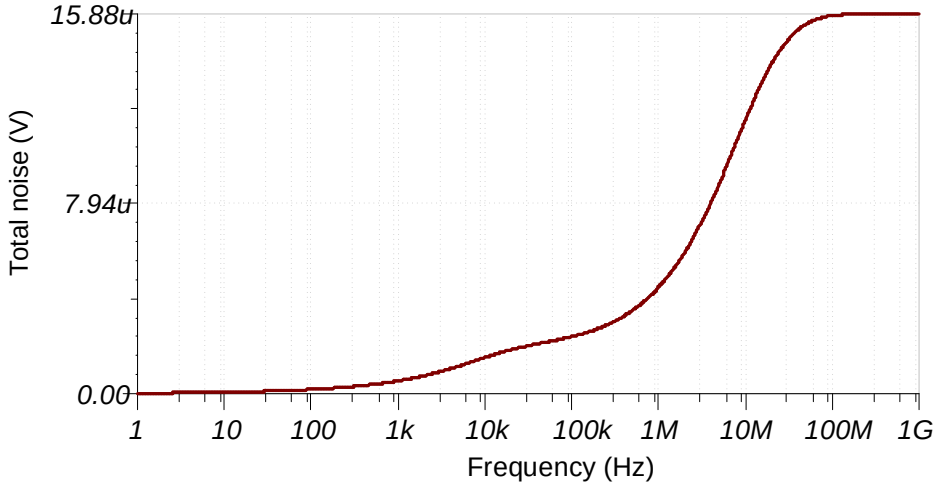
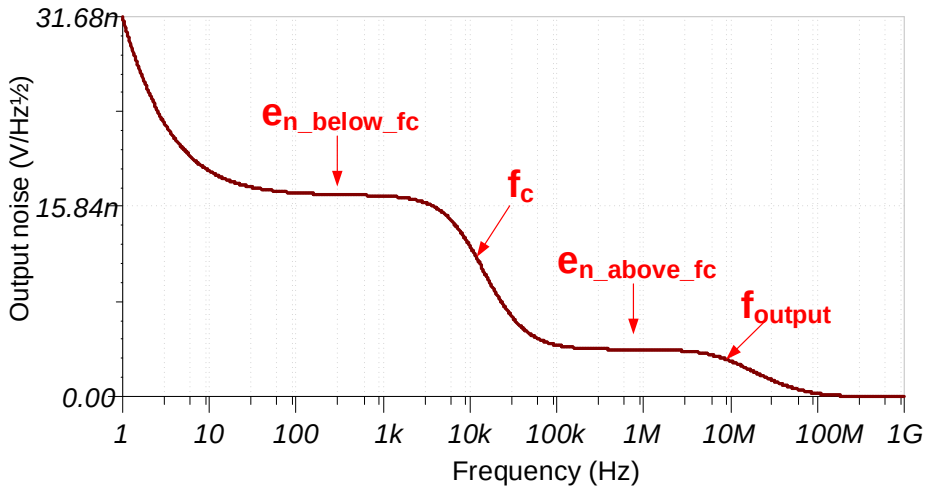
Noise Simulation

The simulated results compare well with the calculated results (that is, simulated = 15.88µVrms, calculated = 14.128µVrms).





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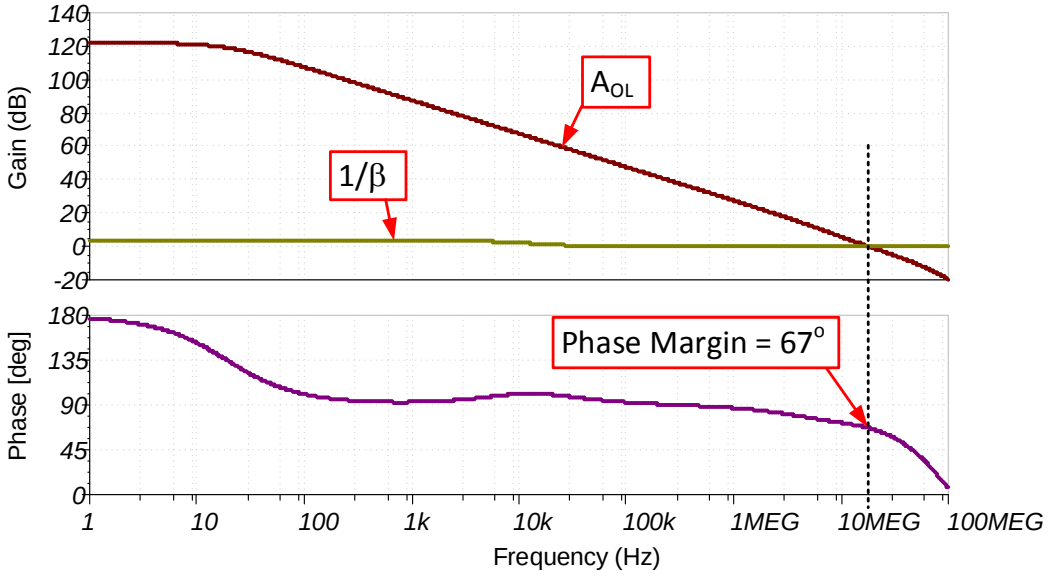
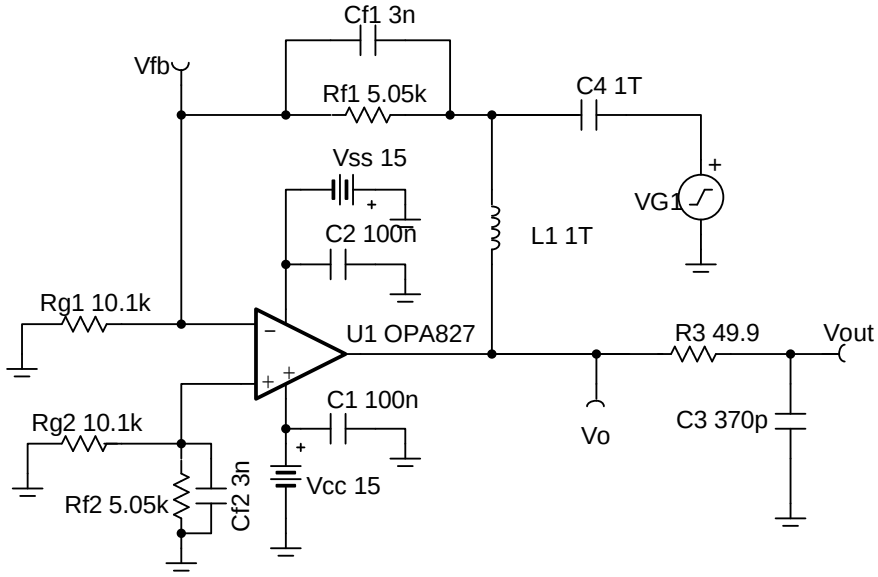
Stability Test

The phase margin for this OPA827 driving circuit is 67.1°, which meets the >45° requirement and is stable. Refer to *Op Amps: Stability 1* for detailed theory explaining stability analysis.





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Design Featured Devices

Device	Key Features	Link	Similar Devices
ADS8568 (1)	16-bit, 8 Channel Simultaneous-Sampling, Bipolar-Input SAR ADC	www.ti.com/product/ADS8568	www.ti.com/adcs
OPA827	Low-Noise, High-Precision, JFET-Input Operational Amplifier	www.ti.com/product/OPA827	www.ti.com/opamp
OPA192	High-Voltage, Rail-to-Rail Input/Output, 5µV, 0.2µV/°C, Precision operational amplifier	www.ti.com/product/OPA192	www.ti.com/opamp

(1) The ADS8568 has integrated a precision voltage reference which can meet most design requirements, but an external REF5050 can be directly connected to the ADS8568 without any additional buffer because the ADS8568 has a built in internal reference buffer for every ADC channel pair. Also, REF5050 has the required low noise and drift for precision SAR applications. C1 is added to balance CMRR (common-mode rejection ratio). Clean analog power supplies are required to achieve best performance specified in the data sheet of the ADC.

Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Link to Key Files (TINA)

Design files for this circuit – http://www.ti.com/lit/zip/sbac180.

Revision History

Revision	Date	Change
A	March 2019	Downstyle the title and changed title role to 'Data Converters'. Added link to circuit cookbook landing page.

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