Low-power sensor measurements: 3.3-V, 1-ksps, 12-bit, single-ended, single-supply circuit

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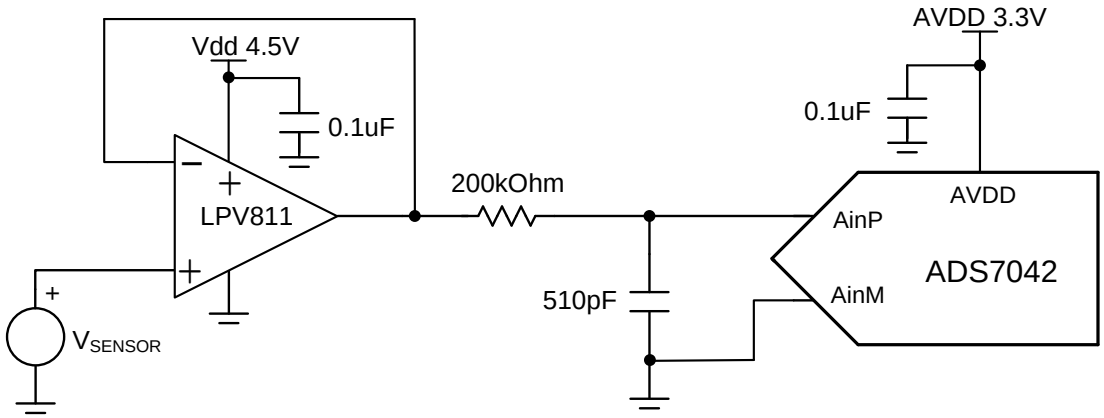
Input	ADC Input	Digital Output ADS7042
VinMin = 0 V	AIN_P = 0V, AIN_M = 0V	000_H or 0_{10}
VinMax = 3.3V	AIN_P = 3.3V, AIN_M = 0V	FFF_H or 4096_{10}

Power Supplies		
AVDD	**Vee**	**Vdd**
3.3V	0V	4.5V

Design Description

This design shows an ultra-low power amplifier being used to drive a SAR ADC that consumes only nanoWatts of power during operation. This design is intended for collecting sensor data by providing overall system-level power consumption on the order of single-digit microWatts. *PIR sensors*, *gas sensors*, and *glucose monitors* are a few examples of possible implementations of this SAR ADC design. The values in the *component selection* section can be adjusted to allow for different data throughput rates and different bandwidth amplifiers. *Low-Power Sensor Measurements: 3.3V, 1ksps, 12-bit Single-Ended, Dual Supply* shows a more sophisticated version of this circuit where the negative supply is connected to a small negative voltage (–0.3V). The single-supply version has degraded performance when the amplifier output is near zero volts. However, in most cases the single-supply configuration is preferred for its simplicity.



Specifications

Specification	Calculated	Simulated	Measured
Transient ADC Input Settling (1ksps)	< 0.5·LSB = 402µV	41.6µV	N/A
AVDD Supply Current (1ksps)	230nA	N/A	214.8nA
AVDD Supply Power (1ksps)	759nW	N/A	709nW
VDD OPAMP Supply Current	450nA	N/A	431.6nA
VDD OPAMP Supply Power	2.025µW	N/A	1.942µW
AVDD + VDD System Power (1ksps)	2.784µW	N/A	2.651µW

Design Notes

1. Determine the linear range of the op amp based on common mode, output swing, and linear open loop gain specification. This is covered in the *component selection* section.
2. Select COG capacitors to minimize distortion.
3. Use 0.1% 20ppm/°C film resistors or better to minimize distortion.
4. The *TI Precision Labs – ADCs* training video series covers methods for selecting the charge bucket circuit Rfilt and Cfilt. These component values are dependent on the amplifier bandwidth, data converter sampling rate, and data converter design. The values shown here will give good settling and AC performance for the amplifier and data converter in this example. If you modify this design you will need to select a different RC filter. Refer to the *Introduction to SAR ADC Front-End Component Selection* training video for an explanation of how to select the RC filter for best settling and AC performance.

Component Selection

1. Select a low-power operational amp:
   - Supply current < 0.5µA
   - Gain bandwidth product > 5kHz (5 times the sampling rate)
   - Unity gain stable
   - For this cookbook, the LPV811 was selected. It has a 450-nA supply current, 8-kHz gain bandwidth product, and is unity gain stable.
2. Find op amp maximum and minimum output for linear operation

   $V_{ee} + 0V < V_{out} < V_{dd} - 0.9V$ from LPV811 Vcm specification

   $V_{ee} + 10mV < V_{out} < V_{dd} - 10mV$ from LPV811 Vout swing specification

   $V_{ee} + 0.3V < V_{out} < V_{dd} - 0.3V$ from LPV811 Aol linear region specification

   $0.3V < V_{in} < 3.4V$ Combined worst case

   NOTE: The linear range of the LPV811 is 300mV above ground. This means to design a system to guarantee a full linear range from 0V to 3.3V (full-scale range (FSR) of ADS7042), then a negative supply is required. This design shows that full-measured SNR and THD specifications of the ADS7042 are met without using a negative supply voltage. This testing was only at room temperature and for a more robust system; *Low-Power Sensor Measurements: 3.3V, 1ksps, 12-bit Single-Ended, Dual Supply* shows this design using a negative supply instead of ground.
3. Typical power calculations (at 1ksps) with expected values:

   $P_{AVDD} = I_{AVDD\_Avg} \cdot AVDD = 230nA \cdot 3.3V = 759nW$

   $P_{LPV811} = I_{LPV811} \cdot (V_{dd} - V_{ee}) = 450nA \cdot (4.5V - 0V) = 2.025\mu W$

   $P_{total} = P_{AVDD} + P_{LPV811} = 759nW + 2.025\mu W = 2.794\mu W$
4. Typical power calculations (at 1ksps) with measured values:

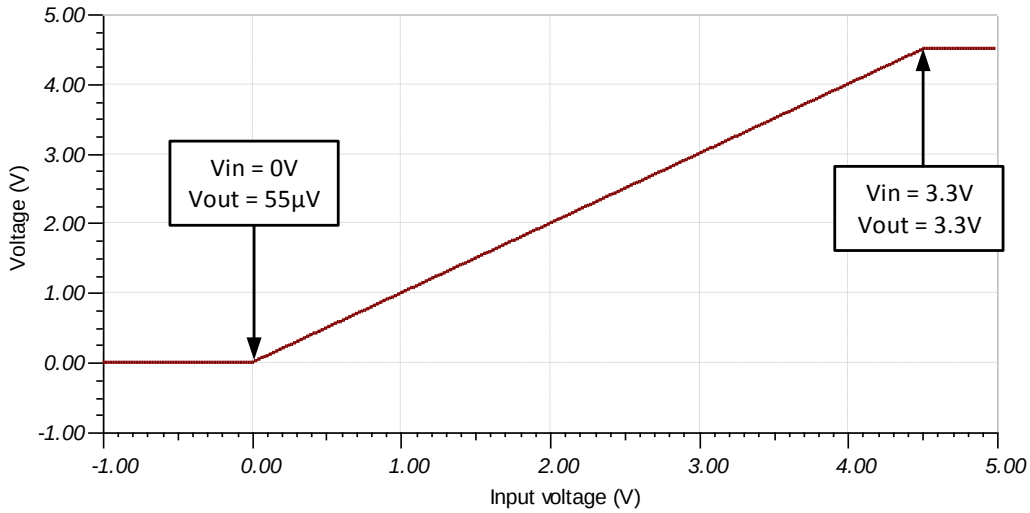
   $P_{AVDD} = I_{AVDD\_Avg} \cdot AVDD = 214nA \cdot 3.3V = 709nW$

   $P_{LPV811} = I_{LPV811} \cdot (V_{dd} - V_{ee}) = 431.6nA \cdot (4.5V - 0V) = 1.942\mu W$

   $P_{total} = P_{AVDD} + P_{LPV811} = 709nW + 1.942\mu W = 2.651\mu W$
5. Find Rfilt and Cfilt to allow for settling at 1ksps. *Refine the Rfilt and Cfilt Values* (a *Precision Labs* video) showing the algorithm for selecting Rfilt and Cfilt. The final value of 200kΩ and 510pF proved to settle to well below ½ of a least significant bit (LSB).

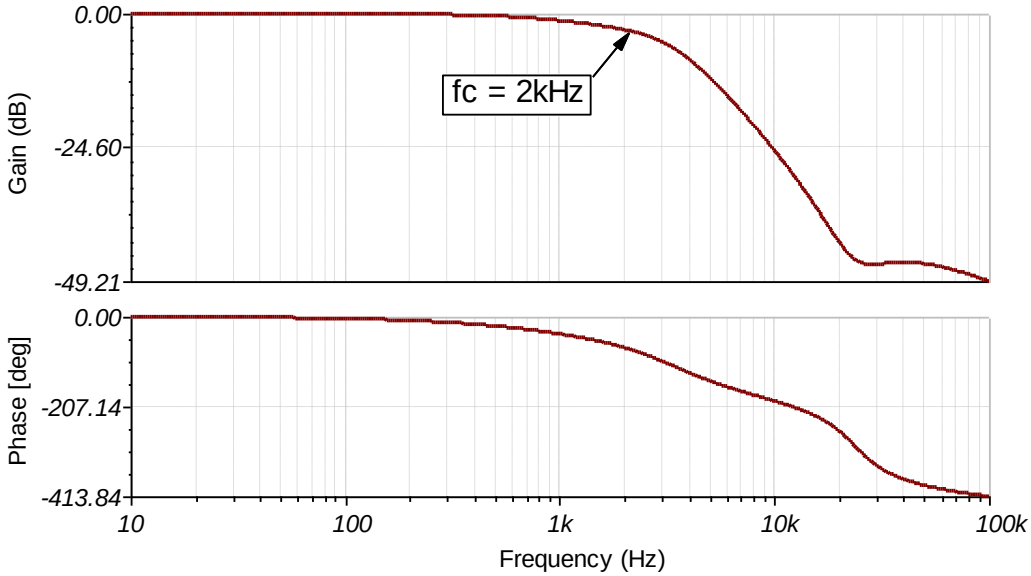
DC Transfer Characteristics

The following graph shows a linear output response for inputs from 0 to 3.3V. The FSR of the ADC falls within the linear range of the op amp.



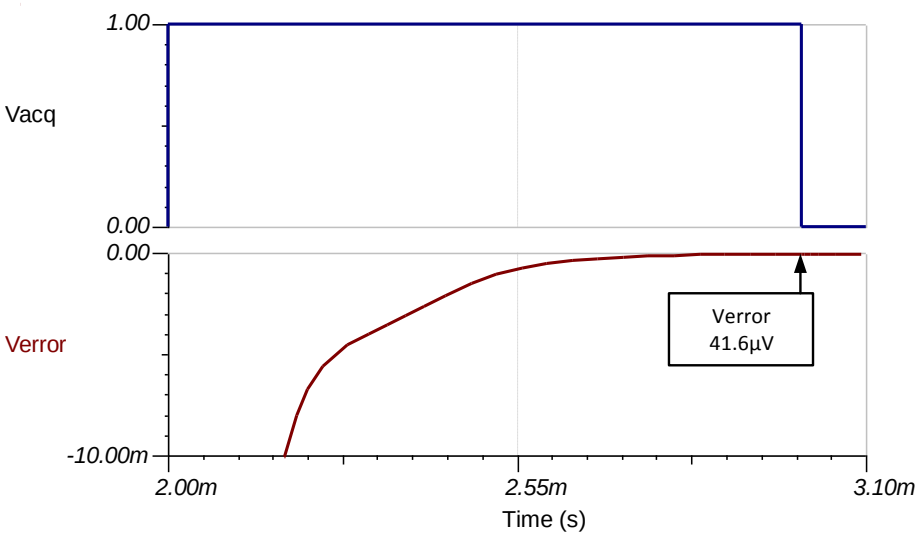
AC Transfer Characteristics

The bandwidth is simulated to be 7.02kHz at the gain of 0dB which is a linear gain of 1. This bandwidth will allow for settling at 1ksps.



Transient ADC Input Settling Simulation

The following simulation shows settling to a 3-V DC input signal. This type of simulation shows that the sample and hold kickback circuit is properly selected to within ½ of a LSB (402µV). Refer to *Introduction to SAR ADC Front-End Component Selection* for detailed theory on this subject.



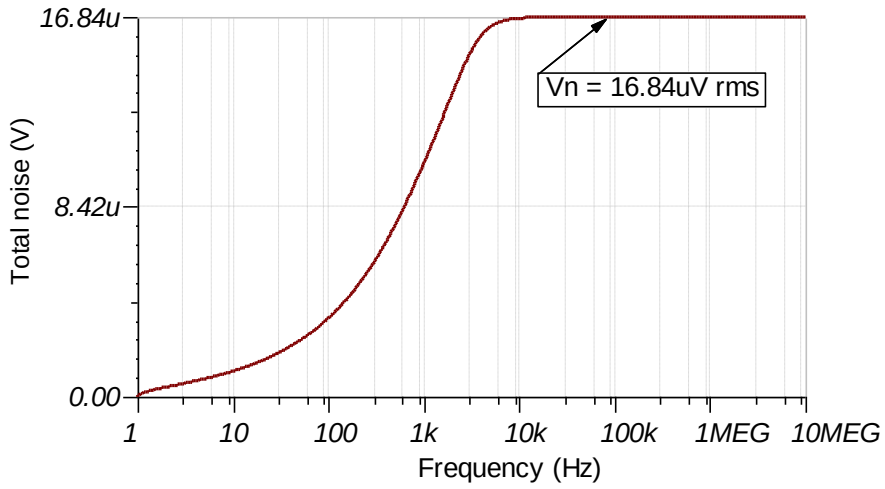
Noise Simulation

This section details a simplified noise calculation for a rough estimate. We neglect resistor noise in this calculation as it is attenuated for frequencies greater than 10kHz.

$$f_c = \frac{1}{2 \cdot \pi \cdot R_{filt} \cdot C_{filt}} = \frac{1}{2 \cdot \pi \cdot (200k\Omega) \cdot (510pF)} = 1560.3Hz$$

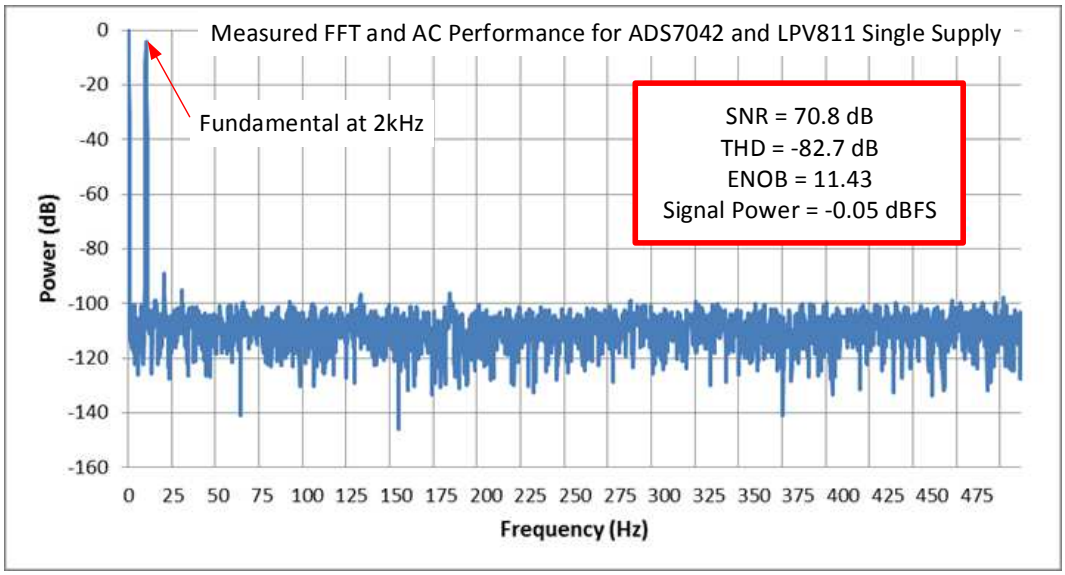
$$E_n = e_{n811} \cdot \sqrt{2 \cdot K_n \cdot f_c} = (340nV / \sqrt{Hz}) \cdot \sqrt{1.57 \cdot (1560Hz)} = 16.8\mu V$$

Note that calculated and simulated match well. Refer to *Calculating the Total Noise for ADC Systems* for detailed theory on this subject.



Measure FFT

This performance was measured on a modified version of the ADS7042EVM-PDK. The AC performance indicates SNR = 70.8dB, THD = –82.7dB, and ENOB (effective number of bits) = 11.43, which matches well with the specified performance of the ADC of SNR = 70dB.



Design Featured Devices

Device	Key Features	Link	Similar Devices
ADS7042 (1)	12-bit resolution, SPI, 1-Msps sample rate, single-ended input, AVDD, Vref input range 1.6 V to 3.6 V.	www.ti.com/product/ADS7042	www.ti.com/adcs
LPV811 (2)	8 kHz bandwidth, Rail-to-Rail output, 450 nA supply current, unity gain stable	www.ti.com/product/LPV811	www.ti.com/opamp

(1) The ADS7042 uses the AVDD as the reference input. A high-PSRR LDO, such as the TPS7A47, should be used as the power supply.
(2) The LPV811 is also commonly used in low speed applications for sensors. Furthermore, the rail-to-rail output allows for linear swing across all of the ADC input range.

Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Link to Key Files

Tina files for low-power sensor measurements - http://www.ti.com/lit/zip/sbam341.

Revision History

Revision	Date	Change
A	March 2019	Downstyle the title and changed title role to 'Data Converters'. Added link to circuit cookbook landing page.

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