Low-power sensor measurements: 3.3-V, 1-kmps, 12-bit, single-ended, single-supply circuit

Reed Kaczmarek

<table>
<thead>
<tr>
<th>Input</th>
<th>ADC Input</th>
<th>Digital Output ADS7042</th>
</tr>
</thead>
<tbody>
<tr>
<td>VinMin = 0 V</td>
<td>AIN_P = 0V, AIN_M = 0V</td>
<td>000b or 010</td>
</tr>
<tr>
<td>VinMax = 3.3V</td>
<td>AIN_P = 3.3V, AIN_M = 0V</td>
<td>FFFb or 4096b</td>
</tr>
</tbody>
</table>

Power Supplies

<table>
<thead>
<tr>
<th>AVDD</th>
<th>Vee</th>
<th>Vdd</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3V</td>
<td>0V</td>
<td>4.5V</td>
</tr>
</tbody>
</table>

Design Description

This design shows an ultra-low power amplifier being used to drive a SAR ADC that consumes only nanoWatts of power during operation. This design is intended for collecting sensor data by providing overall system-level power consumption on the order of single-digit microWatts. PIR sensors, gas sensors, and glucose monitors are a few examples of possible implementations of this SAR ADC design. The values in the component selection section can be adjusted to allow for different data throughput rates and different bandwidth amplifiers. Low-Power Sensor Measurements: 3.3V, 1kmps, 12-bit Single-Ended, Dual Supply shows a more sophisticated version of this circuit where the negative supply is connected to a small negative voltage (–0.3V). The single-supply version has degraded performance when the amplifier output is near zero volts. However, in most cases the single-supply configuration is preferred for its simplicity.
Specifications

<table>
<thead>
<tr>
<th>Specification</th>
<th>Calculated</th>
<th>Simulated</th>
<th>Measured</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transient ADC Input Settling (1ksps)</td>
<td>&lt; 0.5·LSB = 402µV</td>
<td>41.6µV</td>
<td>N/A</td>
</tr>
<tr>
<td>AVDD Supply Current (1ksps)</td>
<td>230nA</td>
<td>N/A</td>
<td>214.8nA</td>
</tr>
<tr>
<td>AVDD Supply Power (1ksps)</td>
<td>759nW</td>
<td>N/A</td>
<td>709nW</td>
</tr>
<tr>
<td>VDD OPAMP Supply Current</td>
<td>450nA</td>
<td>N/A</td>
<td>431.6nA</td>
</tr>
<tr>
<td>VDD OPAMP Supply Power</td>
<td>2.025µW</td>
<td>N/A</td>
<td>1.942µW</td>
</tr>
<tr>
<td>AVDD + VDD System Power (1ksps)</td>
<td>2.784µW</td>
<td>N/A</td>
<td>2.651µW</td>
</tr>
</tbody>
</table>

Design Notes

1. Determine the linear range of the op amp based on common mode, output swing, and linear open loop gain specification. This is covered in the component selection section.
2. Select COG capacitors to minimize distortion.
3. Use 0.1% 20ppm/°C film resistors or better to minimize distortion.
4. The TI Precision Labs – ADCs training video series covers methods for selecting the charge bucket circuit Rfilt and Cfilt. These component values are dependent on the amplifier bandwidth, data converter sampling rate, and data converter design. The values shown here will give good settling and AC performance for the amplifier and data converter in this example. If you modify this design you will need to select a different RC filter. Refer to the Introduction to SAR ADC Front-End Component Selection training video for an explanation of how to select the RC filter for best settling and AC performance.
Component Selection

1. Select a low-power operational amp:
   - Supply current < 0.5µA
   - Gain bandwidth product > 5kHz (5 times the sampling rate)
   - Unity gain stable
   - For this cookbook, the LPV811 was selected. It has a 450-nA supply current, 8-kHz gain bandwidth product, and is unity gain stable.

2. Find op amp maximum and minimum output for linear operation
   \[ V_{ee} + 0V < V_{out} < V_{dd} - 0.9V \text{ from LPV811 Vcm specification} \]
   \[ V_{ee} + 10mV < V_{out} < V_{dd} - 10mV \text{ from LPV811 Vout swing specification} \]
   \[ V_{ee} + 0.3V < V_{out} < V_{dd} - 0.3V \text{ from LPV811 Aol linear region specification} \]
   \[ 0.3V < V_{in} < 3.4V \text{ Combined worst case} \]

   **NOTE:** The linear range of the LPV811 is 300mV above ground. This means to design a system to guarantee a full linear range from 0V to 3.3V (full-scale range (FSR) of ADS7042), then a negative supply is required. This design shows that full-measured SNR and THD specifications of the ADS7042 are met without using a negative supply voltage. This testing was only at room temperature and for a more robust system; Low-Power Sensor Measurements: 3.3V, 1ksps, 12-bit Single-Ended, Dual Supply shows this design using a negative supply instead of ground.

3. Typical power calculations (at 1ksps) with expected values:
   \[ P_{AVDD} = I_{AVDD,\text{avg}} \cdot AVDD = 230nA \cdot 3.3V = 759nW \]
   \[ P_{LPV811} = I_{LPV811} \cdot (V_{dd} - V_{ee}) = 450nA \cdot (4.5V - 0V) = 2.025\mu W \]
   \[ P_{total} = P_{AVDD} + P_{LPV811} = 759nW + 2.025\mu W = 2.794\mu W \]

4. Typical power calculations (at 1ksps) with measured values:
   \[ P_{AVDD} = I_{AVDD,\text{avg}} \cdot AVDD = 214nA \cdot 3.3V = 709nW \]
   \[ P_{LPV811} = I_{LPV811} \cdot (V_{dd} - V_{ee}) = 431.6nA \cdot (4.5V - 0V) = 1.942\mu W \]
   \[ P_{total} = P_{AVDD} + P_{LPV811} = 709nW + 1.942\mu W = 2.651\mu W \]

5. Find Rfilt and Cfilt to allow for settling at 1ksps. **Refine the Rfilt and Cfilt Values** (a Precision Labs video) showing the algorithm for selecting Rfilt and Cfilt. The final value of 200kΩ and 510pF proved to settle to well below ½ of a least significant bit (LSB).
DC Transfer Characteristics

The following graph shows a linear output response for inputs from 0 to 3.3V. The FSR of the ADC falls within the linear range of the op amp.

![DC Transfer Characteristics Graph]

AC Transfer Characteristics

The bandwidth is simulated to be 7.02kHz at the gain of 0dB which is a linear gain of 1. This bandwidth will allow for settling at 1ksps.
Transient ADC Input Settling Simulation

The following simulation shows settling to a 3-V DC input signal. This type of simulation shows that the sample and hold kickback circuit is properly selected to within ½ of a LSB (402µV). Refer to Introduction to SAR ADC Front-End Component Selection for detailed theory on this subject.

Noise Simulation

This section details a simplified noise calculation for a rough estimate. We neglect resistor noise in this calculation as it is attenuated for frequencies greater than 10kHz.

\[ f_c = \frac{1}{2 \pi R R_s C} = \frac{1}{2 \pi \cdot (200\Omega) \cdot (510pF)} = 1560.3Hz \]

\[ E_n = e_{n811} \cdot \sqrt{2 \cdot K \cdot f_c} = (340nV / \sqrt{Hz}) \cdot \sqrt{1.57 \cdot (1560Hz)} = 16.8\mu V \]

Note that calculated and simulated match well. Refer to Calculating the Total Noise for ADC Systems for detailed theory on this subject.
Measure FFT

This performance was measured on a modified version of the ADS7042EVM-PDK. The AC performance indicates SNR = 70.8 dB, THD = -82.7 dB, and ENOB (effective number of bits) = 11.43, which matches well with the specified performance of the ADC of SNR = 70 dB.

![Measured FFT and AC Performance for ADS7042 and LPV811 Single Supply](image)

- SNR = 70.8 dB
- THD = -82.7 dB
- ENOB = 11.43
- Signal Power = -0.05 dBFS
Design Featured Devices

<table>
<thead>
<tr>
<th>Device</th>
<th>Key Features</th>
<th>Link</th>
<th>Similar Devices</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADS7042</td>
<td>12-bit resolution, SPI, 1-Msps sample rate, single-ended input, AVDD. Vref input range 1.6 V to 3.6 V.</td>
<td><a href="http://www.ti.com/product/ADS7042">www.ti.com/product/ADS7042</a></td>
<td><a href="http://www.ti.com/adcs">www.ti.com/adcs</a></td>
</tr>
<tr>
<td>LPV811</td>
<td>8 kHz bandwidth, Rail-to-Rail output, 450 nA supply current, unity gain stable</td>
<td><a href="http://www.ti.com/product/LPV811">www.ti.com/product/LPV811</a></td>
<td><a href="http://www.ti.com/opamp">www.ti.com/opamp</a></td>
</tr>
</tbody>
</table>

(1) The ADS7042 uses the AVDD as the reference input. A high-PSRR LDO, such as the TPS7A47, should be used as the power supply.
(2) The LPV811 is also commonly used in low speed applications for sensors. Furthermore, the rail-to-rail output allows for linear swing across all of the ADC input range.

Design References

See Analog Engineer's Circuit Cookbooks for TI's comprehensive circuit library.

Link to Key Files


Revision History

<table>
<thead>
<tr>
<th>Revision</th>
<th>Date</th>
<th>Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>March 2019</td>
<td>Downstyle the title and changed title role to 'Data Converters'. Added link to circuit cookbook landing page.</td>
</tr>
</tbody>
</table>
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