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Driving a SAR ADC directly without a front-end buffer circuit (low-power, low-sampling-speed DAQ)

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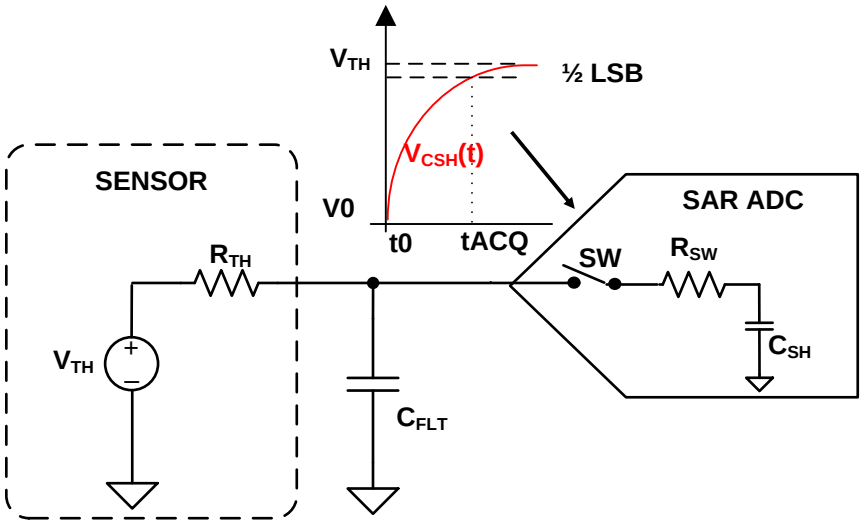
Design Description

This design explains how sensor outputs can be directly interfaced with a SAR ADC input. In applications such as *Environmental Sensors*, *Gas Detectors*, and *Smoke or Fire Detectors*, the input is very slow-moving and the sensor output voltage is sampled at fairly slower speeds (10ksps or so). In such or similar systems, the sensor output can be directly interfaced with the SAR ADC input without the need for a driver amplifier to achieve a small form-factor, low-cost design.

Interfacing Sensor Output Directly to a SAR ADC

The following figure shows a typical application diagram for interfacing a sensor directly to a SAR ADC input without the use of a driver amplifier. The sensor block highlights the Thevenin equivalent of a sensor output. Voltage source, V_{TH}, is the Thevenin-equivalent voltage and source resistance R_{TH} is the Thevenin-equivalent impedance. Most sensor data sheets provide the Thevenin model of the sensor from which the value of the series impedance can be easily calculated.



Specifications

Parameter	Calculated	Simulated	Measured
Transient ADC Input Settling Error	< 0.5LSB < 100.5µV	36.24µV	N/A
Step Input Full Scale Range	3.15V	3.15V	3.14978
Input Source Impedance (R_{TH})	10kΩ	10kΩ	10.01kΩ
Filter Capacitor Value (C_{FLT})	680pF	680pF	N/A
ADC Sampling Speed	10ksps	10ksps	10ksps

Design Note

1. Determine source impedance of input signal. Calculate the RC time constant of the input source impedance and filter capacitor (known value).
2. Determine the minimum acquisition time required for the input signal to settle for a given source impedance and the filter capacitor combination.
3. Select COG capacitors to minimize distortion.
4. Use 0.1% 20ppm/°C film resistors or better for good gain drift and to minimize distortion.

Component Selection for ADC Input Settling

SAR ADCs can be directly interfaced with sensors when the analog input source is capable of driving the switched capacitor load of a SAR ADC and settling the analog input signal to within ½ of an LSB within the acquisition time of the SAR ADC. To achieve this, the external RC filter (R_{TH} and C_{FLT}) must settle within the acquisition time (t_{ACQ}) of the ADC. The relationship between the ADC acquisition time and RC time constant of the external filter is:

$$t_{ACQ} \geq k \cdot \tau_{FLT}$$

where

- $\tau_{FLT} = R_{TH} \cdot C_{FLT}$
- k is the single pole time constant for N bit ADC

The following design example values are given in the table on page 1:

$R_{TH} = 10k\Omega$

$C_{FLT} = 680pF$

K = 11 (Single pole time constant multiplier for 14-bit ADC) – More information is found on page 96 and page 97 of the *Analog Engineer's Pocket Reference*.

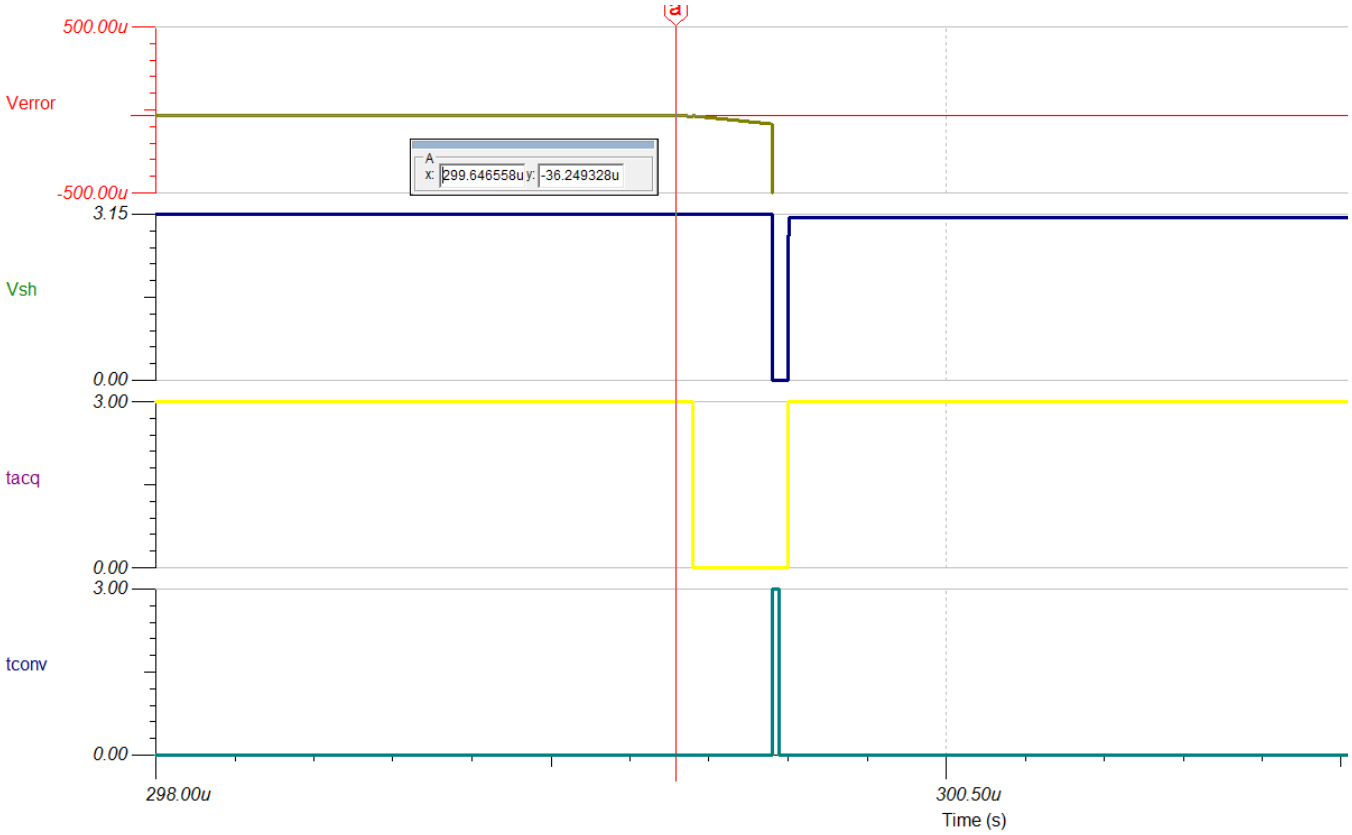
Minimum acquisition time required for proper settling is calculated using this equation:

$$t_{ACQ} \geq 11 \cdot 10k\Omega \cdot 680pF = 74.80\mu s$$

For more information on SAR ADCs and front end design for SAR ADCs, refer to *Introduction to SAR ADC Front-End Component Selection*.

Transient Input Settling Simulation using TI-TINA

The following figure shows the settling of an *ADS7056* ADC given a 3.15-V DC input signal. This type of simulation shows that the sample and hold kickback circuit is properly selected. Refer to *Refine the Rfilt and Cfilt Values* in the *TI Precision Labs - ADCs* training video series for detailed theory on this subject.



Increasing Acquisition Time of SAR ADC for Input Signal Settling

The acquisition time of a SAR ADC can be increased by reducing the throughput in the following ways:

1. Reducing the SCLK frequency to reduce the throughput.
2. Keeping the SCLK fixed at the highest permissible value and increasing the CS high time.

The following table lists the acquisition time for the previous two cases for the *ADS7056* SAR ADC operating at 10ksps throughput (tcycle = 100µs). Case 2 provides a longer acquisition time for the input signal to settle because of the increased frequency of the SCLK given a fixed conversion and cycle time.

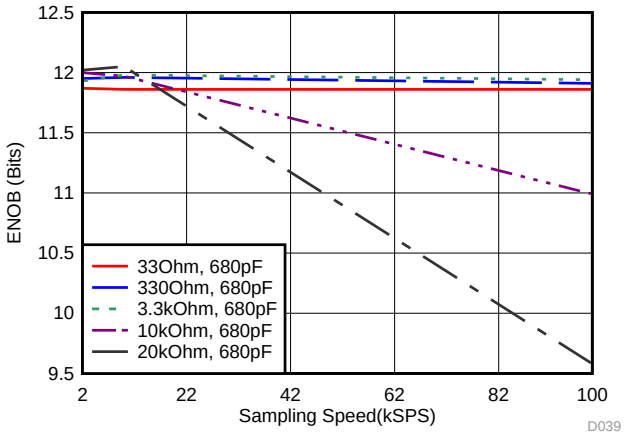
Case	SCLK	t_{cycle}	Conversion Time ($18 \cdot t_{SCLK}$)	Acquisition Time ($t_{cycle} - t_{conv}$)
1	0.24MHz	100µs	74.988µs	25.01µs
2	60MHz	100µs	0.3µs	99.70µs

The following table shows a performance comparison between an 8-, 10-, 12-, and 14-bit ADC with respect to sampling speed and effective number of bits (ENOB) when a sensor output with an output impedance of 10kΩ is directly interfaced with the ADC input. As expected, the ENOB degrades with higher sampling rates because the acquisition time decreases.

Sampling Speed (ksps)	ADS7040 (8-bit ADC) ENOB (R_{TH} = 10kΩ, C_{FLT} = 1.5nF)	ADS7041 (10-bit ADC) ENOB (R_{TH} = 10kΩ, C_{FLT} = 1.5nF)	ADS7042 (12-bit ADC) ENOB (R_{TH} = 10kΩ, C_{FLT} = 1.5nF)	ADS7056 (14-bit ADC) ENOB (R_{TH} = 10kΩ, C_{FLT} = 680pF)
10	7.93	9.87	10	12.05
100	7.92	9.85	9.97	10.99
500	7.88	9.68	9.95	8.00

Performance Achieved at Different Throughput Rates with Different Source impedance

The following figure provides the ENOB achieved from the ADS7056 at different throughout with different input impedances. Note that all the results for the following graph were taken with a 100-Hz analog input signal and without an ADC driver amplifier.



Design Featured Devices:

Device	Key Features	Link	Similar Devices
ADS7040	8-bit resolution, SPI, 1-Msps sample rate, single-ended input, AVDD/Vref input range 1.6V to 3.6V.	www.ti.com/product/ADS7040	www.ti.com/adcs
ADS7041	10-bit resolution, SPI, 1Msps sample rate, single-ended input, AVDD/Vref input range 1.6V to 3.6V.	www.ti.com/product/ADS7041	www.ti.com/adcs
ADS7042	12-bit resolution, SPI, 1-Msps sample rate, single-ended input, AVDD/Vref input range 1.6V to 3.6V.	www.ti.com/product/ADS7042	www.ti.com/adcs
ADS7056	14-bit resolution, SPI, 2.5-Msps sample rate, single-ended input, AVDD/Vref input range 1.6V to 3.6V.	www.ti.com/product/ADS7056	www.ti.com/adcs

NOTE: The ADS7042 and ADS7056 use the AVDD as the reference input. A high-PSRR LDO, such as the TPS7A47, should be used as the power supply.

Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Link to Key file

Source files for interfacing sensor output directly with SAR ADCs – http://www.ti.com/lit/zip/sbac178.

Revision History

Revision	Date	Change
A	March 2019	Downstyle the title and changed title role to 'Data Converters. Added link to circuit cookbook landing page.

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