Application Note

A Basic Guide to RTD Measurements

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ABSTRACT

RTDs, or resistance temperature detectors, are sensors used to measure temperature. These sensors are the among the most accurate temperature sensors available, covering large temperature ranges. However, getting accurate measurements with precision analog-to-digital converters (ADCs) requires attention to detail in design of measurement circuits and calculation of the measurement. This application note starts with an overview of the RTD, discussing their specifications, construction, and details in their use in temperature measurement. Different circuit topologies with precision ADCs are presented for different RTD configurations. Each circuit is shown with a basic design guide, showing calculations necessary to determine the ADC settings, limit measurement errors, and verify that the design fits in the operating range of the ADC.

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1 RTD Overview

RTDs are resistive elements that change resistance over temperature. Because the change in resistance is well characterized, they are used to make precision temperature measurements, with capability of making measurements with accuracies of well under 0.1°C. RTDs are typically constructed from a length of wire wrapped around a ceramic or glass core. RTDs may also be constructed from thick film resistors plated onto a substrate. The wire or resistance is typically platinum but may also be made from nickel or copper. The PT100 is a common RTD constructed from platinum with a resistance of 100 Ω at 0°C. RTD elements are also available with 0°C resistances of 200, 500, 1000, and 2000 Ω.

1.1 Callendar-Van Dusen Equation

The relationship between platinum RTD resistance and temperature is described by the Callendar-Van Dusen (CVD) equation. Equation 1 shows the resistance for temperatures below 0°C and Equation 2 shows the resistance for temperatures above 0°C for a PT100 RTD.

$$\text{For } T < 0: R_{RTD}(T) = R_0 \bullet \{1 + (A \bullet T) + (B \bullet T^2) + [(C \bullet T^3) \bullet (T - 100)]\} \quad (1)$$

$$\text{For } T > 0: R_{RTD}(T) = R_0 \bullet [1 + (A \bullet T) + (B \bullet T^2)] \quad (2)$$

The coefficients in the Callendar-Van Dusen equations are defined by the IEC-60751 standard. R_0 is the resistance of the RTD at 0°C. For a PT100 RTD, R_0 is 100 Ω. For IEC 60751 standard PT100 RTDs, the coefficients are:

- $A = 3.9083 \bullet 10^{-3}$
- $B = –5.775 \bullet 10^{-7}$
- $C = –4.183 \bullet 10^{-12}$

The change in resistance of a PT100 RTD from –200°C to 850°C is displayed in Figure 1-1.

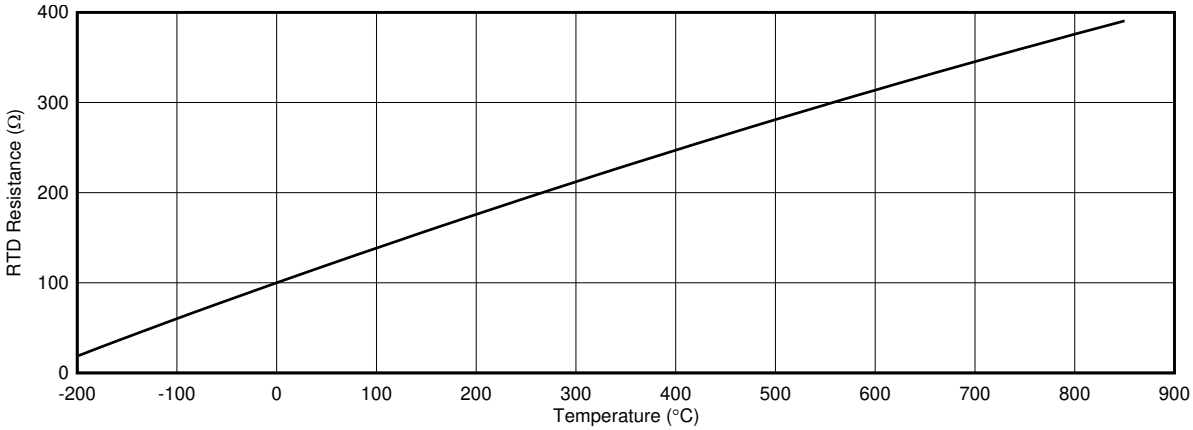

Figure 1-1. PT100 RTD Resistance From –200°C to 850°C

While the change in RTD resistance is fairly linear over small temperature ranges, Figure 1-2 displays the resulting non-linearity if an end-point fit is made to the curve shown in Figure 1-1.

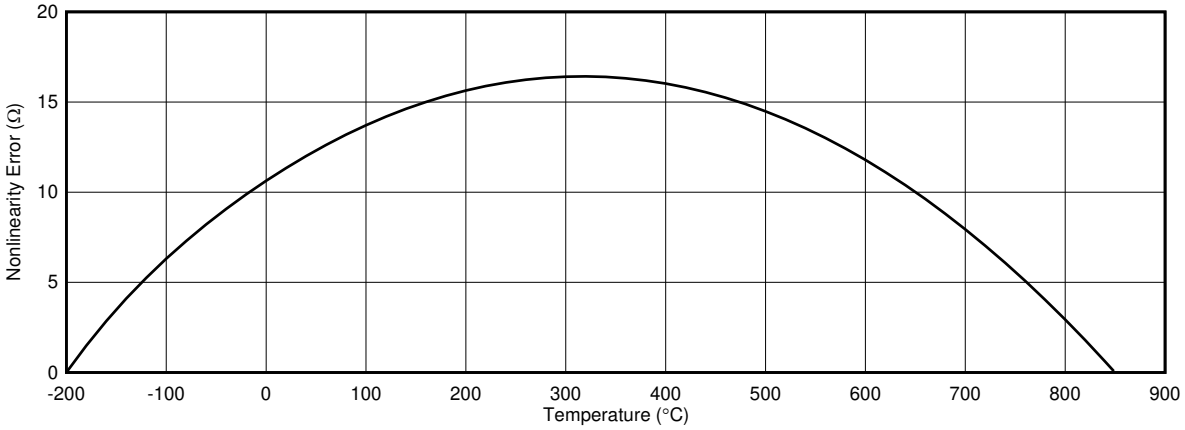

Figure 1-2. PT100 RTD Non-Linearity From –200°C to 850°C

The results show a non-linearity greater than 16 Ω, making a linear approximation difficult over even small ranges. For temperatures greater than 0°C, temperatures can be determined by solving the quadratic from Equation 2. For temperatures lower than 0°C, the third order polynomial of Equation 1 may be difficult to calculate. Using simple microcontrollers, determining the temperature may be computationally difficult and using a look-up table to determine the temperature is common practice.

Newer calibration standards allow for more calculation accuracy using higher order polynomials over segmented temperature ranges, but the Callendar-Van Dusen equation remains a commonly used conversion standard.

1.2 RTD Tolerance Standards

RTDs have good interchangeability. This means that there is little variation from sensor to sensor because of good accuracy tolerance. This allows for good measurement accuracy, even if RTD sensors are replaced from system to system.

There are two tolerance standards that define a grade or class for platinum RTD accuracy. The American standard is ASTM E1137 and is used mostly in North America. The European standard is known as the DIN or IEC standard. DIN IEC 60751 is used world wide. Both standards define the accuracy of the RTD starting with a base resistance of 100 Ω at a temperature of 0°C.

Table 1-1 shows the specifications of different classes of RTDs. In both standards, the RTD has the tightest tolerance at 0°C. An absolute error is combined with a proportional error that has a temperature coefficient.

Table 1-1. RTD Tolerance Class Information

TOLERANCE	TOLERANCE VALUES (°C)	RESISTANCE AT 0°C (Ω)	ERROR AT 100°C (°C)
ASTM Grade B	± (0.25 + 0.0042 • |T|)	100 ± 0.1	± 0.67
ASTM Grade A	± (0.13 + 0.0017 • |T|)	100 ± 0.05	± 0.3
IEC Class C	± (0.6 + 0.01 • |T|)	100 ± 0.24	± 1.6
IEC Class B	± (0.3 + 0.005 • |T|)	100 ± 0.12	± 0.8
IEC Class A	± (0.15 + 0.002 • |T|)	100 ± 0.06	± 0.35
IEC Class AA	± (0.1 + 0.0017 • |T|)	100 ± 0.04	± 0.27
1/10 DIN(1)	± (0.03 + 0.0005 • |T|)	100 ± 0.012	± 0.08

(1) 1/10 DIN is not included in the IEC 60751 specification but is an industry accepted tolerance for performance demanding applications. It is 1/10th of the DIN IEC Class B specification.

The specified temperature range of each RTD class tolerance becomes smaller with more accurate grades and classes. Additionally, the range varies with the RTD construction type. For more details about tolerance values and temperature ranges, consult the data sheets of the RTD manufacturer.

1.3 RTD Wiring Configurations

RTDs are made in three different wiring configurations described in this application note. Each wiring configuration requires a different excitation and circuit topology to reduce the measurement error. The three different wiring configurations are shown in Figure 1-3.

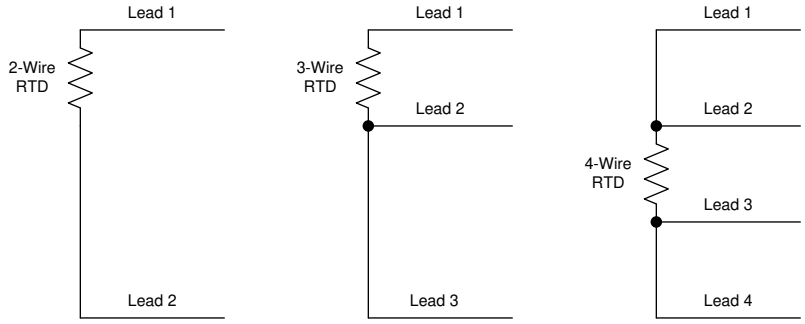

Figure 1-3. Two-Wire, Three-Wire, and Four-Wire RTDs

In the two-wire configuration, the RTD is connected through two wires connected to either end of the RTD. In this configuration, the lead wire resistances cannot be separated from the RTD resistance, adding an error that cannot be separated from the RTD measurement. Two-wire RTDs yield the least accurate RTD measurements and are used when accuracy is not critical or when lead lengths are short. Two-wire RTDs are the least expensive RTD configuration.

In the three-wire configuration, the RTD is connected to a single lead wire on one end and two lead wires on the opposite end. Using different circuit topologies and measurements, lead resistance effects can effectively be cancelled, reducing the error in three-wire RTD measurements. Compensation for lead wire resistance assumes that the lead resistances match.

In the four-wire configuration, two lead wires are connected to either end of the RTD. In this configuration, the RTD resistance may be measured with a four-wire resistive measurement with superior accuracy. The RTD excitation is driven through one lead on either end, while the RTD resistance is measured with the other lead on either end. In this measurement, the RTD resistance is sensed without error contributed from the lead wire reacting with the sensor excitation. Four-wire RTDs yield the most accurate measurements, but are the most expensive RTD configuration.

1.4 Ratiometric Measurements

RTD measurements with an ADC are typically made with a ratiometric measurements. Figure 1-4 shows the basic topology of a ratiometric measurement. Shown are the ADC with a two-wire RTD and a reference resistor R_{REF}. A single excitation current source (IDAC1) is used to excite the RTD as well as to establish a reference voltage across R_{REF} for the ADC.

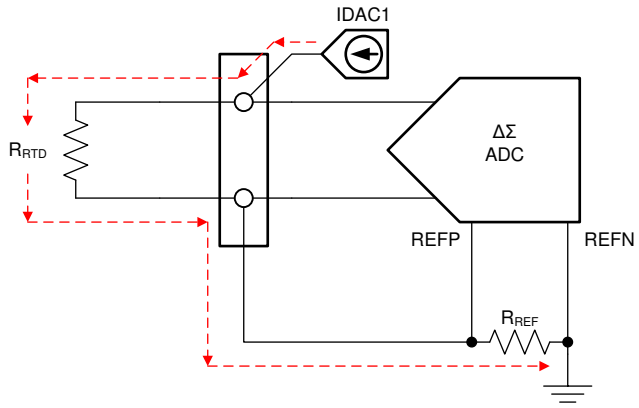

Figure 1-4. Example of a Ratiometric RTD Measurement

With IDAC1, the ADC measures the voltage across the RTD using the voltage across R_{REF} as the reference. This provides an output code that is proportional to the ratio of the RTD voltage and the reference voltage as shown in Equation 3. Ratiometric measurements will only produce positive output data, assuming zero offset error. For a fully-differential measurement, this is only the positive half of the full-scale range of the ADC, reducing the measurement resolution by one bit. The following equations assume a 24-bit bipolar ADC, with $\pm V_{REF}$ as the full-scale range of the ADC.

$$\text{Output code} = 2^{23} \cdot V_{RTD} / V_{REF} = 2^{23} \cdot I_{IDAC1} \cdot R_{RTD} / (I_{IDAC1} \cdot R_{REF}) \quad (3)$$

The currents cancel so that the equation reduces to Equation 4:

$$\text{Output code} = 2^{23} \cdot R_{RTD} / R_{REF} \quad (4)$$

In the end, the RTD resistance can be represented from the code as a function of the reference resistance.

$$R_{RTD} = \text{Output code} \cdot R_{REF} / 2^{23} \quad (5)$$

The measurement depends on the resistive value of the RTD and the reference resistor R_{REF}, but not on the IDAC1 current value. Therefore, the absolute accuracy and temperature drift of the excitation current does not matter. In a ratiometric measurement, as long as there is no current leakage from IDAC1 outside of this circuit, the measurement depends only on R_{RTD} and R_{REF}. ADC conversions do not need to be translated to voltage.

Assuming the ADC has a low gain error, R_{REF} is often the largest source of error. The reference resistor must be a high accuracy precision resistor with low drift. Any error in the reference resistance becomes a gain error in the measurement.

1.4.1 Lead Resistance Cancellation

In Figure 1-5, the lead resistances of a three-wire RTD are shown and a second excitation current source is added, labeled IDAC2.

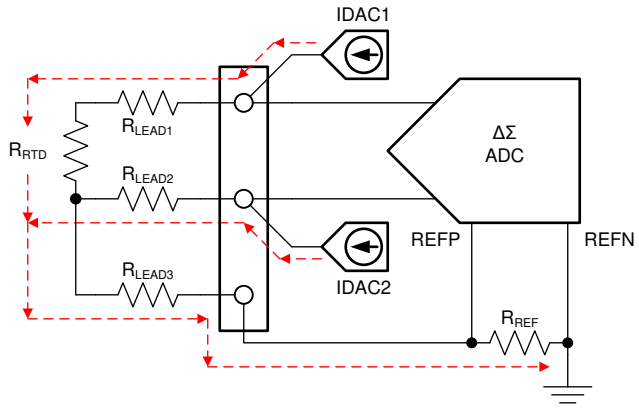

Figure 1-5. Example of Lead Wire Resistance Cancellation

With a single excitation current source, R_{LEAD1} adds an error to the measurement. By adding IDAC2, the second excitation current source is used to cancel out the error in the lead wire resistance. When adding the lead resistances and the second current source, the equation becomes:

$$\text{Output code} = 2^{23} \cdot [I_{IDAC1} \cdot (R_{RTD} + R_{LEAD1}) - (I_{IDAC2} \cdot R_{LEAD2})] / [(I_{IDAC1} + I_{IDAC2}) \cdot R_{REF}] \quad (6)$$

If the lead resistances match and the excitation currents match, then $R_{LEAD1} = R_{LEAD2}$ and $I_{IDAC1} = I_{IDAC2}$. The lead wire resistances cancel out so that Equation 6 reduces to the result in Equation 7 maintaining a ratiometric measurement.

$$\text{Output code} = 2^{23} \cdot R_{RTD} / (2 \cdot R_{REF}) = 2^{22} \cdot R_{RTD} / R_{REF} \quad (7)$$

$$R_{RTD} = \text{Output code} \cdot R_{REF} / 2^{22} \quad (8)$$

R_{LEAD3} is not part of the measurement, because it is not in the input measurement path or in the reference input path.

1.4.2 IDAC Current Chopping

As described in the previous section, the two current sources must be matched to cancel the lead resistances of the RTD wires. Any mismatch in the two current sources may be minimized by using the multiplexer (MUX) to swap or *chop* the two current sources between the two inputs. Taking two measurements in each configuration and averaging the results reduces the effects of mismatched current sources.

Using the configuration from Figure 1-5, Equation 6 results in the first measurement. Figure 1-6 swaps IDAC1 and IDAC2, and Equation 9 results in the second measurement.

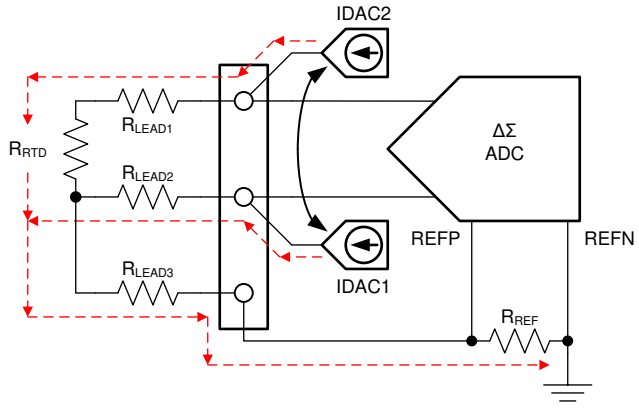

Figure 1-6. Swapping IDAC1 and IDAC2 to Chop the Measurement

$$\text{Output code} = 2^{23} \cdot [I_{IDAC2} \cdot (R_{LEAD1} + R_{RTD}) - (I_{IDAC1} \cdot R_{LEAD2})] / [(I_{IDAC1} + I_{IDAC2}) \cdot R_{REF}] \quad (9)$$

To chop the RTD measurement, we average the first and second measurements. Take Equation 6, add it to Equation 9 and then divide by two to average the result. This is shown in the following:

$$\text{Averaged output code} = 2^{23} \cdot \{[I_{IDAC1} \cdot (R_{LEAD1} + R_{RTD}) - (I_{IDAC2} \cdot R_{LEAD2})] + [I_{IDAC2} \cdot (R_{LEAD1} + R_{RTD}) - (I_{IDAC1} \cdot R_{LEAD2})]\} / \{2 \cdot [(I_{IDAC1} + I_{IDAC2}) \cdot R_{REF}]\} \quad (10)$$

Then combine $(I_{IDAC1} + I_{IDAC2})$ terms:

$$\text{Averaged output code} = 2^{23} \cdot [(I_{IDAC1} + I_{IDAC2}) \cdot (R_{LEAD1} + R_{RTD}) - (I_{IDAC1} + I_{IDAC2}) \cdot R_{LEAD2})] / [2 \cdot (I_{IDAC1} + I_{IDAC2}) \cdot R_{REF}] \quad (11)$$

Then cancel the $I_{IDAC1} + I_{IDAC2}$ terms and set $R_{LEAD1} = R_{LEAD2} = R_{LEAD}$ to get the following equations:

$$\text{Averaged output code} = 2^{23} \cdot [(R_{LEAD} + R_{RTD}) - R_{LEAD}] / (2 \cdot R_{REF})] \quad (12)$$

After this, the R_{LEAD} terms are cancelled as well.

$$\text{Averaged output code} = 2^{23} \cdot R_{RTD} / (2 \cdot R_{REF}) = 2^{22} \cdot R_{RTD} / R_{REF} \quad (13)$$

Going through the results to Equation 13, it is not important that I_{IDAC1} and I_{IDAC2} are not equal, it is only important that I_{IDAC1} and I_{IDAC2} are the same values after they are swapped. If they are the same, then the $(I_{IDAC1} + I_{IDAC2})$ terms cancel out.

There may still be errors in the system. Here, R_{LEAD1} and R_{LEAD2} are assumed to be the same. If they are different, this becomes an error. Also, if there are leakage currents in the measurement (from TVS or other protection diodes for example), then the leakage contributes to the error.

1.5 Design Considerations

Designing an RTD measurement system requires balancing several different design goals and circuit considerations. After selecting components and excitation magnitude, the designer must verify that the design fits in the operating range of the ADC which includes reference voltage magnitude, the input range of the PGA, and the compliance voltage of any excitation current sources. This section is a basic guide to setting the parameters of operation to design an RTD measurement system with precision ADCs. The basic ratiometric measurement shown in Figure 1-4 will be the starting point for an RTD measurement circuit.

Later sections describe different circuit topologies used for measurement of different RTD wiring configurations. By extension, calculations found here can be applied to different topologies shown later.

1.5.1 Identify the RTD Range of Operation

Start by determining the expected temperature measurement range required for the system, because this will set the range of RTD resistance measurement. As an example, start with a PT100 RTD. The resistance of a PT100 RTD over temperature was shown in Figure 1-1. If the required system temperature measurement range is –200°C to 850°C, this requires the full measurement range of a PT100 RTD. With this temperature range, the RTD would have an equivalent resistance range of 20 Ω to 400 Ω. Use this resistance range to start the design of the measurement system. Determining the temperature range and then the RTD resistance range helps set the excitation current, gain, and the reference resistance in the design.

1.5.2 Set the Excitation Current Sources and Consider RTD Self Heating

Many precision ADCs used for RTD measurement will have programmable excitation current sources (IDACs) in several magnitudes. A precision ADC device may have a matched pair of IDACs used for excitation. These IDACs can be set to currents of 10, 50, 100, 250, 500, 750, 1000, 1500, and 2000 µA. Excitation currents are used to drive both the RTD, the reference resistance and biasing resistors for some designs.

For the best noise performance, maximize the excitation current used for the RTD and reference resistance excitation. However, most excitation currents should be kept lower than 1 mA because of self heating. Because there is current running through the RTD, the RTD itself will dissipate power through heat. This self heating will cause an error in the measurement. The change in temperature (ΔT) is determined by the power dissipation of the RTD divided by the self-heating coefficient E, in mW/°C. This change in temperature becomes a temperature measurement error and is shown in Equation 14.

$$\Delta T = (I_{IDAC})^2 \bullet R_{RTD} / E \tag{14}$$

The typical range of RTD self-heating coefficients is 2.5 mW/°C for small, thin-film elements and 65 mW/°C for larger, wire-wound elements. With 1-mA excitation at the maximum RTD resistance value and a larger self-heating coefficient, the power dissipation in the RTD is less than 0.4 mW and will keep the measurement errors due to self-heating to less than 0.01°C. Self-heating coefficients will vary with RTD construction and the measurement medium (in air or in water, for example). Consult the RTD manufacturer data sheet for sensor characteristics.

Referring back to Figure 1-4, this topology uses a single IDAC current source. Other topologies may use matched sources to for lead current calculation.

1.5.3 Set Reference Voltage and PGA Gain

After selecting the IDAC current, use the maximum reference resistor possible, but consider several factors in the setting the reference. The reference voltage must be within the minimum and maximum reference voltages for operation. Many ADCs will have a minimum value of the reference of 0.5 V. Some devices will have a reference maximum of AVDD – AVSS, while others may have a lower maximum of AVDD – AVSS – 1 V. Consult the ADC data sheet for more specifications on the external reference input range.

A good selection for the reference voltage is using a value close to the midpoint of AVDD – AVSS. Often, this reference voltage is used to set up the common-mode voltage for the input measurement. PGA amplification may be limited by its input range and output swing. By setting the input common-mode voltage to the midpoint in the supplies, the PGA will have the maximum range possible. Many precision ADCs have a PGA that can amplify small input signals. These PGAs often will have gains from 1 V/V to 128 V/V in factors of 2.

Also, select a reference resistance that maximizes the usable input range of the ADC. As an example, it helps to show this with several values. Start with a 2-wire RTD ratiometric measurement with a PT100 where the maximum resistance is 400 Ω. This is the setup shown for a basic ratiometric measurement in Figure 1-4.

If the IDAC current is selected to be 1 mA, then the reference resistor could be chosen to be 1620 Ω. The measurement of the 400 Ω could be set to a PGA gain of 4. This would make the input voltage 1.6 V, while the reference voltage is set to 1.62 V. This would maximize the input voltage range of the ADC to 98.8% of the positive full-scale range. A reference resistor of 1600 Ω could have been chosen to maximize the ADC, however a small gain error or resistance error may push a 400 Ω measurement out of the range of operation. For this example, the next largest 1% resistor value above 1600 was selected.

Another benefit of setting the reference voltage to 1.62 V is that it sets the RTD measurement near the midpoint of the supply voltage. A reference of 1.62 V sets the input voltage for the ADC negative input. The input voltage is highest at the maximum RTD resistance is 0.4 V using an IDAC current of 1 mA and RTD resistance of 400 Ω. This sets the input voltage to 2.02 V for the ADC positive input.

Selecting a marginally larger resistance only reduces the resolution of the measurement. If the reference resistor is selected to be 2400 Ω then the reference voltage becomes 2.4 V. With an input to the ADC of 1.6 V (from 0.4 V after PGA gain of 4) compared to a reference voltage of 2.4 V, the ADC uses only 67% of the positive full-scale range.

1.5.4 Verify the Design Fits the Device Range of Operation

After determining the RTD range of operation, selecting the IDAC currents, the reference resistance, and the PGA gain, verify that the design still is within the range of operation of the device.

The PGA will have an input range dependent on the input common-mode voltage and the PGA gain. This may be different for each ADC. Determine the minimum and maximum input voltage and the common-mode voltage for each input voltage operation. By setting the input common-mode voltage to near mid-supply, the input voltage should be within the PGA range of operation. However, it is important to verify this through the equations given in the data sheet of the selected ADC. Consult the ADC data sheet for descriptions of the PGA and limitations in its input range.

Additionally, calculate the voltage at the output of the IDAC current sources. As the output voltage rises near the supply, the IDAC current will lose compliance as the output impedance of the current source is reduced. Calculate the voltage based on the IDAC currents driving the RTD resistance, reference resistance and bias resistance if necessary. If this voltage gets too close to the positive supply, the current may be reduced. Note that this compliance voltage will be different from device to device, and may vary by output current magnitude. Again, it is important to verify the compliance voltage based on the IDAC current source specifications in the data sheet of the selected ADC.

1.5.5 Design Iteration

If the design does not fall within the range of operation for the PGA, or is outside the compliance voltage of the IDAC, then another iteration the design may be necessary. It may be necessary to reduce or increase the reference resistance, or change any biasing resistors to set the PGA input range or set the IDAC output to with the compliance voltage.

2 RTD Measurement Circuits

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

The following sections describe circuit topologies for the three RTD wiring configurations. Each section provides the basic topology, with benefits and drawbacks for the circuit. Different topologies have different connections for analog inputs, reference inputs, and IDAC outputs. A basic theory of operation is provided with notes to guide the reader through important considerations in the design. However, a design procedure similar to the Design Considerations section can be followed to determine system values and parameters. Later sections describe measurements with different combinations of RTDs, allowing for more versatile temperature measurement systems. The circuits use a single ADC with a multiplexer to measure multiple elements and route excitation current to the sensor.

Conversion results are shown with a generic 24-bit bipolar ADC, using the positive full-scale range of the device. Conversions with 16-bit ADCs are similar in calculation. Results are shown as functions of the reference resistance. Conversion to temperature depends on the linearity and error of the individual RTD model, and is not discussed in this applications note.

2.1 Two-Wire RTD Measurement With Low-Side Reference

The most basic RTD measurement uses a two-wire RTD for temperature measurement. Shown below is a schematic and design for a two-wire RTD measurement with an ADC. A ratiometric measurement is created with the RTD as the input and a precision resistor as the reference input.

2.1.1 Schematic

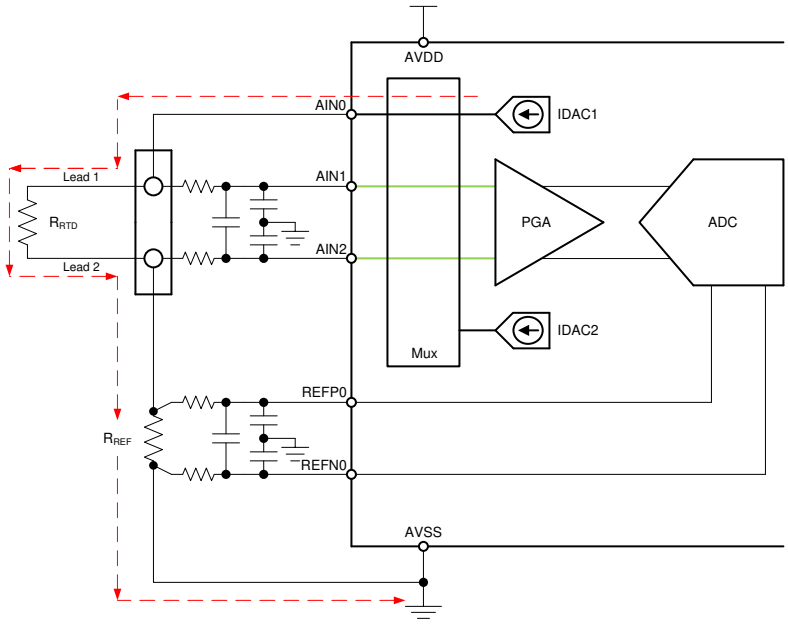

Figure 2-1. Two-Wire RTD, Low-Side Reference Measurement Circuit

2.1.2 Pros and Cons

Pros:

- Simplest implementation of RTD temperature measurement
- Uses only two analog input pins for measurement and one IDAC current for sensor and reference resistor excitation
- Good for local measurements, where the lead length and resistance are small
- Ratiometric measurement, IDAC noise and drift are cancelled

Cons:

- Least accurate measurement for RTDs
- No lead wire compensation; lead resistance affects measurement accuracy

2.1.3 Design Notes

An IDAC current source drives both the RTD and the reference resistor, R_{REF}. Because the same current drives both elements, the ADC measurement is a ratiometric measurement. Calculation for the RTD resistance does not require a conversion to a voltage, but does require a precision reference resistor with high accuracy and low drift.

The measurement circuit requires:

- Single dedicated IDAC output pin
- AINP and AINN inputs
- External reference input
- Precision reference resistor

First, identify the range of operation for the RTD. For example, a PT100 RTD has a range of 20 Ω to 400 Ω if the temperature measurement range is from −200°C to 850°C. The reference resistor must be larger than the maximum RTD value. The reference resistance and PGA gain determines the positive full-scale range of the measurement.

Then, choose the reference resistor and IDAC current value. Ideally, choosing the largest IDAC current provides the best performance by increasing the sensor signal above any noise in the system. However, there are several other considerations in determining the values. First, higher current may lead to self-heating of the RTD, which adds error to the measurement. Second, the reference resistance acts as a level shift for the sensor measurement. This level shift is used to raise the DC bias of the analog input signal so that the voltage is within the input range of the PGA. Generally, the analog input signal is set near mid-supply for best operation.

To verify that the design is within the ADC range of operation, Calculate the voltages for AIN1 and AIN2 and the maximum differential input voltage. Verify that V_{AIN1} and V_{AIN2} are within the input range of the PGA given the gain setting and supply voltage. Use the maximum RTD resistance based on the desired temperature measurement.

$$V_{AIN1} = I_{IDAC1} \bullet (R_{RTD} + R_{REF}) \quad (15)$$

$$V_{AIN2} = I_{IDAC1} \bullet R_{REF} \quad (16)$$

Additionally, the output voltage of the IDAC source calculated from V_{AIN1} must be low enough from AVDD to be within the compliance voltage of the IDAC current source. When the IDAC output voltage rises too close to AVDD, the IDAC loses compliance and the excitation current is reduced.

The reference resistor, R_{REF} must be a precision resistor with high accuracy and low drift. Any error in the R_{REF} reflects the same error in the RTD measurement. The REFP0 and REFN0 pins are shown connecting to the R_{REF} resistor as a Kelvin connection to get the best measurement of the reference voltage. This eliminates any series resistance as an error from the reference resistance measurement.

The lead wire resistance is an error term in the two-wire RTD measurement. The previous calculations neglect the lead resistances, but can be added to the R_{RTD} term.

2.1.4 Measurement Conversion

$$\text{Output Code} = 2^{23} \bullet \text{Gain} \bullet V_{RTD} / V_{REF} = 2^{23} \bullet \text{Gain} \bullet (I_{IDAC1} \bullet R_{RTD}) / (I_{IDAC1} \bullet R_{REF}) = 2^{23} \bullet \text{Gain} \bullet R_{RTD} / R_{REF} \quad (17)$$

$$R_{RTD} = R_{REF} \bullet \text{Output Code} / (2^{23} \bullet \text{Gain}) \quad (18)$$

2.1.5 Generic Register Settings

- Select multiplexer settings for AINP and AINN to measure leads 1 and 2 of the RTD
- Enable the PGA, set gain to desired value
- Select data rate and digital filter settings
- Select reference input to measure R_{REF} for ratiometric measurement
- Enable the internal reference (the IDAC requires an enabled internal reference)
- Set IDAC magnitude and select IDAC1 output pin to drive lead 1 of the RTD

2.2 Two-Wire RTD Measurement With High-Side Reference

A two-wire RTD temperature measurement may also be made with a high-side reference. By itself, a high-side reference does not have any benefit over a low-side reference in a two-wire RTD application. However, it may be used to set up other RTD measurements with a high-side reference.

2.2.1 Schematic

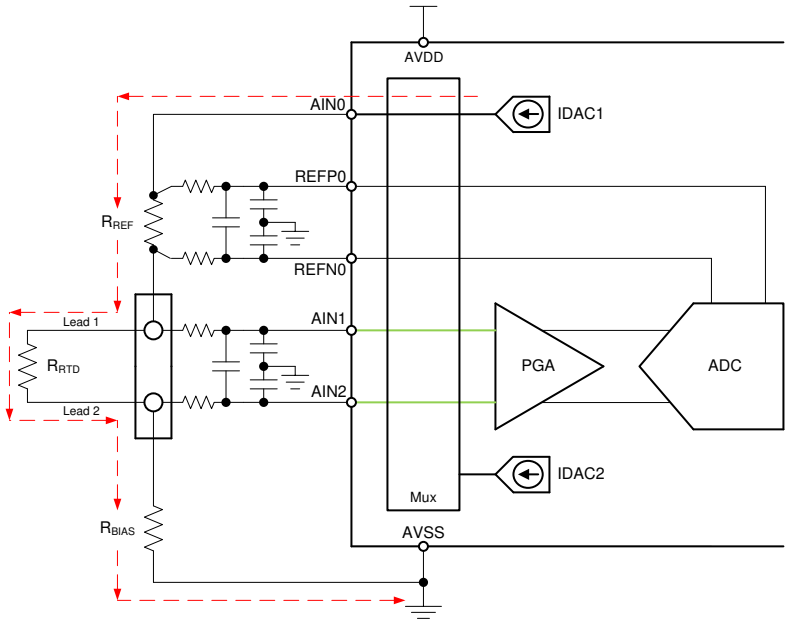

Figure 2-2. Two-Wire RTD, High-Side Reference Measurement Circuit

2.2.2 Pros and Cons

Pros:

- Simple implementation of RTD temperature measurement
- Requires only two analog input pins for measurement and one IDAC current for sensor and reference resistor excitation
- Good for local measurements, where the lead length and resistance are small
- Ratiometric measurement, IDAC noise and drift are cancelled

Cons:

- Least accurate measurement for RTDs
- No lead wire compensation; lead resistance affects measurement
- Requires R_{BIAS} to set the input common-mode voltage of the RTD measurement accuracy

2.2.3 Design Notes

An IDAC current source drives the RTD, R_{REF}, and R_{BIAS}. Similar to the two-wire RTD design in Section 2.1, the same current drives both the RTD and R_{REF}, creating a ratiometric measurement so that the ADC output is calculated as a ratio between the RTD resistance and the reference resistance.

However, in a high-side reference application, the measurement requires R_{BIAS} to set the RTD measurement near mid-supply, so that AIN1 and AIN2 are in the range of the PGA. Additionally, using R_{BIAS} increases the DC voltage seen at AIN0, which must be low enough to be within the compliance voltage of the IDAC output.

The measurement circuit requires:

- Single dedicated IDAC output pin
- AINP and AINN inputs
- External reference input
- Precision reference resistor
- Biasing resistor to level-shift the input measurement within the range of the PGA

First, identify the range of operation for the RTD. The reference resistance and PGA gain determines the positive full-scale range of the measurement.

Then, choose the reference resistor and IDAC current value. As in the previous circuit topology, choosing the reference resistor and IDAC current balances several design considerations including signal noise, RTD self-heating, setting the input near mid-supply to keep the measurement within the input range of the PGA, and keeping the output voltage of the IDAC within the compliance output voltage. In this high-side reference, the compliance range is more likely to be violated because there is more resistance with the addition of R_{BIAS}.

To verify that the design is within the ADC range of operation, Calculate the voltages for AIN1 and AIN2 and the maximum differential input voltage. Verify that V_{AIN1} and V_{AIN2} are within the input range of the PGA given the gain setting and supply voltage. Use the maximum RTD resistance based on the desired temperature measurement. The R_{BIAS} resistance acts as a level shift for the sensor measurement. This level shift raises the DC bias of the analog input signal so that the voltage is within the input range of the PGA. Generally the analog input signal is set near mid-supply for best operation.

$$V_{AIN1} = I_{IDAC1} \cdot (R_{RTD} + R_{BIAS}) \quad (19)$$

$$V_{AIN2} = I_{IDAC1} \cdot R_{BIAS} \quad (20)$$

Finally, the output voltage of the IDAC source calculated from V_{AIN0} must be low enough from AVDD to be within the compliance voltage of the IDAC current source. With the addition of R_{BIAS}, the voltage seen across the sum of R_{REF}, R_{RTD}, and R_{BIAS} is significantly higher than the low-side-reference example. When the IDAC output voltage rises too close to AVDD, the IDAC loses compliance and the excitation current is reduced. The output voltage of the IDAC at AIN0 can be calculated from Equation 21.

$$V_{AIN0} = I_{IDAC1} \cdot (R_{REF} + R_{RTD} + R_{BIAS}) \quad (21)$$

The reference resistor, R_{REF} must be a precision resistor with high accuracy and low drift. Any error in the R_{REF} reflects the same error in the RTD measurement. The REFP0 and REFN0 pins are shown connecting to the R_{REF} resistor as a Kelvin connection to get the best measurement of the reference voltage. This eliminates any series resistance as an error from the reference resistance measurement.

The lead wire resistance is an error term in the two-wire RTD measurement. The previous calculations neglect the lead resistances, but can be added to the R_{RTD} term.

2.2.4 Measurement Conversion

$$\text{Output code} = 2^{23} \cdot \text{Gain} \cdot V_{RTD} / V_{REF} = 2^{23} \cdot \text{Gain} \cdot I_{IDAC1} \cdot R_{RTD} / (I_{IDAC1} \cdot R_{REF}) = 2^{23} \cdot \text{Gain} \cdot R_{RTD} / R_{REF} \quad (22)$$

$$R_{RTD} = R_{REF} \cdot \text{Output code} / (2^{23} \cdot \text{Gain}) \quad (23)$$

2.2.5 Generic Register Settings

- Select multiplexer settings for AINP and AINN to measure leads 1 and 2 of the RTD
- Enable the PGA, set gain to desired value
- Select data rate and digital filter settings
- Select reference input to measure R_{REF} for ratiometric measurement
- Enable the internal reference (the IDAC requires an enabled internal reference)
- Set IDAC magnitude and select IDAC1 output pin to drive REFP0

2.3 Three-Wire RTD Measurement, Low-Side Reference

Using matched IDAC current sources, the error from RTD lead resistances can be removed. A three-wire RTD is required for this measurement using a low-side reference.

2.3.1 Schematic

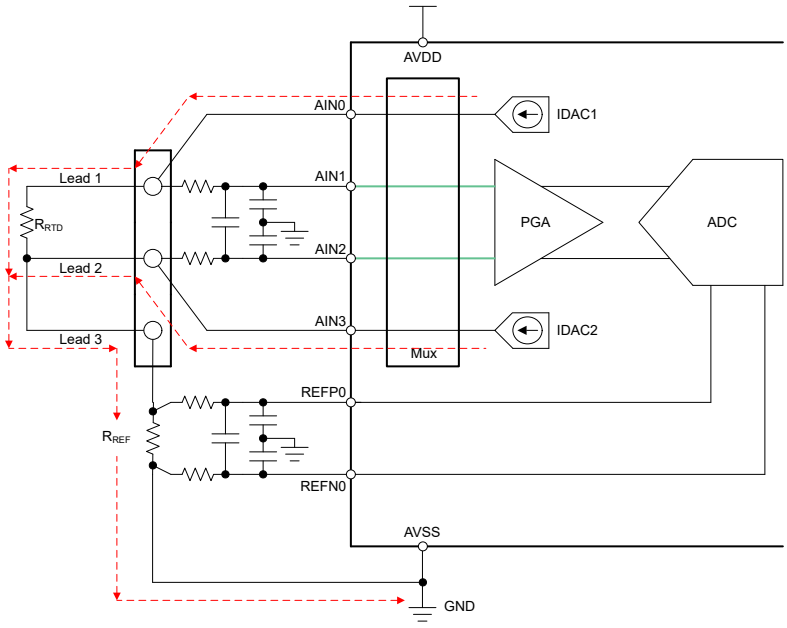

Figure 2-3. Three-Wire RTD, Low-Side Reference Measurement Circuit

2.3.2 Pros and Cons

Pros:

- IDAC currents are used for sensor and reference resistor excitation
- Allows for lead wire compensation; errors from voltage drops across lead resistances are removed
- Ratiometric measurement, IDAC noise and drift are cancelled

Cons:

- Requires two matched IDAC currents for both lead wire compensation and for R_{RTD} measurement

2.3.3 Design Notes

For this three-wire RTD design, two matched IDAC current sources are used to actively cancel the lead resistance errors. IDAC1 sources current through lead 1 of the RTD to both the RTD and the reference resistor, R_{REF}. IDAC2 sources current through lead 2 of the RTD to the reference resistor. If IDAC1 and IDAC2 are identical and the lead resistances match, then the error from the lead resistances cancels in the measurement made from AIN1 and AIN2.

The measurement circuit requires:

- Two dedicated IDAC output pins
- AINP and AINN inputs
- External reference input
- Precision reference resistor

Note that the RTD is driven from IDAC1 while R_{REF} is driven by IDAC1 and IDAC2 combined. Presuming that the IDAC currents match, the measurement is also ratiometric, and does not require converting the input or reference to voltage for the conversion. As with the two-wire RTD measurement, the topology requires a precision reference resistor with high accuracy and low drift.

IDAC currents from AIN0 and AIN3 are driven into two of the three RTD leads. IDAC1 drives the RTD and one lead resistance, while IDAC2 drives the second lead resistance. The voltage drop across the lead resistances cancel each other in the ADC measurement, assuming the IDAC currents match and the lead resistances match.

Without the lead resistances, the measurement voltage is $I_{IDAC1} \cdot R_{RTD}$, while the reference voltage is $(I_{IDAC1} + I_{IDAC2}) \cdot R_{REF}$. If the two IDAC currents match, the IDAC terms drop out of the measurement conversion.

The following shows how the matched IDAC sources cancel the lead resistance errors. Equation 24 and Equation 25 start with the voltages at AIN1 and AIN2 and include the lead resistance contribution.

$$V_{AIN1} = [I_{IDAC1} \cdot (R_{RTD} + R_{LEAD1})] + [(I_{IDAC1} + I_{IDAC2}) \cdot (R_{LEAD3} + R_{REF})] \quad (24)$$

$$V_{AIN2} = (I_{IDAC2} \cdot R_{LEAD2}) + [(I_{IDAC1} + I_{IDAC2}) \cdot (R_{LEAD3} + R_{REF})] \quad (25)$$

The ADC input voltage measures $V_{AIN1} - V_{AIN2}$, with R_{LEAD3} and R_{REF} terms dropping out.

$$V_{AIN1} - V_{AIN2} = [I_{IDAC1} \cdot (R_{RTD} + R_{LEAD1})] - (I_{IDAC2} \cdot R_{LEAD2}) \quad (26)$$

Assuming the lead resistances are equal and the IDAC currents are matched, so that $R_{LEAD1} = R_{LEAD2} = R_{LEAD}$ and $I_{IDAC1} = I_{IDAC2} = I_{IDAC}$. The result becomes:

$$V_{AIN1} - V_{AIN2} = I_{IDAC} \cdot R_{RTD} \quad (27)$$

At the same time, the reference resistor shunts the sum of I_{IDAC1} and I_{IDAC2} to become:

$$V_{REF} = (I_{IDAC1} + I_{IDAC2}) \cdot R_{REF} = 2 \cdot I_{IDAC} \cdot R_{REF} \quad (28)$$

As with the two wire RTD example, start the design with the expected usable range of the RTD. The reference resistor and IDAC current values are chosen to place the input voltage within the PGA range, while ensuring that the IDAC is operating within its compliance voltage. As in all ratiometric measurements, the reference resistor, R_{REF} must be a precision resistor with high accuracy and low drift.

To verify that the design is within the ADC range of operation, start by calculating the voltages of AIN1 and AIN2 and the maximum differential input voltage. Assuming the lead resistances are small and can be ignored, Equation 24 and Equation 25 reduce to Equation 29 and Equation 30. Verify that V_{AIN1} and V_{AIN2} are within the input range of the PGA given the gain setting and supply voltage. Use the maximum RTD resistance based on the desired temperature measurement.

$$V_{AIN1} = (I_{IDAC1} \cdot R_{RTD}) + (I_{IDAC1} + I_{IDAC2}) \cdot R_{REF} \quad (29)$$

$$V_{AIN2} = (I_{IDAC1} + I_{IDAC2}) \cdot R_{REF} \quad (30)$$

Additionally, verify the output voltage of the IDAC sources calculated from V_{AIN0} and V_{AIN3} are low enough from AVDD to be within the compliance voltage of the IDAC current source. Because the voltage for IDAC1 always be higher than that of IDAC2, it is sufficient to calculate the output voltage at V_{AIN0} to verify the IDAC compliance voltage. This calculation is already shown in Equation 29, because V_{AIN0} is the same potential as V_{AIN1}.

The reference resistor, R_{REF} must be a precision resistor with high accuracy and low drift. Any error in the R_{REF} reflects the same error in the RTD measurement. The REFP0 and REFN0 pins are shown connecting to the R_{REF} resistor as a Kelvin connection to get the best measurement of the reference voltage. This eliminates any series resistance as an error from the reference resistance measurement.

2.3.4 Measurement Conversion

$$\text{Output code} = 2^{23} \cdot \text{Gain} \cdot V_{RTD} / V_{REF} = 2^{23} \cdot \text{Gain} \cdot I_{IDAC} \cdot R_{RTD} / (2 \cdot I_{IDAC} \cdot R_{REF}) = 2^{22} \cdot \text{Gain} \cdot R_{RTD} / R_{REF} \quad (31)$$

$$R_{RTD} = R_{REF} \cdot \text{Output code} / (2^{22} \cdot \text{Gain}) \quad (32)$$

2.3.5 Generic Register Settings

- Select multiplexer settings for AINP and AINN to measure leads 1 and 2 of the RTD
- Enable the PGA, set gain to desired value
- Select data rate and digital filter settings
- Select reference input to measure R_{REF} for ratiometric measurement
- Enable the internal reference (the IDAC requires an enabled internal reference)

- Set IDAC magnitude and select IDAC1 output pin to drive lead 1 of the RTD and select IDAC2 output pin to drive lead 2 of the RTD

2.3.6 Chopping IDAC Currents for Matching

As previously mentioned, IDAC current matching is important. The impact of IDAC current mismatch is small for lead compensation because the additional error is small. However, IDAC current mismatch results in a gain error in the RTD measurement. As an example if IDAC2 is larger than IDAC1 by 1%, the reference would be 0.5% larger than expected, resulting in a 0.5% gain error:

$$V_{REF} = (I_{IDAC1} + 1.01 \cdot I_{IDAC1}) \cdot R_{REF} = 2.01 \cdot I_{IDAC1} \cdot R_{REF} \quad (33)$$

This gain error due to mismatched IDAC current sources can be removed by chopping the IDAC currents. Chopping is achieved by making a measurement and averaging this first measurement with a second measurement after the IDAC currents have been swapped. Starting with the original configuration, the input voltage and reference voltage are given in the following. Equation 34 shows the first measurement, while Equation 35 shows the reference voltage.

$$V_{MEAS1} = [I_{IDAC1} \cdot (R_{RTD} + R_{LEAD1})] - (I_{IDAC2} \cdot R_{LEAD2}) \quad (34)$$

$$V_{REF} = (I_{IDAC1} + I_{IDAC2}) \cdot R_{REF} \quad (35)$$

If the IDACs are swapped so that IDAC2 is sourced from AIN0, and IDAC1 is sourced from AIN3, the reference voltage stays the same. However, the second measurement now becomes:

$$V_{MEAS2} = [I_{IDAC2} \cdot (R_{RTD} + R_{LEAD1})] - (I_{IDAC1} \cdot R_{LEAD2}) \quad (36)$$

Averaging the first input measurement and the second input measurement, the result is:

$$(V_{MEAS1} + V_{MEAS2}) / 2 = [(I_{IDAC1} + I_{IDAC1}) \cdot (R_{RTD} + R_{LEAD1}) / 2] - [(I_{IDAC1} + I_{IDAC1}) \cdot R_{LEAD2} / 2] \quad (37)$$

The resulting ADC measurement is:

$$\text{Averaged output code} = 2^{23} \cdot \text{Gain} \cdot \{[(I_{IDAC1} + I_{IDAC1}) \cdot (R_{RTD} + R_{LEAD1}) / 2] - [(I_{IDAC1} + I_{IDAC1}) \cdot R_{LEAD2} / 2]\} / (I_{IDAC1} + I_{IDAC2}) \cdot R_{REF} \quad (38)$$

Using averaging, the $(I_{IDAC1} + I_{IDAC2})$ terms cancel; and if the lead wire resistances are equal, they are cancelled as well:

$$\text{Averaged output code} = 2^{23} \cdot \text{Gain} \cdot R_{RTD} / (2 \cdot R_{REF}) = 2^{22} \cdot \text{Gain} \cdot R_{RTD} / R_{REF} \quad (39)$$

$$R_{RTD} = R_{REF} \cdot \text{Averaged output code} / (2^{22} \cdot \text{Gain}) \quad (40)$$

With averaging, the ADC output code is no longer dependent on IDAC current matching, resulting in a more accurate measurement.

For chopping IDAC currents, set the register values:

- For the first measurement, select multiplexer settings for AINP and AINN to measure leads 1 and 2 of the three-wire RTD
- Enable the PGA, set gain to desired value
- Select data rate and digital filter settings
- Select reference input to measure R_{REF} for ratiometric measurement
- Enable the internal reference (the IDAC requires an enabled internal reference)
- Set IDAC magnitude and select IDAC1 output pin to drive lead 1 of the RTD and select IDAC2 output pin to drive lead 2 of the RTD
- For the second measurement, swap the IDAC output pins, select IDAC2 output pin to drive lead 1 of the RTD and select IDAC1 output pin to drive lead 2 of the RTD
- Average the first and second measurements

2.4 Three-Wire RTD Measurement, Low-Side Reference, One IDAC Current Source

In this circuit topology, two measurements are used to make the RTD measurement and compensate for the lead wire resistance. Instead of using two matched IDAC current sources to cancel the lead resistance, a single IDAC current is used and the lead resistance is measured separately for cancellation.

2.4.1 Schematic

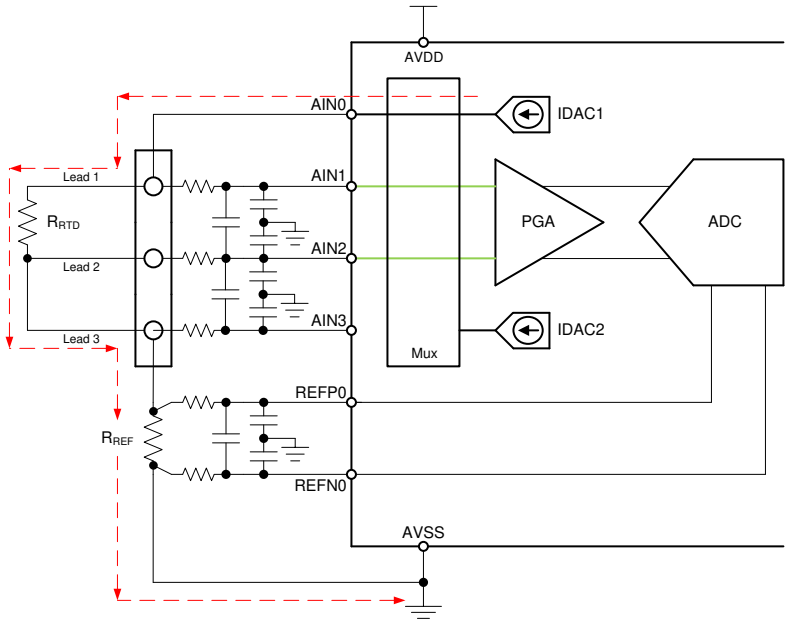

Figure 2-4. Three-Wire RTD, Low-Side Reference Measurement Circuit With One IDAC Current Source

2.4.2 Pros and Cons

Pros:

- Single IDAC current is used for sensor and reference resistor excitation; does not require chopping for IDAC mismatch
- Allows for lead wire compensation; errors from voltage drops across lead resistances are removed
- Ratiometric measurement, IDAC noise and drift are cancelled

Cons:

- Requires two measurements to remove lead resistance error

2.4.3 Design Notes

In this topology, two measurements are taken for lead resistance cancellation. In the first measurement, the ADC measures the voltage across the RTD and the resistance for lead 1 as driven by the single excitation current source. In the second measurement, the ADC measures the resistance for lead 3 as driven by the same excitation current source. This method assumes that the resistance in lead 1 and lead 3 are equal. By subtracting the second measurement from the first, the RTD resistance can be accurately measured, and the lead resistance cancelled.

The measurement circuit requires:

- Single dedicated IDAC output pin
- AINP and AINN inputs
- A measurement for the RTD and a parasitic lead resistance
- A second measurement to measure an equivalent lead resistance to cancel
- External reference input
- Precision reference resistor

Starting with IDAC1 driving AIN0, the voltage at AIN1 and AIN2 can be calculated. For the first measurement:

$$V_{AIN1} = I_{IDAC1} \cdot (R_{RTD} + R_{LEAD1} + R_{LEAD3} + R_{REF}) \quad (41)$$

$$V_{AIN2} = I_{IDAC1} \cdot (R_{LEAD3} + R_{REF}) \quad (42)$$

$$V_{MEAS1} = V_{AIN1} - V_{AIN2} = I_{IDAC1} \cdot (R_{RTD} + R_{LEAD1}) \quad (43)$$

Because current does not flow through lead 2, there is no R_{LEAD2} term in the measurement. For the second measurement, the ADC measures the voltage from AIN2 to AIN3.

$$V_{AIN3} = I_{IDAC1} \cdot R_{REF} \quad (44)$$

$$V_{MEAS2} = V_{AIN2} - V_{AIN3} = I_{IDAC1} \cdot R_{LEAD3} \quad (45)$$

V_{MEAS2} yields the measurement of the lead 3 resistance. Subtracting V_{MEAS2} from V_{MEAS1}, the result is:

$$V_{MEAS1} - V_{MEAS2} = [I_{IDAC1} \cdot (R_{RTD} + R_{LEAD1})] - (I_{IDAC1} \cdot R_{LEAD3}) \quad (46)$$

Assuming the resistance from lead 1 equals the resistance from lead 3, the result is:

$$V_{MEAS1} - V_{MEAS2} = I_{IDAC1} \cdot (R_{RTD} + R_{LEAD1} - R_{LEAD3}) = I_{IDAC1} \cdot R_{RTD} \quad (47)$$

For both V_{MEAS1} and V_{MEAS2}, the reference resistor shunts I_{IDAC1} for a reference voltage of:

$$V_{REF} = I_{IDAC} \cdot R_{REF} \quad (48)$$

As with the previous examples, start the design with the expected usable range of the RTD. The reference resistor and IDAC current values are chosen to place the input voltage within the PGA range, while ensuring that the IDAC is operating within its compliance voltage. As in all ratiometric measurements, the reference resistor, R_{REF} must be a precision resistor with high accuracy and low drift.

To verify that the design is within the PGA range of operation, start by calculating the voltages of AIN1 and AIN2 and the maximum differential input voltage. Assuming the lead resistances are small and can be ignored, Equation 41 and Equation 42 reduce to Equation 49 and Equation 50. Verify that V_{AIN1} and V_{AIN2} are within the input range of the PGA given the gain setting and supply voltage. Use the maximum RTD resistance based on the desired temperature measurement.

$$V_{AIN1} = I_{IDAC1} \cdot (R_{RTD} + R_{REF}) \quad (49)$$

$$V_{AIN2} = I_{IDAC1} \cdot R_{REF} \quad (50)$$

Additionally, verify the output voltage of the IDAC sources calculated from V_{AIN0} and V_{AIN3} are low enough from AVDD to be within the compliance voltage of the IDAC current source. Because the voltage for IDAC1 always be higher than that of IDAC2, it is sufficient to calculate the output voltage at V_{AIN0} to verify the IDAC compliance voltage. This calculation is already shown in Equation 49, because V_{AIN0} is the same potential as V_{AIN1}.

The reference resistor, R_{REF} must be a precision resistor with high accuracy and low drift. Any error in the R_{REF} reflects the same error in the RTD measurement. The REFP0 and REFN0 pins are shown connecting to the R_{REF} resistor as a Kelvin connection to get the best measurement of the reference voltage. This eliminates any series resistance as an error from the reference resistance measurement.

2.4.4 Measurement Conversion

Measure the voltage of $V_{MEAS1} = V_{RTD} + V_{LEAD1}$:

$$\text{Output code 1} = 2^{23} \cdot \text{Gain} \cdot (V_{RTD} + V_{LEAD1}) / V_{REF} = 2^{23} \cdot \text{Gain} \cdot I_{IDAC} \cdot (R_{RTD} + R_{LEAD1}) / (I_{IDAC} \cdot R_{REF}) = 2^{23} \cdot \text{Gain} \cdot (R_{RTD} + R_{LEAD1}) / R_{REF} \quad (51)$$

Measure the voltage of $V_{MEAS2} = V_{LEAD3}$:

$$\text{Output code 2} = 2^{23} \cdot \text{Gain} \cdot V_{LEAD3} / V_{REF} = 2^{23} \cdot \text{Gain} \cdot I_{IDAC} \cdot R_{LEAD3} / (I_{IDAC} \cdot R_{REF}) = 2^{23} \cdot \text{Gain} \cdot R_{LEAD3} / R_{REF} \quad (52)$$

Assuming the lead resistances are equal, subtract V_{MEAS2} from V_{MEAS1} to get the RTD measurement:

$$\text{Output code 1} - \text{Output code 2} = [2^{23} \cdot \text{Gain} \cdot (V_{RTD} + V_{LEAD1}) / V_{REF}] - [2^{23} \cdot \text{Gain} \cdot R_{LEAD3} / R_{REF}] = 2^{23} \cdot \text{Gain} \cdot V_{RTD} / V_{REF} \quad (53)$$

$$R_{RTD} = R_{REF} \cdot (\text{Output code 1} - \text{Output code 2}) / (2^{23} \cdot \text{Gain}) \quad (54)$$

2.4.5 Configuration Register Settings

- For the first measurement, select multiplexer settings for AINP and AINN to measure leads 1 and 2 of the three-wire RTD
- Enable the PGA, set gain to desired value
- Select data rate and digital filter settings
- Select reference input to measure R_{REF} for ratiometric measurement
- Enable the internal reference (the IDAC requires an enabled internal reference)
- Set IDAC magnitude and select IDAC1 output pin to drive lead 1 of the RTD and select IDAC2 output pin to drive lead 2 of the RTD
- For the second measurement, select the multiplexer settings for AINP and AINN to measure leads 2 and 3 of the three-wire RTD
- Subtract the second measurement from the first measurement to remove the lead resistance

2.5 Three-Wire RTD Measurement, High-Side Reference

Using a high side reference in the measurement reduces the matching requirement for IDAC1 and IDAC2. In this topology, a single IDAC current goes through the RTD and R_{REF}, removing the gain error from IDAC mismatch.

2.5.1 Schematic

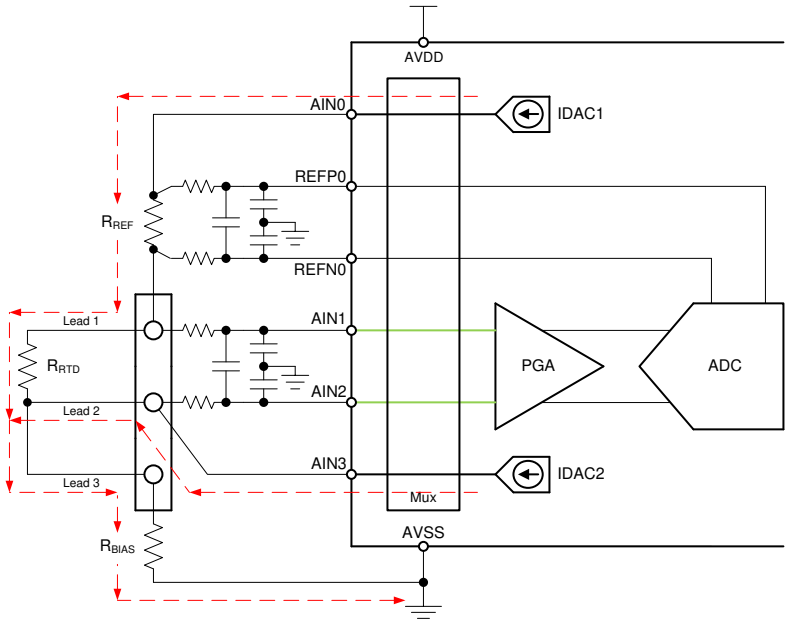

Figure 2-5. Three-Wire RTD, High-Side Reference Measurement Circuit

2.5.2 Pros and Cons

Pros:

- Single IDAC current is used for sensor and reference resistor excitation, measurement is less reliant on IDAC current match
- Allows for lead wire compensation; voltage drops across lead resistances are compensated
- Ratiometric measurement, IDAC noise and drift are cancelled

Cons:

- Requires R_{BIAS} to set the input common mode voltage of the RTD measurement

2.5.3 Design Notes

Similar to the three-wire RTD measurement with a low side reference, measurement with a high side reference uses lead wire compensation to remove the lead resistance as an error in the measurement. However, using the high side reference, the same current is used to drive the reference resistor and the RTD. The lead wire compensation using the second IDAC current does not introduce a gain error term with mismatched IDACs. Using the high side reference makes this measurement less reliant on IDAC current mismatch so that chopping is not required.

The measurement circuit requires:

- Single dedicated IDAC output pin
- AINP and AINN inputs
- External reference input
- Precision reference resistor

IDAC1 sources current to R_{REF} which then flows into to lead 1 of the three-wire RTD. Similar to the low side current measurement, IDAC2 sources current to lead 2 of the RTD to cancel the error from lead wire resistance. IDAC1 and IDAC2 sum into R_{BIAS}, which is required to establish the DC offset of the input signal. This DC offset sets the RTD voltage near mid-supply so the input is within the input range of the PGA.

As with the previous topologies, this measurement is ratiometric, and does not require converting the input or reference to voltage for the conversion. Also as in the previous RTD measurements, the topology requires a precision reference resistor with high accuracy and low drift.

Calculating the input voltages at AIN1 and AIN2, the result is:

$$V_{AIN1} = [I_{IDAC1} \cdot (R_{RTD} + R_{LEAD1})] + [(I_{IDAC1} + I_{IDAC2}) \cdot (R_{LEAD3} + R_{BIAS})] \quad (55)$$

$$V_{AIN2} = (I_{IDAC2} \cdot R_{LEAD2}) + [(I_{IDAC1} + I_{IDAC2}) \cdot (R_{LEAD3} + R_{BIAS})] \quad (56)$$

The ADC input voltage measures $V_{AIN1} – V_{AIN2}$, with R_{LEAD3} and R_{BIAS} terms dropping out.

$$V_{AIN1} – V_{AIN2} = [I_{IDAC1} \cdot (R_{RTD} + R_{LEAD1})] – (I_{IDAC2} \cdot R_{LEAD2}) \quad (57)$$

Assuming lead resistances are equal and IDAC currents are matched, with $I_{IDAC1} = I_{IDAC2} = I_{IDAC}$. The result becomes:

$$V_{AIN1} – V_{AIN2} = I_{IDAC1} \cdot R_{RTD} \quad (58)$$

At the same time, the reference resistor is driven from only IDAC1:

$$V_{REF} = I_{IDAC1} \cdot R_{REF} \quad (59)$$

As with the previous examples, start the design with the expected usable range of the RTD. The reference resistor and IDAC current values are chosen to place the input voltage within the PGA range, while ensuring that the IDAC is operating within its compliance voltage. As in all ratiometric measurements, the reference resistor, R_{REF} must be a precision resistor with high accuracy and low drift.

To verify that the design is within the PGA range of operation, start by calculating the voltages of AIN1 and AIN2 and the maximum differential input voltage. Assuming the lead resistances are small and can be ignored, Equation 55 and Equation 56 reduce to Equation 60 and Equation 61. Verify that V_{AIN1} and V_{AIN2} are within the input range of the PGA given the gain setting and supply voltage. Use the maximum RTD resistance based on the desired temperature measurement.

$$V_{AIN1} = (I_{IDAC1} \cdot R_{RTD}) + [(I_{IDAC1} + I_{IDAC2}) \cdot R_{BIAS}] \quad (60)$$

$$V_{AIN2} = (I_{IDAC1} + I_{IDAC2}) \cdot (R_{BIAS}) \quad (61)$$

Additionally, verify the output voltage of the IDAC sources calculated from V_{AIN0} and V_{AIN3} are low enough from AVDD to be within the compliance voltage of the IDAC current source. Because the voltage for IDAC1 always be higher than that of IDAC2, it is sufficient to calculate the output voltage at V_{AIN0} to verify the IDAC compliance voltage. The output voltage of the IDAC at AIN0 can be calculated from Equation 62.

$$V_{AIN0} = [I_{IDAC1} \cdot (R_{REF} + R_{RTD})] + [(I_{IDAC1} + I_{IDAC2}) \cdot R_{BIAS}] \quad (62)$$

The reference resistor, R_{REF} must be a precision resistor with high accuracy and low drift. Any error in the R_{REF} reflects the same error in the RTD measurement. The REFP0 and REFN0 pins are shown connecting to the R_{REF} resistor as a Kelvin connection to get the best measurement of the reference voltage. This eliminates any series resistance as an error from the reference resistance measurement.

2.5.4 Measurement Conversion

$$\text{Output Code} = 2^{23} \cdot \text{Gain} \cdot V_{RTD} / V_{REF} = 2^{23} \cdot \text{Gain} \cdot I_{IDAC} \cdot R_{RTD} / (I_{IDAC} \cdot R_{REF}) = 2^{23} \cdot \text{Gain} \cdot R_{RTD} / R_{REF} \quad (63)$$

$$R_{RTD} = R_{REF} \cdot \text{Output code} / (2^{23} \cdot \text{Gain}) \quad (64)$$

2.5.5 Configuration Register Settings

For the measurement, set the register values:

- Select multiplexer settings for AINP and AINN to measure leads 1 and 2 of the RTD
- Enable the PGA, set gain to desired value
- Select data rate and digital filter settings
- Select reference input to measure R_{REF} for ratiometric measurement
- Enable the internal reference (the IDAC requires an enabled internal reference)
- Set IDAC magnitude and select IDAC1 output pin to drive the reference resistor R_{REF} and select IDAC2 output pin to drive lead 2 of the RTD

2.6 Four-Wire RTD Measurement, Low-Side Reference

A four-wire RTD has the best measurement accuracy. The lead resistance reacting with the IDAC current does not add an error term for the ADC measurement.

2.6.1 Schematic

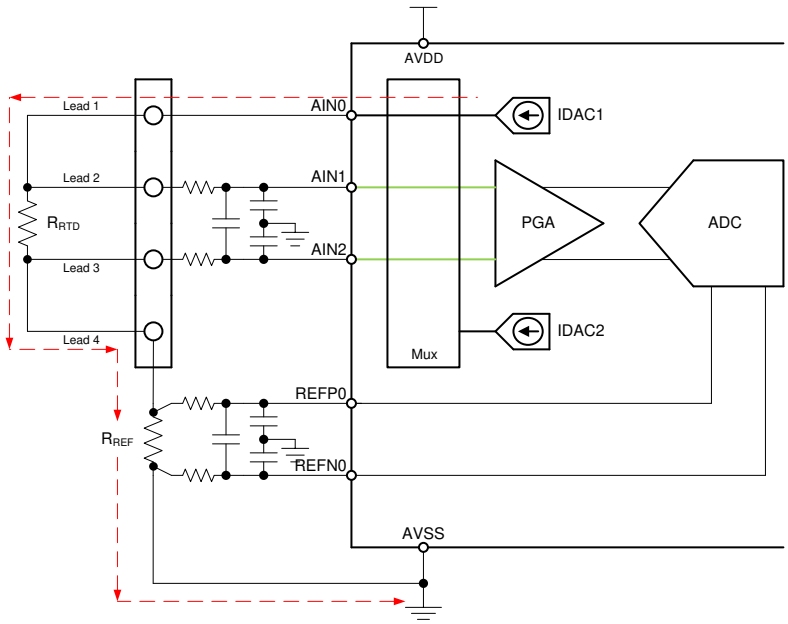

Figure 2-6. Four-Wire RTD, Low-Side Reference Measurement Circuit

2.6.2 Pros and Cons

Pros:

- Single IDAC current is used for sensor and reference resistor excitation
- Most accurate RTD measurement, no need for lead compensation
- Ratiometric measurement, IDAC noise and drift are cancelled

Cons:

- The four-wire RTD is the most expensive RTD configuration

2.6.3 Design Notes

This design should be exactly the same as in the two-wire RTD design in Section 2.1. The IDAC current is being routed through an alternate input and measurements are taken from AIN1 and AIN2. However, the considerations in reference resistor size, IDAC current, reference voltage, and PGA input voltage are exactly the same.

The measurement circuit requires:

- Single dedicated IDAC output pin
- AINP and AINN inputs
- External reference input

- Precision reference resistor

To verify that the design is within the ADC range of operation, Calculate the voltages for AIN1 and AIN2 and the maximum differential input voltage. Verify that V_{AIN1} and V_{AIN2} are within the input range of the PGA given the gain setting and supply voltage. Use the maximum RTD resistance based on the desired temperature measurement.

$$V_{AIN1} = I_{IDAC1} \cdot (R_{RTD} + R_{REF}) \quad (65)$$

$$V_{AIN2} = I_{IDAC1} \cdot R_{REF} \quad (66)$$

Additionally, verify that the voltage seen at the IDAC pin (where $V_{AIN0} = V_{AIN1}$) is within the current source compliance voltage. When the IDAC output voltage rises too close to AVDD, the IDAC loses compliance and the excitation current is reduced.

The reference resistor, R_{REF} must be a precision resistor with high accuracy and low drift. Any error in the R_{REF} reflects the same error in the RTD measurement. The REFP0 and REFN0 pins are shown connecting to the R_{REF} resistor as a Kelvin connection to get the best measurement of the reference voltage. This eliminates any series resistance as an error from the reference resistance measurement.

2.6.4 Measurement Conversion

$$\text{Output code} = 2^{23} \cdot \text{Gain} \cdot V_{RTD} / V_{REF} = 2^{23} \cdot \text{Gain} \cdot (I_{IDAC1} \cdot R_{RTD}) / (I_{IDAC1} \cdot R_{REF}) = 2^{23} \cdot \text{Gain} \cdot R_{RTD} / R_{REF} \quad (67)$$

$$R_{RTD} = R_{REF} \cdot \text{Output code} / (2^{23} \cdot \text{Gain}) \quad (68)$$

2.6.5 Configuration Register Settings

For the measurement, set the register values:

- Select multiplexer settings for AINP and AINN to measure leads 2 and 3 of the RTD
- Enable the PGA, set gain to desired value
- Select data rate and digital filter settings
- Select reference input to measure R_{REF} for ratiometric measurement
- Enable the internal reference (the IDAC requires an enabled internal reference)
- Set IDAC magnitude and select IDAC1 output pin to drive lead 1 of the RTD

2.7 Two Series Two-Wire RTD Measurements, Low-Side Reference

A single IDAC may drive multiple RTDs at the same time. In this schematic, two two-wire RTDs are stacked on top of each other for measurement through different inputs of the ADC multiplexer.

2.7.1 Schematic

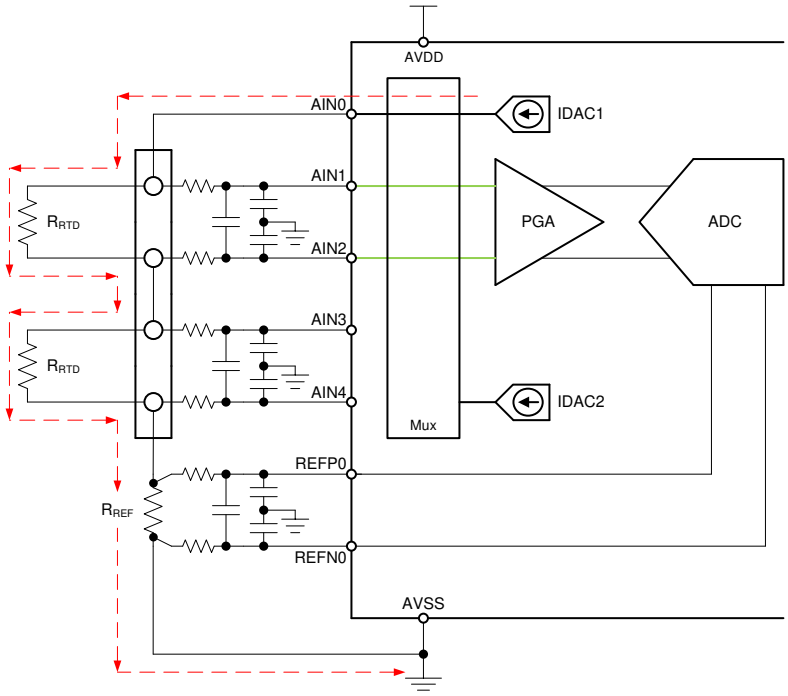

Figure 2-7. Two Series Two-Wire RTD, Low-Side Reference Measurement Circuit

2.7.2 Pros and Cons

Pros:

- Single IDAC current is used for multiple sensors at the same time
- Ratiometric measurement, IDAC noise and drift are cancelled

Cons:

- Stacking sensors may impact IDAC voltage compliance and PGA input range

2.7.3 Design Notes

This circuit should be similar to the two-wire design in Section 2.1. However, measurement of two stacked RTDs requires two calculations to verify the input range of the PGA and has a larger resistive stack for the compliance voltage for the IDAC current. A single IDAC current source drives both RTDs and the reference resistor, R_{REF}.

The measurement circuit requires:

- Single dedicated IDAC output pin
- AINP and AINN inputs for two different RTD measurements
- External reference input
- Precision reference resistor

Then, verify that V_{AIN1} and V_{AIN2}, and V_{AIN3} and V_{AIN4} are in the input range of the PGA. Calculate the voltages for AIN1 and AIN2 and then AIN3 and AIN4 at the maximum differential input voltages. For the first measurement:

$$V_{AIN1} = I_{IDAC1} \cdot (R_{RTD1} + R_{RTD2} + R_{REF}) \quad (69)$$

$$V_{AIN2} = I_{IDAC1} \cdot (R_{RTD2} + R_{REF}) \quad (70)$$

Then for the second measurement:

$$V_{AIN3} = I_{IDAC1} \cdot (R_{RTD2} + R_{REF}) \quad (71)$$

$$V_{AIN4} = I_{IDAC1} \cdot R_{REF} \quad (72)$$

Additionally, verify that the voltage seen at the IDAC pin (where $V_{AIN0} = V_{AIN1}$) is within the current source compliance voltage. When the IDAC output voltage rises too close to AVDD, the IDAC loses compliance and the current is reduced.

2.7.4 Measurement Conversion

For each RTD measurement:

$$\text{Output Code} = 2^{23} \cdot \text{Gain} \cdot V_{RTD} / V_{REF} = 2^{23} \cdot \text{Gain} \cdot I_{IDAC1} \cdot R_{RTD} / (I_{IDAC1} \cdot R_{REF}) = 2^{23} \cdot \text{Gain} \cdot R_{RTD} / R_{REF} \quad (73)$$

$$R_{RTD} = R_{REF} \cdot \text{Output code} / (2^{23} \cdot \text{Gain}) \quad (74)$$

2.7.5 Configuration Register Settings

For the first RTD measurement, set the register values:

- Select multiplexer settings for AINP and AINN to measure leads 1 and 2 of the first RTD
- Enable the PGA, set gain to desired value
- Select data rate and digital filter settings
- Select reference input to measure R_{REF} for ratiometric measurement
- Enable the internal reference (the IDAC requires an enabled internal reference)
- Set IDAC magnitude and select IDAC1 output pin to drive lead 1 of the RTD

For the second RTD measurement, set the register values:

- Select multiplexer settings for AINP and AINN to measure leads 1 and 2 of the second RTD

2.8 Two Series Four-Wire RTD Measurements

Similar to the two two-wire RTD measurement example circuit, a single IDAC may drive multiple four-wire RTDs at the same time. Two four-wire RTDs are set up for measurement by stacking them and measuring them through different inputs of the multiplexer.

2.8.1 Schematic

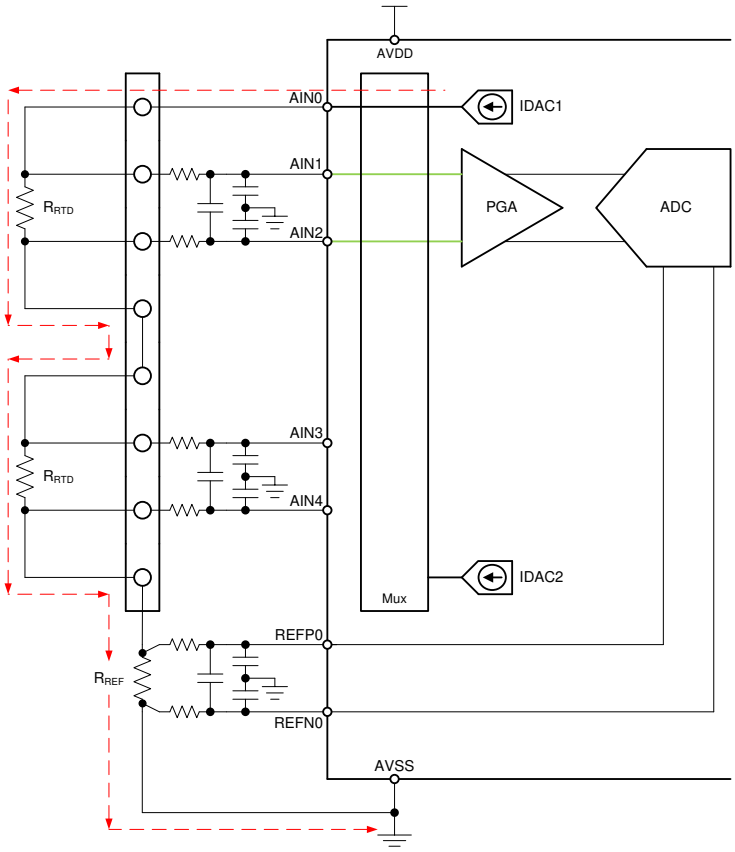

Figure 2-8. Two Series Four-Wire RTD, Low-Side Reference Measurement Circuit

2.8.2 Pros and Cons

Pros:

- Single IDAC current is used for multiple sensors at the same time
- Ratiometric measurement, IDAC noise and drift are cancelled

Cons:

- Stacking sensors may impact IDAC voltage compliance and PGA input range

2.8.3 Design Notes

Design considerations should be exactly the same as the two series, two-wire RTD design in Section 2.7

The measurement circuit requires:

- Single dedicated IDAC output pin
- AINP and AINN inputs for two different RTD measurements
- External reference input
- Precision reference resistor

Then, verify that V_{AIN1} and V_{AIN2}, and V_{AIN3} and V_{AIN4} are in the input range of the PGA. Calculate the voltages for AIN1 and AIN2 and then AIN3 and AIN4 at the maximum differential input voltages. For the first measurement:

$$V_{AIN1} = I_{IDAC1} \cdot (R_{RTD1} + R_{RTD2} + R_{REF}) \quad (75)$$

$$V_{AIN2} = I_{IDAC1} \cdot (R_{RTD2} + R_{REF}) \quad (76)$$

Then for the second measurement:

$$V_{AIN3} = I_{IDAC1} \cdot (R_{RTD2} + R_{REF}) \quad (77)$$

$$V_{AIN4} = I_{IDAC1} \cdot R_{REF} \quad (78)$$

Additionally, verify that the voltage seen at the IDAC pin (where $V_{AIN0} = V_{AIN1}$) is within the current source compliance voltage. When the IDAC output voltage rises too close to AVDD, the IDAC loses compliance and the excitation current is reduced.

2.8.4 Measurement Conversion

For each RTD measurement:

$$\text{Output Code} = 2^{23} \cdot \text{Gain} \cdot V_{RTD} / V_{REF} = 2^{23} \cdot \text{Gain} \cdot I_{IDAC1} \cdot R_{RTD} / (I_{IDAC1} \cdot R_{REF}) = 2^{23} \cdot \text{Gain} \cdot R_{RTD} / R_{REF} \quad (79)$$

$$R_{RTD} = R_{REF} \cdot \text{Output code} / (2^{23} \cdot \text{Gain}) \quad (80)$$

2.8.5 Configuration Measurement Settings

For the first RTD measurement, set the register values:

- Select multiplexer settings for AINP and AINN to measure leads 2 and 3 of the first RTD
- Enable the PGA, set gain to desired value
- Select data rate and digital filter settings
- Select reference input to measure R_{REF} for ratiometric measurement
- Enable the internal reference (the IDAC requires an enabled internal reference)
- Set IDAC magnitude and select IDAC1 output pin to drive lead 1 of the first RTD

For the second RTD measurement, set the register values:

- Select multiplexer settings for AINP and AINN to measure leads 2 and 3 of the second RTD

2.9 Multiple Two-Wire RTD Measurements

Using the multiplexer of the ADC, multiple two-wire RTDs can be measured by changing the output of the IDAC current source.

2.9.1 Schematic

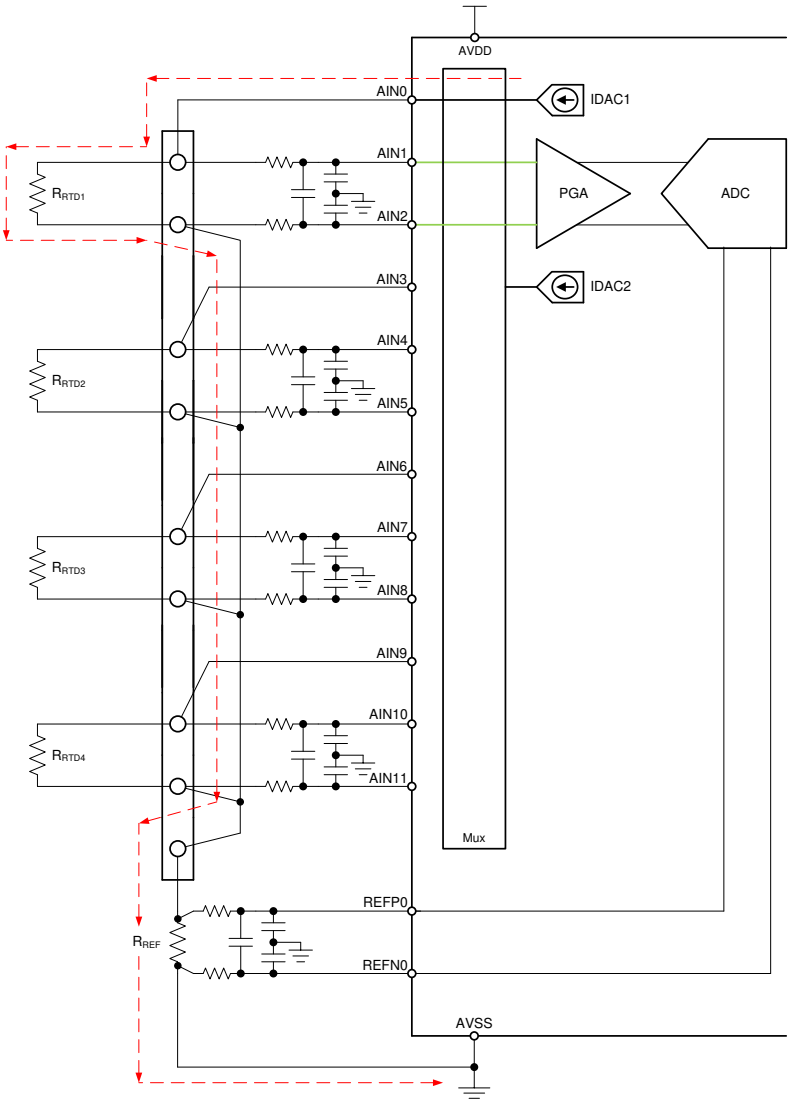

Figure 2-9. Multiple Two-Wire RTDs Measurement Circuit

2.9.2 Pros and Cons

Pros:

- Single IDAC current is used for multiple sensors
- Ratiometric measurement, IDAC noise and drift are cancelled

Cons:

- Requires cycling of IDAC and measurement from channel to channel
- Extra settling time may be required to settle the input RC filtering for inputs and reference

2.9.3 Design Notes

Figure 2-9 shows a circuit topology measuring four two-wire RTDs. To make four measurements, IDAC1 is routed to each of the RTDs separately for each measurement. At the negative input, all RTDs are joined together so that the IDAC1 current is shunted to a common reference resistor.

The measurement circuit requires:

- A single dedicated IDAC output pin and AINP and AINN inputs for each RTD measurement
- External reference input
- Precision reference resistor

The multiplexer isolates each RTD measurement. First IDAC1 is routed to AIN0 for the RTD1 measurement between AIN1 and AIN2. Aside from a small amount of input leakage current for each analog pin, the connections to RTD2, RTD3, and RTD4 should have no bearing on the RTD1 measurement.

After measuring RTD1, IDAC1 is then routed to AIN3 to measure RTD2 between AIN4 and AIN5. This continues by routing IDAC1 to AIN6 for measuring RTD3, and by routing IDAC1 to AIN9 for measuring RTD4. Each RTD measurement requires three pins from the device. One pin sources the IDAC current to provide the excitation, while the other two pins are the analog inputs used to measure the RTDs. The design is identical to the two-wire RTD design in Section 2.1 outlined earlier.

Cycling from channel-to-channel, may require some delay to account for settling as the IDAC1 is routed to different RTDs. Even if the IDAC change is instantaneous, the current is routed from AIN0, to AIN3, to AIN6, and to AIN9. This requires that the voltages from the RTDs settle through the input RC filter at the front end of the ADC. For most devices, this additional delay must be programmed in from the SPI master. For some devices, a built-in programmable delay can be used to insert a small time period to allow for input settling.

2.9.4 Measurement Conversion

$$\text{Output Code} = 2^{23} \cdot \text{Gain} \cdot V_{RTD} / V_{REF} = 2^{23} \cdot \text{Gain} \cdot I_{IDAC1} \cdot R_{RTD} / (I_{IDAC1} \cdot R_{REF}) = 2^{23} \cdot \text{Gain} \cdot R_{RTD} / R_{REF} \quad (81)$$

$$R_{RTD} = R_{REF} \cdot \text{Output Code} / (2^{23} \cdot \text{Gain}) \quad (82)$$

2.9.5 Configuration Register Settings

For the first RTD measurement, set the register values:

- Select multiplexer settings for AINP and AINN to measure leads 1 and 2 of the first RTD
- Enable the PGA, set gain to desired value
- Select data rate and digital filter settings
- Select reference input to measure R_{REF} for ratiometric measurement
- Enable the internal reference (the IDAC requires an enabled internal reference)
- Set IDAC magnitude and select IDAC1 output pin to drive lead 1 of the first RTD

For the second RTD measurement, set the register values:

- Select multiplexer settings for AINP and AINN to measure leads 1 and 2 of the second RTD
- Set IDAC magnitude and select IDAC1 output pin to drive lead 1 of the second RTD

For the third RTD measurement, set the register values:

- Select multiplexer settings for AINP and AINN to measure leads 1 and 2 of the third RTD
- Set IDAC magnitude and select IDAC1 output pin to drive lead 1 of the third RTD

For the fourth RTD measurement, set the register values:

- Select multiplexer settings for AINP and AINN to measure leads 1 and 2 of the fourth RTD
- Set IDAC magnitude and select IDAC1 output pin to drive lead 1 of the fourth RTD

2.10 Multiple Three-Wire RTD Measurements

Using the multiplexer of the ADC, multiple three-wire RTDs can be measured with a change in configuration. This circuit shows the topology of three three-wire RTDs measured using matched IDAC current sources.

2.10.1 Schematic

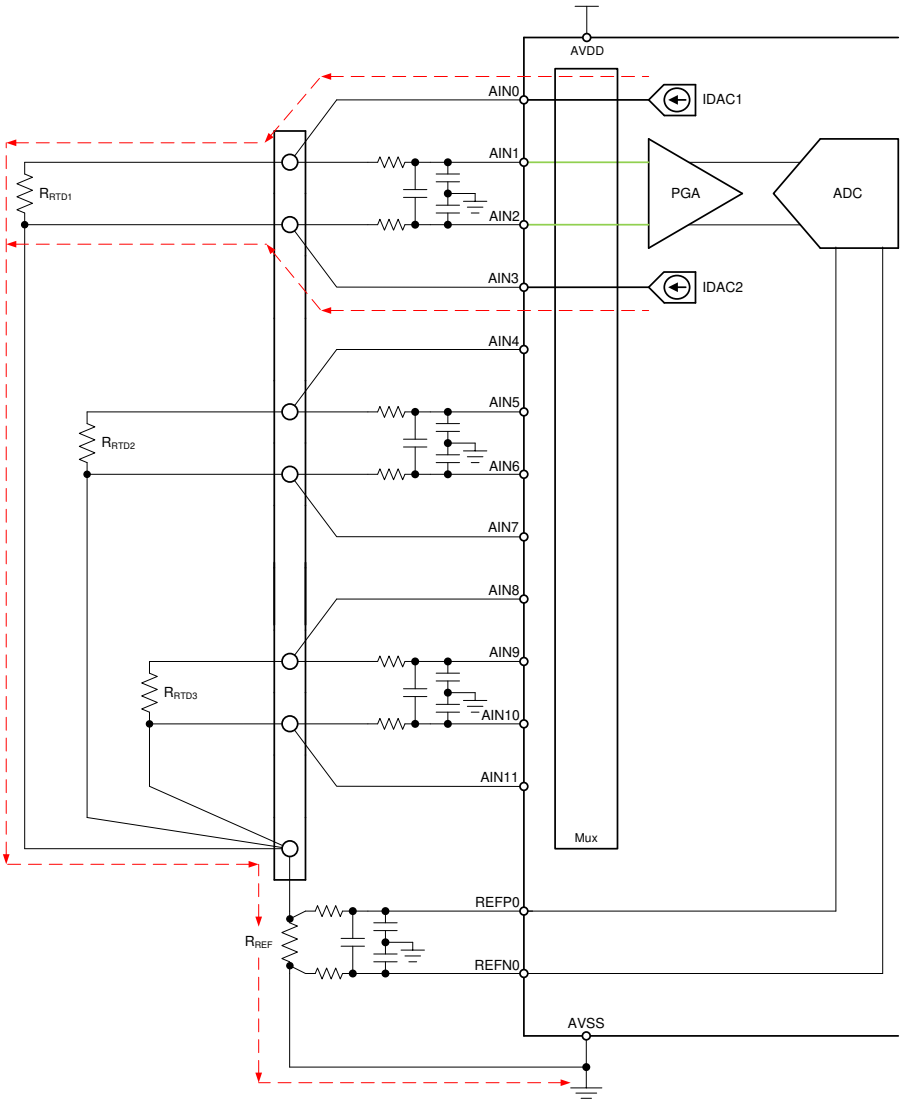

Figure 2-10. Multiple Three-Wire RTDs Measurement Circuit

2.10.2 Pros and Cons

Pros:

- Better accuracy than similar two-wire measurement
- Ratiometric measurement, IDAC noise and drift are cancelled

Cons:

- Requires cycling of IDAC and measurement from channel to channel
- Extra settling time may be required to settle the input RC filtering for inputs and reference

2.10.3 Design Notes

Figure 2-10 shows a circuit topology measuring three three-wire RTDs. For each RTD, IDAC1 is used to drive lead 1 of the RTD, while IDAC2 is used to drive lead 2 of the RTD, used for lead wire compensation. All RTDs are joined together at lead 3 so that the IDAC currents are shunted to a common reference resistor.

The measurement circuit requires:

- Two dedicated IDAC output pins and AINP and AINN inputs for each RTD measurement
- External reference input
- Precision reference resistor

The multiplexer isolates each RTD measurement. First IDAC1 is routed to AIN0 and IDAC2 is routed to AIN3 for the RTD1 measurement between AIN1 and AIN2. Aside from a small amount of input current for each analog pin, the connections to RTD2, RTD3, and RTD4 should have no bearing on the RTD1 measurement.

After measuring RTD1, IDAC1 is then routed to AIN4 and IDAC2 is routed to AIN7 to measure RTD2 between AIN5 and AIN6. Finally, IDAC1 is then routed to AIN8 and IDAC2 is routed to AIN11 to measure RTD2 between AIN9 and AIN10. Each RTD measurement requires four pins from the device. Two pins source the IDAC current for lead wire compensation, while the other two pins are the analog inputs used to measure the RTDs. The design is identical to the three-wire RTD measurement design in Section 2.3 outlined earlier.

Cycling from channel-to-channel, may require some delay to account for settling as the IDAC1 is routed to different RTDs. Even if the IDAC change is instantaneous, the IDAC currents are routed from AIN0 and AIN3, to AIN4 and AIN7, and to AIN8 and AIN11. This requires that the voltages from the RTDs settle through the input RC filter at the front end of the ADC. For most devices, this must be programmed in from the SPI master. For some devices, a built-in programmable delay can be used to insert a small time period to allow for input settling.

As mentioned in Section 2.3.6, chopping of the IDAC currents may be used to reduce the error associated with IDAC mismatch.

2.10.4 Measurement Conversion

$$\text{Output Code} = 2^{23} \cdot \text{Gain} \cdot V_{RTD} / V_{REF} = 2^{23} \cdot \text{Gain} \cdot I_{IDAC} \cdot R_{RTD} / (2 \cdot I_{IDAC} \cdot R_{REF}) = 2^{22} \cdot \text{Gain} \cdot R_{RTD} / R_{REF} \quad (83)$$

$$R_{RTD} = R_{REF} \cdot \text{Output code} / (2^{22} \cdot \text{Gain}) \quad (84)$$

2.10.5 Configuration Register Settings

For the first RTD measurement:

- Select multiplexer settings for AINP and AINN to measure leads 1 and 2 of the first RTD
- Enable the PGA, set gain to desired value
- Select data rate and digital filter settings
- Select reference input to measure R_{REF} for ratiometric measurement
- Enable the internal reference (the IDAC requires an enabled internal reference)
- Set IDAC magnitude and select IDAC1 output pin to drive lead 1 of the RTD and select IDAC2 output pin to drive lead 2 of the RTD

For the second RTD measurement:

- Select multiplexer settings for AINP and AINN to measure leads 1 and 2 of the second RTD
- Set IDAC magnitude and select IDAC1 output pin to drive lead 1 of the RTD and select IDAC2 output pin to drive lead 2 of the second RTD

For the third RTD measurement:

- Select multiplexer settings for AINP and AINN to measure leads 1 and 2 of the third RTD
- Set IDAC magnitude and select IDAC1 output pin to drive lead 1 of the RTD and select IDAC2 output pin to drive lead 2 of the third RTD

2.11 Multiple Four-Wire RTD Measurements in Parallel

Using the multiplexer of the ADC, multiple four-wire RTDs can be measured with a change in configuration.

2.11.1 Schematic

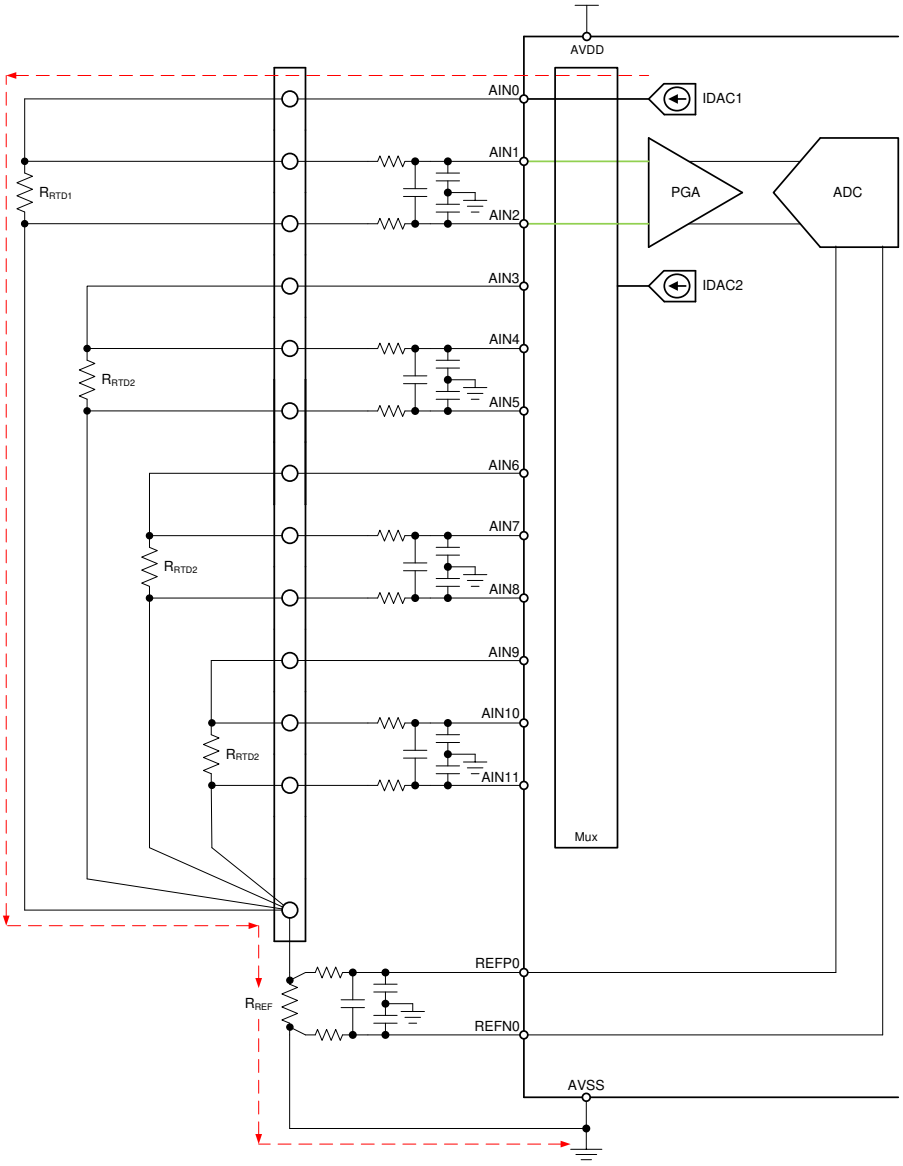

Figure 2-11. Multiple Paralleled Four-Wire RTDs Measurement Circuit

2.11.2 Pros and Cons

Pros:

- Best accuracy of RTD measurement
- Ratiometric measurement, IDAC noise and drift are cancelled

Cons:

- Requires cycling of IDAC and measurement from channel to channel
- Extra settling time may be required to settle the input RC filtering for inputs and reference

2.11.3 Design Notes

Figure 2-11 shows a circuit topology measuring four four-wire RTDs. To make four measurements, IDAC1 is routed to lead 1 of each RTD individually for the measurement. The analog inputs are connected to leads 2 and

3 of each RTD. All RTDs are joined together through lead 4, so that the IDAC1 current is shunted to a common reference resistor.

The measurement circuit requires:

- A single dedicated IDAC output pin and AINP and AINN inputs for each RTD measurement
- External reference input
- Precision reference resistor

The multiplexer isolates each RTD measurement. First IDAC1 is routed to AIN0 for the RTD1 measurement between AIN1 and AIN2. Aside from a small amount of input leakage current for each analog pin, the connections to RTD2, RTD3, and RTD4 should have no bearing on the RTD1 measurement.

After measuring RTD1, IDAC1 is then routed to AIN3 to measure RTD2 between AIN4 and AIN5. This continues by routing IDAC1 to AIN6 for measuring RTD3, and by routing IDAC1 to AIN9 for measuring RTD4. Each RTD measurement requires three pins from the device. One pin sources the IDAC current to provide the excitation, while the other two pins are the analog inputs used to measure the RTD. Notice that the topology is similar to that shown in the four-wire RTD design in Section 2.6, with the exception that the IDAC current is brought out to the connection of lead 1 of each RTD, separated from the measurement leads.

Cycling from channel-to-channel, may require some delay to account for settling as the IDAC1 is routed to different RTDs. Even if the IDAC change is instantaneous, the current is routed from AIN0, to AIN3, to AIN6, and to AIN9. This requires that the voltages from the RTDs settle through the input RC filter at the front end of the ADC. For most devices, this must be programmed in from the SPI master. For some devices, a built-in programmable delay can be used to insert a small time period to allow for input settling.

2.11.4 Measurement Conversion

$$\text{Output Code} = 2^{23} \cdot \text{Gain} \cdot V_{RTD} / V_{REF} = 2^{23} \cdot \text{Gain} \cdot I_{IDAC1} \cdot R_{RTD} / (I_{IDAC1} \cdot R_{REF}) = 2^{23} \cdot \text{Gain} \cdot R_{RTD} / R_{REF} \quad (85)$$

$$R_{RTD} = R_{REF} \cdot \text{Output Code} / (2^{23} \cdot \text{Gain}) \quad (86)$$

2.11.5 Configuration Register Settings

For the first RTD measurement, set the register values:

- Select multiplexer settings for AINP and AINN to measure leads 2 and 3 of the first RTD
- Enable the PGA, set gain to desired value
- Select data rate and digital filter settings
- Select reference input to measure R_{REF} for ratiometric measurement
- Enable the internal reference (the IDAC requires an enabled internal reference)
- Set IDAC magnitude and select IDAC1 output pin to drive lead 1 of the first RTD

For the second RTD measurement, set the register values:

- Select multiplexer settings for AINP and AINN to measure leads 2 and 3 of the second RTD
- Set IDAC magnitude and select IDAC1 output pin to drive lead 1 of the second RTD

For the third RTD measurement, set the register values:

- Select multiplexer settings for AINP and AINN to measure leads 2 and 3 of the third RTD
- Set IDAC magnitude and select IDAC1 output pin to drive lead 1 of the third RTD

For the fourth RTD measurement, set the register values:

- Select multiplexer settings for AINP and AINN to measure leads 2 and 3 of the fourth RTD
- Set IDAC magnitude and select IDAC1 output pin to drive lead 1 of the fourth RTD

2.12 Universal RTD Measurement Interface With Low-Side Reference

Using the multiplexer, multiple RTD types can be measured with a universal interface connected to the ADC. The ADC configuration must be changed for each type, setting different analog inputs and while using a single IDAC output. With changes to the configuration registers, two-, three-, and four-wire RTDs can all be measured with a four connection interface.

2.12.1 Schematic

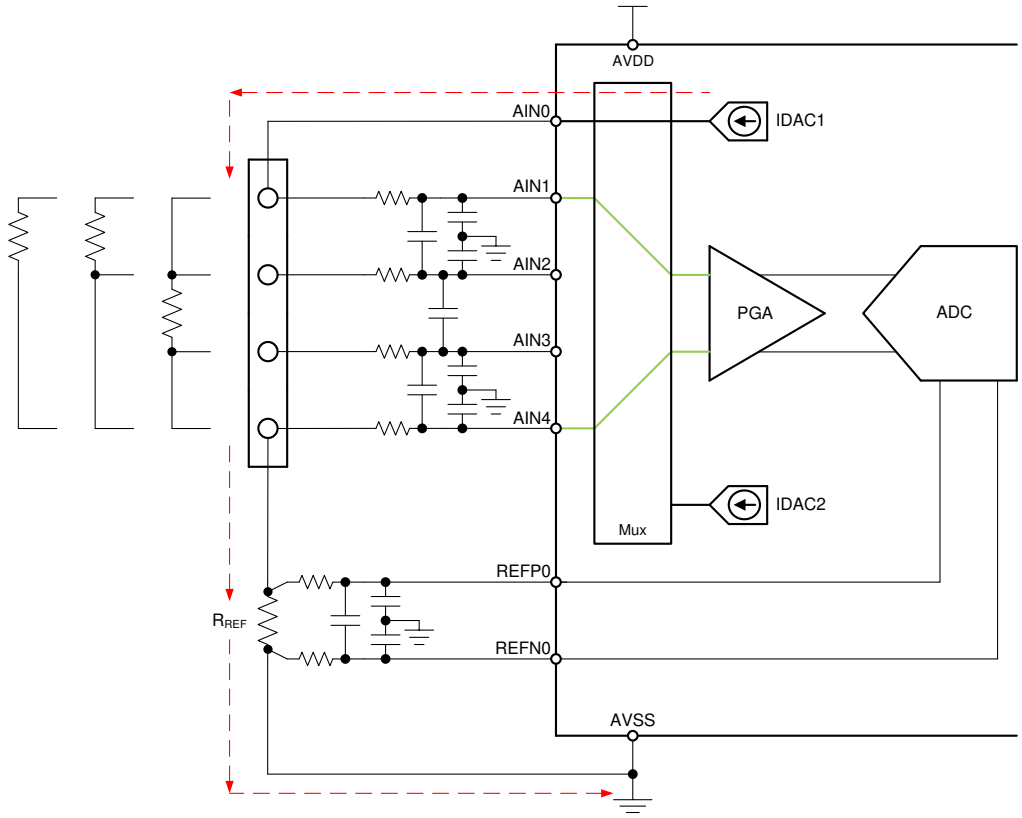

Figure 2-12. Universal RTD Measurement Interface With Low-Side Reference Circuit

2.12.2 Pros and Cons

Pros:

- Set up measurements for two-, three-, and four-wire RTD measurements

Cons:

- Requires multiple inputs for each universal measurement channel
- Requires re-programming the input channel and configuration depending on the type of RTD being measured

2.12.3 Design Notes

Figure 2-12 shows a circuit topology for measuring two-, three- and four-wire RTDs. There are four connections to the RTD header and five connections to the ADC multiplexer. The device is programmed differently depending on which type of RTD is being used.

The measurement circuit requires:

- Single dedicated IDAC output pin and four analog inputs pins for the different RTD configurations
- External reference input
- Precision reference resistor

As a universal connector for different RTD configurations, this design combines several elements from different designs outlined in this application note.

2.12.3.1 Universal Measurement Interface - Two-Wire RTD

The two-wire measurement topology is the same as shown in the two-wire RTD design in Section 2.1. One IDAC sources current from AIN0 into the first RTD connection measured by AIN1. The RTD is measured from AIN1 to AIN4. The IDAC current is then shunted into the reference resistor R_{REF}.

$$V_{AIN1} - V_{AIN4} = I_{IDAC1} \cdot (R_{LEAD1} + R_{RTD} + R_{LEAD2}) \quad (87)$$

As mentioned in previous two-wire RTD measurement designs, the lead resistance of the RTD is an error term that cannot be removed.

2.12.3.2 Universal Measurement Interface - Three-Wire RTD

For the three-wire measurement, the theory is similar to the three-wire RTD design in Section 2.4. As in the previously mentioned design, two measurements are required. A single IDAC current drives the RTD and two lead resistances. One measurement reads the RTD and one lead resistance and a second measurement measures another lead resistance which is then subtracted from the first measurement.

The ADC makes a measurement from AIN1 to AIN2. This results in the voltage across the RTD and one lead resistance.

$$V_{MEAS1} = V_{AIN1} - V_{AIN2} = I_{IDAC1} \cdot (R_{LEAD1} + R_{RTD}) \quad (88)$$

A second measurement is taken from AIN2 to AIN4. This results in the voltage across lead 3.

$$V_{MEAS2} = V_{AIN2} - V_{AIN4} = I_{IDAC} \cdot R_{LEAD3} \quad (89)$$

Assuming that the lead resistances are equal, subtract Equation 89 from Equation 88. There resulting measurement is shown in Equation 90.

$$V_{MEAS1} - V_{MEAS2} = I_{IDAC1} \cdot (R_{LEAD} + R_{RTD}) - I_{IDAC1} \cdot R_{LEAD} = I_{IDAC1} \cdot R_{RTD} \quad (90)$$

2.12.3.3 Universal Measurement Interface - Four-Wire RTD

For the four-wire measurement, the theory is similar to the four-wire design in Section 2.6. The IDAC drives the four-wire RTD through lead 1 and sources the R_{REF} through lead 4 of the RTD. Because the ADC measures the RTD from AIN2 to AIN3, none of the lead resistances with IDAC current are measured.

$$V_{AIN2} - V_{AIN3} = I_{IDAC} \cdot R_{RTD} \quad (91)$$

2.12.4 Measurement Conversion

2.12.4.1 Two-Wire Measurement

$$\text{Output Code} = 2^{23} \cdot \text{Gain} \cdot (V_{RTD} + 2 \cdot V_{LEAD}) / V_{REF} = 2^{23} \cdot \text{Gain} \cdot I_{IDAC1} \cdot (R_{RTD} + 2 \cdot R_{LEAD}) / (I_{IDAC1} \cdot R_{REF}) = 2^{23} \cdot \text{Gain} \cdot (R_{RTD} + 2 \cdot R_{LEAD}) / R_{REF} \quad (92)$$

Ignoring the lead resistance:

$$\text{Output Code} = 2^{23} \cdot \text{Gain} \cdot V_{RTD} / V_{REF} \quad (93)$$

$$R_{RTD} = R_{REF} \cdot \text{Output Code} / (2^{23} \cdot \text{Gain}) \quad (94)$$

2.12.4.2 Three-Wire Measurement

Measure the voltage of $V_{MEAS1} = V_{RTD} + V_{LEAD1}$:

$$\text{Output code 1} = 2^{23} \cdot \text{Gain} \cdot (V_{RTD} + V_{LEAD1}) / V_{REF} = 2^{23} \cdot \text{Gain} \cdot I_{IDAC} \cdot (R_{RTD} + R_{LEAD1}) / (I_{IDAC} \cdot R_{REF}) = 2^{23} \cdot \text{Gain} \cdot (R_{RTD} + R_{LEAD1}) / R_{REF} \quad (95)$$

Measure the voltage of $V_{MEAS2} = V_{LEAD3}$:

$$\text{Output code 2} = 2^{23} \cdot \text{Gain} \cdot V_{LEAD3} / V_{REF} = 2^{23} \cdot \text{Gain} \cdot I_{IDAC} \cdot R_{LEAD3} / (I_{IDAC} \cdot R_{REF}) = 2^{23} \cdot \text{Gain} \cdot R_{LEAD3} / R_{REF} \quad (96)$$

Assuming the lead resistances are equal, subtract V_{MEAS2} from V_{MEAS1} to get the RTD measurement:

$$\text{Output code 1} - \text{Output code 2} = [2^{23} \cdot \text{Gain} \cdot (V_{RTD} + V_{LEAD1}) / V_{REF}] - [2^{23} \cdot \text{Gain} \cdot R_{LEAD3} / R_{REF}] = 2^{23} \cdot \text{Gain} \cdot V_{RTD} / V_{REF} \quad (97)$$

$$R_{RTD} = R_{REF} \cdot (\text{Output code 1} - \text{Output code 2}) / (2^{23} \cdot \text{Gain}) \quad (98)$$

2.12.4.3 Four-Wire Measurement

$$\text{Output Code} = 2^{23} \cdot \text{Gain} \cdot V_{RTD} / V_{REF} = 2^{23} \cdot \text{Gain} \cdot I_{IDAC} \cdot R_{RTD} / (I_{IDAC} \cdot R_{REF}) \quad (99)$$

$$R_{RTD} = R_{REF} \cdot \text{Output Code} / (2^{23} \cdot \text{Gain}) \quad (100)$$

2.12.5 Configuration Register Settings

For the two-wire RTD measurement, set these registers:

- Select multiplexer settings for AINP and AINN to measure leads 1 and 2 of the two-wire RTD
- Enable the PGA, set gain to desired value
- Select data rate and digital filter settings
- Select reference input to measure R_{REF} for ratiometric measurement
- Enable the internal reference (the IDAC requires an enabled internal reference)
- Set IDAC magnitude and select IDAC1 output pin to drive lead 1 of the first RTD

For the three-wire RTD measurement, set these registers:

- For the first measurement, select multiplexer settings for AINP and AINN to measure leads 1 and 2 of the three-wire RTD
- Enable the PGA, set gain to desired value
- Select data rate and digital filter settings
- Select reference input to measure R_{REF} for ratiometric measurement
- Enable the internal reference (the IDAC requires an enabled internal reference)
- Set IDAC magnitude and select IDAC1 output pin to drive lead 1 of the first RTD
- For the second measurement, select the multiplexer settings for AINP and AINN to measure leads 2 and 3 of the three-wire RTD
- Subtract the second measurement from the first measurement

For the four-wire RTD measurement, set these registers:

- Select multiplexer settings for AINP and AINN to measure leads 2 and 3 of the two-wire RTD
- Enable the PGA, set gain to desired value
- Select data rate and digital filter settings
- Select reference input to measure R_{REF} for ratiometric measurement
- Enable the internal reference (the IDAC requires an enabled internal reference)
- Set IDAC magnitude and select IDAC1 output pin to drive lead 1 of the first RTD

2.13 Universal RTD Measurement Interface With High-Side Reference

Similar to the previous design, a universal RTD measurement interface can be constructed with a high-side reference. As shown in previous designs, a bias resistor is required to shift the input voltage up to be in the input range of the PGA.

2.13.1 Schematic

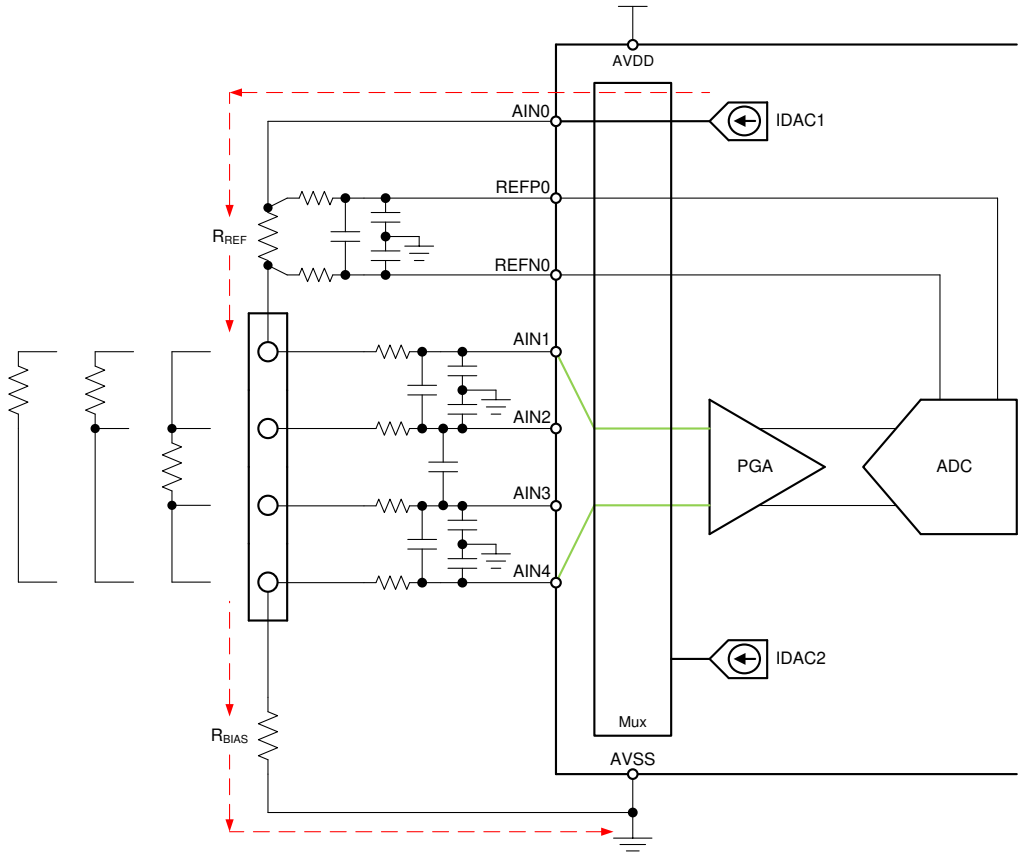

Figure 2-13. Universal RTD Measurement Interface With High-Side Reference Circuit

2.13.2 Pros and Cons

Pros:

- Set up measurements for two-, three-, and four-wire RTD measurements

Cons:

- Requires multiple inputs for each universal measurement channel
- Requires re-programming the input channel and configuration depending on the type of RTD being measured

2.13.3 Design Notes

Figure 2-13 shows a circuit topology for measuring two-, three-, and four-wire RTDs using a high-side reference. There are four connections to the RTD header and five connections to the ADC multiplexer. The device is programmed differently depending on which type of RTD is being used.

The measurement circuit requires:

- Single dedicated IDAC output pin and four analog inputs pins for the different RTD configurations
- External reference input
- Precision reference resistor

The IDAC always sources current from AIN0 into the first RTD connection and RBIAS is used to shift the input voltage level to near mid-supply so that the RTD measurement is in the PGA input range.

2.13.3.1 Universal Measurement Interface, High-Side Reference - Two-Wire RTD

The two-wire measurement topology is the same as shown in the two-wire RTD design in Section 2.2. One IDAC sources current from AIN0 into the reference resistor R_{REF}. Then the current flows into the first RTD connection measured by AIN1. The RTD is attached to and measured from AIN1 to AIN4. The IDAC current is then shunted into the bias resistor R_{BIAS}.

$$V_{AIN1} - V_{AIN4} = I_{IDAC1} \bullet (R_{LEAD1} + R_{RTD} + R_{LEAD2}) \quad (101)$$

For the two-wire RTD measurement, the lead resistance of the RTD is an error term that cannot be removed.

2.13.3.2 Universal Measurement Interface, High-Side Reference - Three-Wire RTD

For the three-wire measurement, the theory is similar to the three-wire design in Section 2.4 except with a high side reference. As in the previously mentioned design, two measurements are required. A single IDAC current drives the RTD and two lead resistances. One measurement reads the RTD and one lead resistance and a second measurement measures another lead resistance which is then subtracted from the first measurement. After the current flows out of the RTD, the current is shunted to ground through R_{BIAS}. The three-wire RTD is attached to the following header connections. Lead 1 is attached to AIN1; lead 2 is attached to AIN2; and lead 3 is attached to AIN4.

The ADC makes a measurement from AIN1 to AIN2. This results in the voltage across the RTD and one lead resistance.

$$V_{MEAS1} = V_{AIN1} - V_{AIN2} = I_{IDAC1} \bullet (R_{LEAD1} + R_{RTD}) \quad (102)$$

A second measurement is taken from AIN2 to AIN4. This results in the voltage across lead 3.

$$V_{MEAS2} = V_{AIN2} - V_{AIN4} = I_{IDAC} \bullet R_{LEAD3} \quad (103)$$

Assuming that the lead resistances are equal, subtract Equation 103 from Equation 102. There resulting measurement is shown in Equation 104.

$$V_{MEAS1} - V_{MEAS2} = I_{IDAC1} \bullet (R_{LEAD} + R_{RTD}) - I_{IDAC1} \bullet R_{LEAD} = I_{IDAC1} \bullet R_{RTD} \quad (104)$$

2.13.3.3 Universal Measurement Interface, High-Side Reference - Four-Wire RTD

For the four-wire measurement, the theory is similar to the two-wire RTD design in Section 2.2, except the four-wire RTD removes the lead resistance from the IDAC current measurement. The IDAC drives the four-wire RTD through lead 1 and sources the R_{REF} through lead 4 of the RTD. Because the ADC measures the RTD from AIN2 to AIN3, none of the lead resistances with IDAC current are measured. IDAC current from lead 4 drives RBIAS which allows for the input voltage level shift so the measurement is in the PGA input range.

$$V_{AIN2} - V_{AIN3} = I_{IDAC} \bullet R_{RTD} \quad (105)$$

2.13.4 Measurement Conversion

2.13.4.1 Two-Wire Measurement

$$\text{Output Code} = 2^{23} \bullet \text{Gain} \bullet (V_{RTD} + 2 \bullet V_{LEAD}) / V_{REF} = 2^{23} \bullet \text{Gain} \bullet I_{IDAC1} \bullet (R_{RTD} + 2 \bullet R_{LEAD}) / (I_{IDAC1} \bullet R_{REF}) = 2^{23} \bullet \text{Gain} \bullet (R_{RTD} + 2 \bullet R_{LEAD}) / R_{REF} \quad (106)$$

Ignoring the lead resistance:

$$\text{Output Code} = 2^{23} \bullet \text{Gain} \bullet R_{RTD} / R_{REF} \quad (107)$$

$$R_{RTD} = R_{REF} \bullet \text{Output Code} / (2^{23} \bullet \text{Gain}) \quad (108)$$

2.13.4.2 Three-Wire Measurement

Measure the voltage of $V_{MEAS1} = V_{RTD} + V_{LEAD1}$:

$$\text{Output code 1} = 2^{23} \bullet \text{Gain} \bullet (V_{RTD} + V_{LEAD1}) / V_{REF} = 2^{23} \bullet \text{Gain} \bullet I_{IDAC} \bullet (R_{RTD} + R_{LEAD1}) / (I_{IDAC} \bullet R_{REF}) = 2^{23} \bullet \text{Gain} \bullet (R_{RTD} + R_{LEAD1}) / R_{REF} \quad (109)$$

Measure the voltage of $V_{MEAS2} = V_{LEAD3}$:

$$\text{Output code 2} = 2^{23} \bullet \text{Gain} \bullet V_{LEAD3} / V_{REF} = 2^{23} \bullet \text{Gain} \bullet I_{IDAC} \bullet R_{LEAD3} / (I_{IDAC} \bullet R_{REF}) = 2^{23} \bullet \text{Gain} \bullet R_{LEAD3} / R_{REF} \quad (110)$$

Assuming the lead resistances are equal, subtract V_{MEAS2} from V_{MEAS1} to get the RTD measurement:

$$\text{Output code 1} - \text{Output code 2} = [2^{23} \bullet \text{Gain} \bullet (V_{RTD} + V_{LEAD1}) / V_{REF}] - (2^{23} \bullet \text{Gain} \bullet R_{LEAD3} / R_{REF}) = 2^{23} \bullet \text{Gain} \bullet V_{RTD} / V_{REF} \quad (111)$$

$$R_{RTD} = R_{REF} \bullet (\text{Output code 1} - \text{Output code 2}) / (2^{23} \bullet \text{Gain}) \quad (112)$$

2.13.4.3 Four-Wire Measurement

$$\text{Output Code} = 2^{23} \bullet \text{Gain} \bullet V_{RTD} / V_{REF} = 2^{23} \bullet \text{Gain} \bullet I_{IDAC} \bullet R_{RTD} / (I_{IDAC} \bullet R_{REF}) \quad (113)$$

$$R_{RTD} = R_{REF} \bullet \text{Output Code} / (2^{23} \bullet \text{Gain}) \quad (114)$$

2.13.5 Configuration Register Settings

For the two-wire RTD measurement, set these registers:

- Select multiplexer settings for AINP and AINN to measure leads 1 and 2 of the two-wire RTD
- Enable the PGA, set gain to desired value
- Select data rate and digital filter settings
- Select reference input to measure R_{REF} for ratiometric measurement
- Enable the internal reference (the IDAC requires an enabled internal reference)
- Set IDAC magnitude and select IDAC1 output pin to drive the reference resistor R_{REF}

For the three-wire RTD measurement, set these registers:

- For the first measurement, select multiplexer settings for AINP and AINN to measure leads 1 and 2 of the three-wire RTD
- Enable the PGA, set gain to desired value
- Select data rate and digital filter settings
- Select reference input to measure R_{REF} for ratiometric measurement
- Enable the internal reference (the IDAC requires an enabled internal reference)
- Set IDAC magnitude and select IDAC1 output pin to drive the reference resistor R_{REF}
- For the second measurement, select the multiplexer settings for AINP and AINN to measure leads 2 and 3 of the three-wire RTD
- Subtract the second measurement from the first measurement

For the four-wire RTD measurement, set these registers:

- Select multiplexer settings for AINP and AINN to measure leads 2 and 3 of the two-wire RTD
- Enable the PGA, set gain to desired value
- Select data rate and digital filter settings
- Select reference input to measure R_{REF} for ratiometric measurement
- Enable the internal reference (the IDAC requires an enabled internal reference)
- Set IDAC magnitude and select IDAC1 output pin to drive the reference resistor R_{REF}

3 Summary

RTDs are temperature sensors that are capable of precision measurements over a large range of temperatures. However, different RTD configurations give different precision and accuracy depending on the circuit topologies. To get the best measurement performance requires attention to the details in the design.

The circuits shown in this application note are a simple guide to how RTD measurements are made with precision ADCs. An overview was presented along with different RTD circuit designs. Circuits using two-, three-, and four-wire RTD measurement circuits are presented. These circuits represent basic topologies, and designs may be altered to fit specific systems and combinations of multiple RTD configurations.

The topologies presented here are a sampling of different RTD measurements. As the designs show, topologies can be combined for systems that measure multiple combinations of RTD wiring configurations. With larger systems measuring multiple elements, these circuits can be combined and altered to fit many different applications.

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (June 2018) to Revision A (March 2023)	Page
• Updated the numbering format for tables, figures and cross-references throughout the document	1

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