Circuit for driving an ADC with an instrumentation amplifier in high gain

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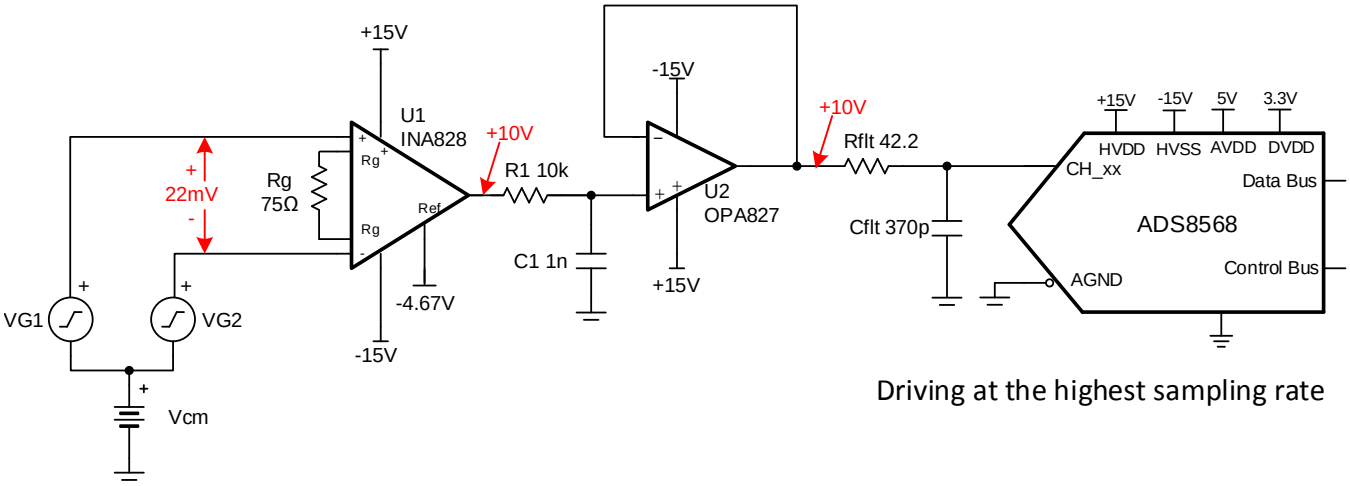
Input	ADC Input	Digital Output ADS8568
VinDiffMin = –8mV	CH_x = –10V	8000H
VinDiffMax = +22mV	CH_x = +10V	7FFFH

Power Supplies			
AVDD		**Vee**	**Vdd**
5.0V	3.3V	+15V	–15V

Design Description

Instrumentation amplifiers are optimized for low noise, low offset, low drift, high CMRR and high accuracy but these instrument amplifiers may not be able to drive a precision ADC to settle the signal properly during the acquisition time of ADC. This design shows an example of how to set the gain and offset shift to amplify a low level asymmetric input signal. Also, the high gain limits the INA828 instrumentation amplifier bandwidth, so an OPA827 op amp is used as a buffer so that the ADS8568 full sampling rate can be achieved. A related cookbook circuit shows a simplified approach that does not include the wide bandwidth buffer (*Driving High Voltage SAR ADC with an Instrumentation Amplifier*), this simplified approach has limited sampling rate as compared to the buffered design in this document. Also *Driving High Voltage SAR ADC with a Buffered Instrumentation Amplifier*, analyzes this design in unity gain. This circuit implementation is applicable to all *Bridge Transducers in PLC's* and *Analog Input Modules* that require precision signal-processing and data-conversion.



Driving at the highest sampling rate

Specifications

Specification	Goal	Calculated	Simulated
Transient Settling Error	>0.5 LSB (152µV)	NA	0.36µV
Noise		1.1mV	1.14mV
System Offset Error		33.6mV	NA
System Offset Drift		334µV/ºC	NA
System Gain Error		0.53%	NA
System Gain Drift		54.2ppm/ºC	NA

Design Notes

1. The bandwidth of instrumentation amplifiers is typically not enough to drive SAR data converters at a higher data rate. This is especially true when the instrumentation amplifier is in high gain. so a wide bandwidth driver is needed because the SAR ADC with switched-capacitor input structure has an input capacitor that needs to be fully charged during each acquisition time. The OPA827 buffer is added to allow the ADC to run at full sampling rate (ADS8568 510kSPS for parallel interface).
2. Check the common-mode range of the amplifier using the *Common-Mode Input Range Calculator for Instrumentation Amplifiers* software tool.
3. Select COG capacitors for C_1 and C_{filt} to minimize distortion.
4. The gain set resistor, R_g, should be a 0.1% 20ppm/°C film resistors or better for low gain error and low gain drift.
5. The *TI Precision Labs* video series covers the method for selecting the driver amplifier and the charge bucket circuit R_{filt} and C_{filt}. See *Introduction of SAR ADC Front-End Component Selection* for details.
6. Set the cutoff of the filter between the op amp and instrumentation amplifier for anti aliasing and to minimize noise. See *Aliasing and Anti-aliasing Filters* for more details on aliasing and anti-aliasing filters.
7. Because of the high instrumentation amplifier gain, the DC errors (offset, gain, and drift) are significant. Calibration is a good approach to minimizing these errors. See *Understanding and Calibrating the Offset and Gain for ADC Systems* for more details on calibration.

Component Selection

1. Find the gain based on differential input signal and the ADS8568 full-scale input range.

$$G = \frac{V_{out} - V_{out}}{V_{in} - V_{in}} = \frac{10V - (-10V)}{22mV - (-8mV)} = 666.7$$

$$R_g = \frac{50k\Omega}{G - 1} = \frac{50k\Omega}{666.7} = 75.1\Omega$$

$$R_g = 75.1\Omega \text{ standard value}$$

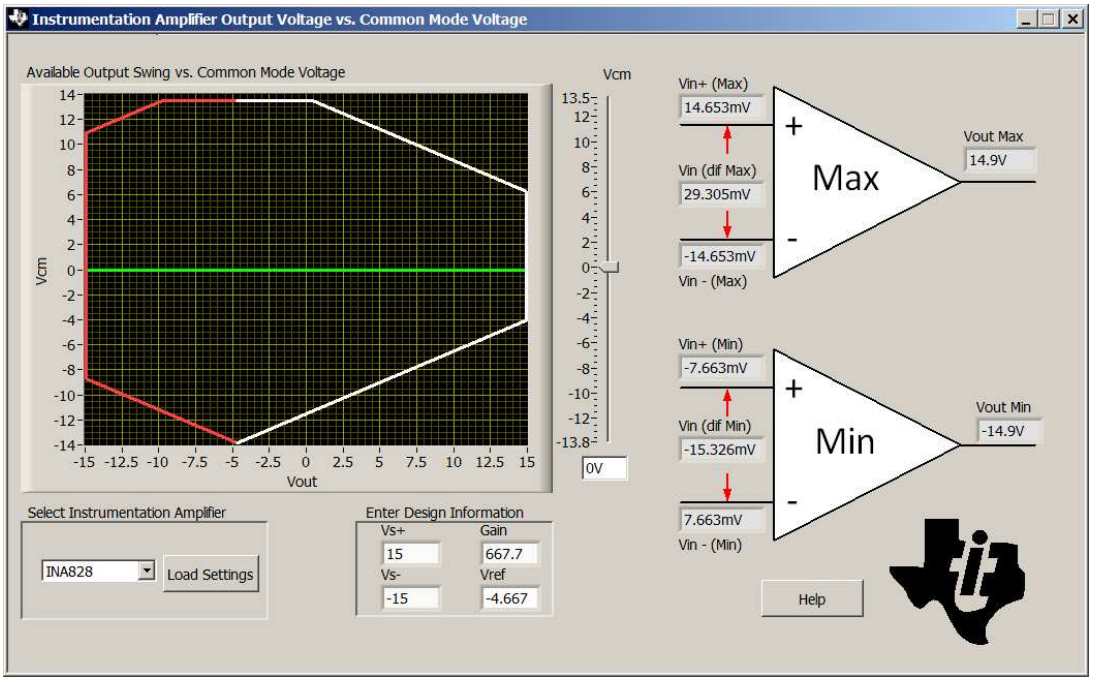
$$G = 1 + \frac{50k\Omega}{R_g} = 667.7$$

2. The input signal in this design is ±10-V high voltage signal, so the gain of INA828 should be set to 1 and no gain resistor (R_g) is needed.

$$V_{out} = G \cdot V_{in} + V_{ref}$$

$$V_{ref} = V_{out} - G \cdot V_{in} = 10V - 667.7 \cdot 22mV = -4.667V$$

3. Use the *Common-Mode Input Range Calculator for Instrumentation Amplifiers* to determine if the INA826 is violating the common-mode range. The common-mode calculator in the following figure indicates that the output swing is ±14.9V for a 0-V common-mode input.

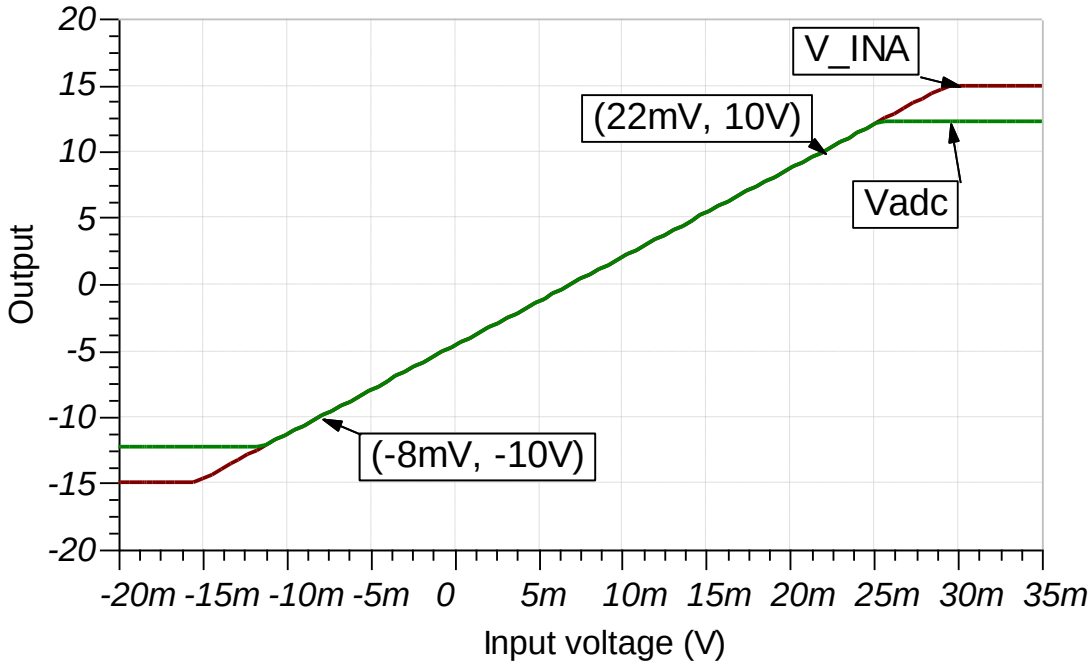


4. Find the value for C_{filt}, and R_{filt} using TINA SPICE and the methods described in *Introduction of SAR ADC Front-End Component Selection* videos. The value of R_{filt} and C_{filt} shown in this document will work for these circuits; however, if you use different amplifiers you will have to use TINA SPICE to find new values.
5. Select the RC filter between the INA828 and OPA827 based on your system requirements (f_{cRC} = 15.9kHz in this example).

$$f_{cRC} = \frac{1}{2\pi \cdot R_1 \cdot C_1} = \frac{1}{2\pi \cdot (10k\Omega) \cdot (1pF)} = 15.9kHz$$

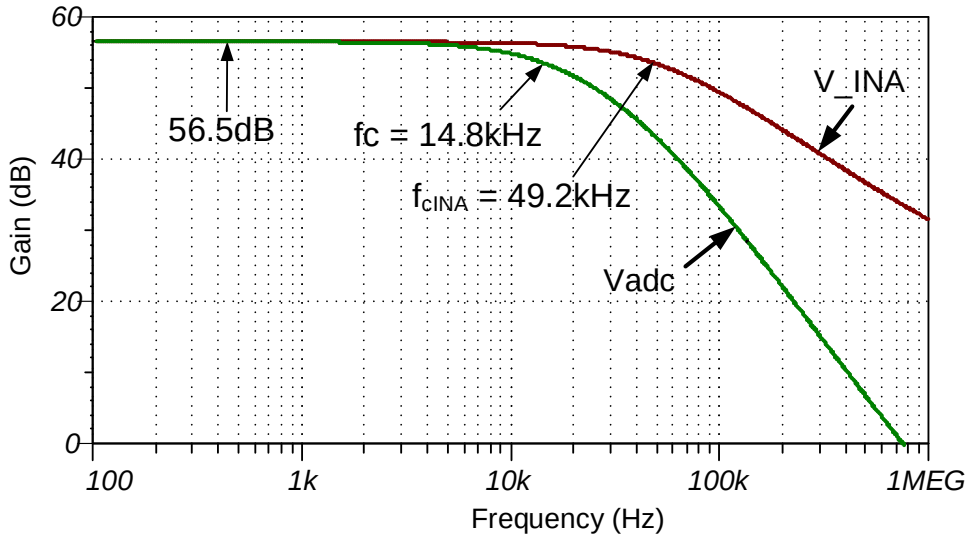
DC Transfer Characteristics

The following graph shows a linear output response for inputs from differential –10V to +10V. See *Determining a SAR ADC's Linear Range when using Instrumentation Amplifiers* for detailed theory on this subject. The full-scale range (FSR) of the ADC falls within the linear range of the Instrumentation Amplifier.



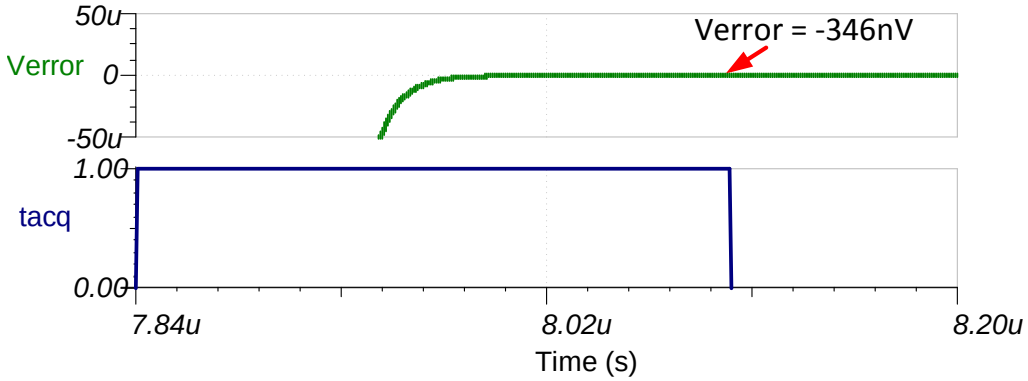
AC Transfer Characteristics

The bandwidth for this design is simulated to be 14.8kHz and the gain is 56.4dB (667.7V/V). The bandwidth limit is set by a combination RC filter (f_{cRC} = 15.9kHz) and the instrumentation amplifier (f_{cINA}=49.2kHz).



Transient ADC Input Settling Simulation (510kSPS)

The OPA827 buffer (22-MHz GBW) is used because it is capable of responding to the rapid transients from the charge kickback of the ADS8568. The op-amp buffer allows the system to achieve the ADS8568 maximum sampling rate of 510kSPS. The following simulation shows settling to a full-scale DC input signal with the INA828 and OPA827 buffer, and ADS8568. This type of simulation shows that the sample and hold kickback circuit is properly selected to meet desired ½ of a LSB (152µV). See *Introduction to SAR ADC Front-End Component Selection* for detailed theory on this subject.



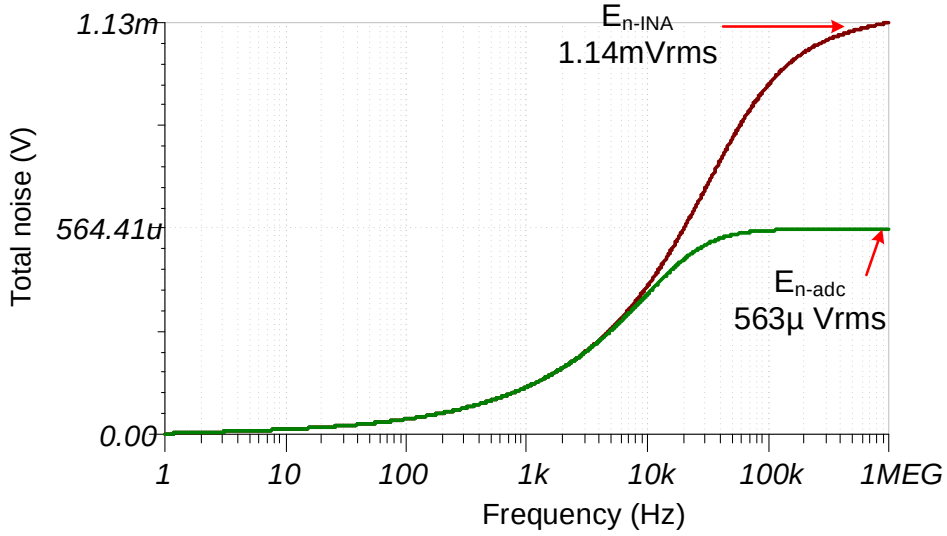
Noise Simulation

The section walks through a simplified noise calculation for a rough estimate. We neglect the noise from the OPA827 as the noise of the INA828 is dominant also neglect resistor noise in this calculation as it is attenuated for frequencies greater than 15.92kHz.

$$E_n = Gain \cdot \sqrt{e_{NI}^2 + \left(\frac{e_{NO}}{Gain}\right)^2} \cdot \sqrt{K_n f_c}$$

$$E_n = 667.7 \cdot \sqrt{\left(7nV/\sqrt{Hz}\right)^2 + \left(\frac{90nV/\sqrt{Hz}}{667.7}\right)^2} \cdot \sqrt{1.57 \cdot 14.8kHz} = 595\mu Vrms$$

Note that calculated and simulated match well (simulated = 563µV_{RMS}, calculated = 595µV_{RMS}). See *TI Precision Labs - Op Amps: Noise 4* for detailed theory on amplifier noise calculations and *Calculating Total Noise for ADC Systems* for data converter noise.



Gain Error and Offset Estimates:

The following offset and offset drift calculations will be dominated by the instrumentation amplifier since it is in high gain. Gain error calculations include the gain error of the ADC and instrumentation amplifier. For offset and gain error, the maximum room temperature value is used. See *Statistics Behind Error Analysis* for details on system gain and offset error.

System Offset Calculation:

$V_{osi} = 50\mu V,\ V_{oso} = 250\mu V$ max at room temp

$G = 667.7V/V$

$$V_{osRTI} = V_{osi} + \frac{V_{oso}}{G} = 50\mu V + \frac{250\mu V}{667.7} = 50.4\mu V$$

$$V_{osRTO} = G \cdot V_{osRTI} = 667.7 \cdot 50.4\mu V = 33.6mV$$

$V_{os(System)} \approx 33.6mV$ total system offset is dominated by INA828 offset

System Offset Drift Calculation:

$V_{osDrift(INA828RTI)} = 0.5\,\mu V/^{o}C$

$V_{osDrift(INA828RTO)} = G \cdot V_{osDriftINA828RTI} = 667.7 \cdot 0.5\,\mu V/^{\circ}C = 334\,\mu V/^{\circ}C$

$V_{osDrift(System)} \approx 334\,\mu V/^{\circ}C$ the INA drift dominates because of the high gain.

System Gain Error Calculation:

$GE_{ina} = \pm 0.15\%$, max room temp INA828

$GE_{Rg} = \pm 0.1\%$, Rg Tolerance

$GE_{ADS8568} = \pm 0.5\%$, max room temp ADS8568

$$GE_{total} = \sqrt{(GE_{ina})^2 + (GE_{Rg})^2 + (GE_{ADS8568})^2} = \sqrt{(0.15\%)^2 + (0.1\%)^2 + (0.5\%)^2} = 0.53\%$$

System Gain Drift Calculation:

$$\frac{\Delta GE_{INA}}{\Delta T} \approx 50ppm/^{\circ}C$$

$$\frac{\Delta GE_{Rg}}{\Delta T} \approx 20ppm/^{\circ}C$$

$$\frac{\Delta GE_{ADC8568}}{\Delta T} \approx 6ppm/^{\circ}C$$

$$\frac{\Delta GE_{System}}{\Delta T} \approx \sqrt{(50ppm/^{\circ}C)^2 + (20ppm/^{\circ}C)^2 + (6ppm/^{\circ}C)^2} = 54.2ppm/^{\circ}C$$

Design Featured Devices

Device	Key Features	Link	Other Possible Devices
ADS8568	16-bit resolution, SPI, 500kSPS sample rate, single-ended input, simultaneous sampling, internal reference, programmable range up to ±12V.	http://www.ti.com/product/ADS8568	http://www.ti.com/adcs
INA828	Bandwidth 1MHz (G=1), low noise 18nV/√Hz, low offset ±40μV, low offset drift ±0.4μV/ºC, low gain drift 0.1ppm/ºC. (Typical values)	http://www.ti.com/product/INA828	http://www.ti.com/inas
OPA827	Gain bandwidth 22MHz, low noise 4nV/√Hz, low offset ±75μV, low offset drift ±0.1μV/ºC (Typical values)	http://www.ti.com/product/OPA827	http://www.ti.com/opamp

Link to Key Files

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Source files for this circuit - http://www.ti.com/lit/zip/SBAC215.

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