SBAA315A–October 2018–Revised November 2018

True differential, 4 × 2 MUX, analog front end, simultaneous-sampling ADC circuit

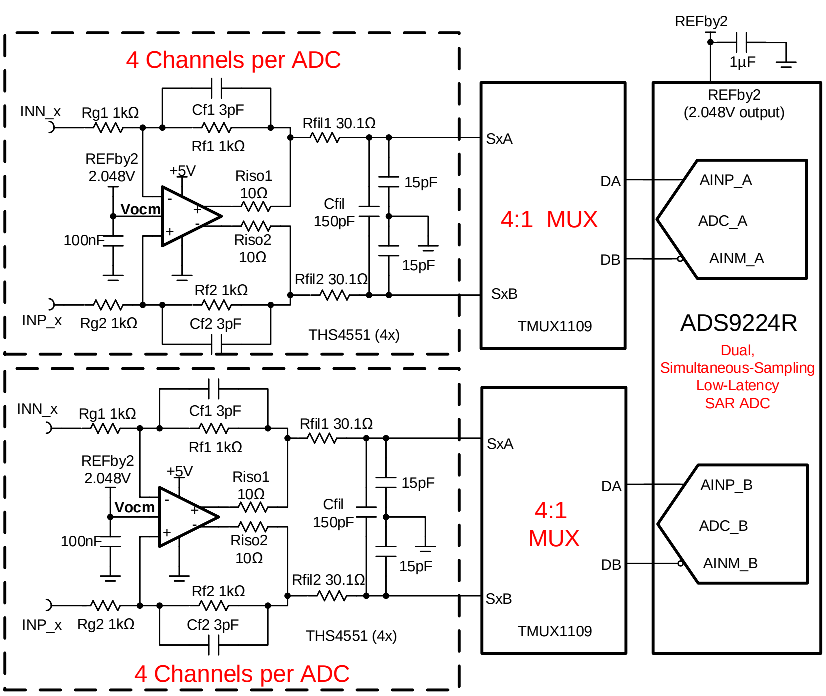
Luis Chioye

Input (THS4551 Inputs)	ADC Input (THS4551 Output)	Digital Output ADS7042
VinP = +0.23V, VinN =+3.866V, VinMin(Dif) = -3.636V	VoutP = +0.23V, VoutN = 3.866V, Vout(Dif) = -3.636V	$8E60_H$ -29088_{10}
VinP = +3.866V, VinN =0.23V, VinMax(Dif) = +3.636V	VoutP = 3.866V, VoutN = +0.23V, Vout(Dif) = +3.636V	$71A0_H$ $+29088_{10}$

Power Supplies			
Vcc	Vee	Vref	Vocm
5	0V	4.096V	2.048V

Design Description

This dual simultaneous-sampling SAR ADC and 4 × 2 channel multiplexed analog front end data acquisition solution can measure differential voltage signals in the range of ±3.866V supporting ADC sampling rates up to 3-MSPS (or effective sampling rate of 750-kSPS per channel) with 16-B resolution. The circuit consists of a dual simultaneous sampling SAR ADC, with each SAR ADC connected to two 4:1 (2x) multiplexers, providing 4 differential input channels per ADC. Eight *Fully Differential Amplifiers* (FDAs) drive the multiplexed SAR ADC inputs. This circuit is applicable in the accurate measurement of dual simultaneous signals in applications such as Optical Modules and Analog Input Modules. It also can be used in motor drive applications such as Servo Drive Control Module, Servo Drive Position Feedback, and Servo Drive Position Sensor.



Specifications

Specification	Goal	Calculated	Simulated
Dual ADC Sampling Speed	3-MSPS	3-MSPS	3-MSPS
Sampling Rate per Channel (dual, simultaneous)	750-kSPS (3-MSPS / 4)	750-kSPS (3-MSPS / 4)	750-kSPS (3-MSPS / 4)
Transient ADC Input Settling	<< 1 LSB << 125 µV	NA	20 µV
Noise (at ADC Input)	$50\mu V_{rms}$	$55.9\mu V_{rms}$	$51.1\mu V_{rms}$

Design Notes

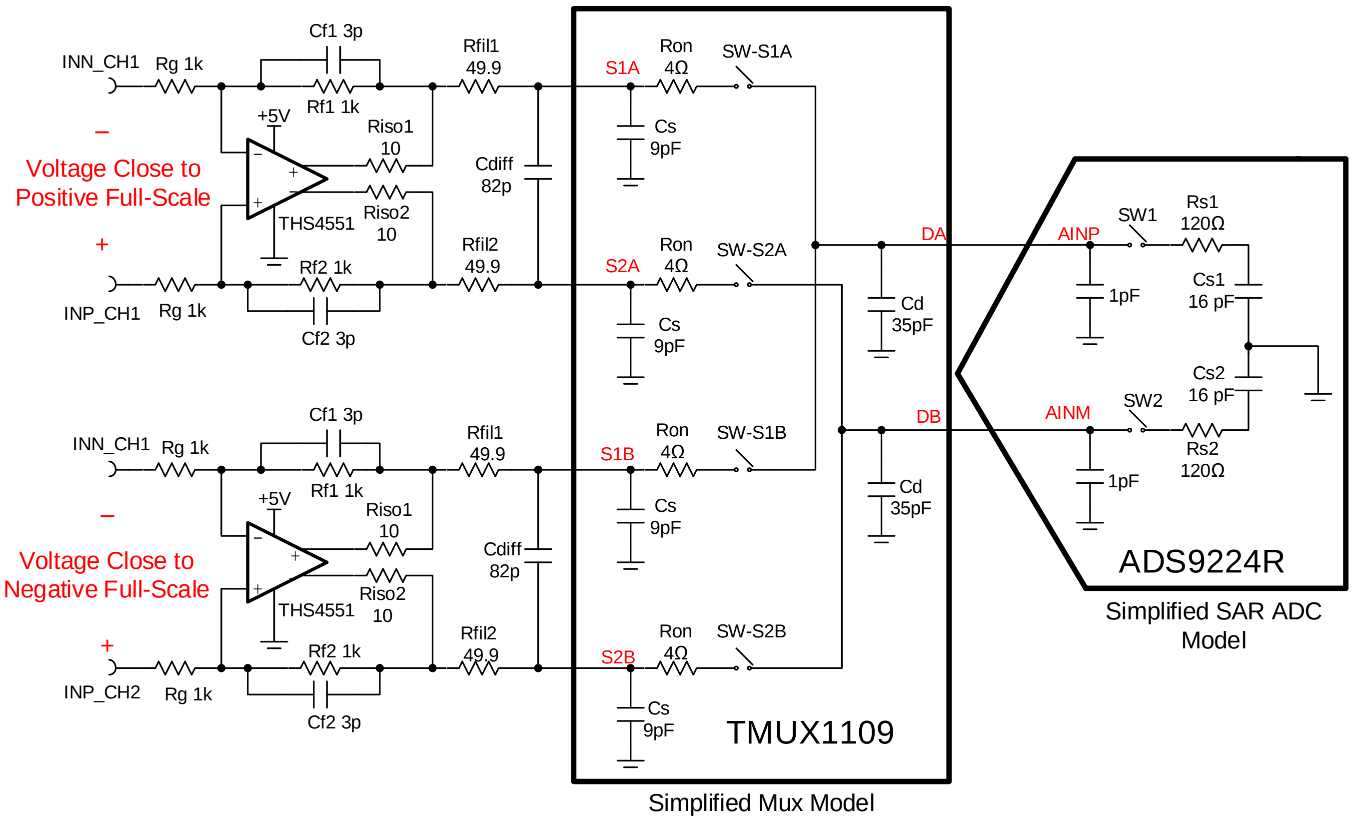
1. The ADS9224R was selected because of the dual simultaneous sampling and high throughput (3-MSPS) requirements.
2. The TMUX1109 4:1 (2x) multiplexer was selected to support 4-channel differential inputs for each ADC.
3. Find ADC full-scale range, resolution and common-mode range specifications. This is covered in the component selection.
4. Determine the linear range of the FDA (THS4551) based on common-mode and output swing specification. This is covered in the component selection section.
5. Select COG capacitors for all filter capacitors at the ADC input to minimize distortion.
6. Select the FDA gain resistors RF1,2 , RG1,2. Use 0.1% 20ppm/°C film resistors or better for good accuracy, low gain drift and to minimize distortion.
7. *Introduction to SAR ADC Front-End Component Selection* covers the methods for selecting the charge bucket circuit Rfil1, Rfil1 and Cfil. These component values are dependent on the amplifier bandwidth, data converter sampling rare, and data converter design. The values shown here will give good settling and AC performance for the amplifier and data converter in this example. If the design is modified, a different RC filter must be selected.
8. The THS4551 is commonly used in high-speed precision fully differential SAR applications as it has sufficient bandwidth to settle to charge kickback transients from the ADC input sampling, and multiplexer charge injection and provides the common-mode level shifting to the voltage range of the SAR ADC.

Component Selection

1. Find ADC full-scale input range. In this circuit, ADS9224 internal V_REF= 2.5V
   $ADC_{Full-Scale\ Range} = \left(\pm 1.6384 V/V\right) \cdot V_{REF} = \pm 4.096V$ from ADS9224R datasheet
2. Find required ADC common-mode voltage 2.
   $V_{CM} = \frac{+ADC_{Full-Scale\ Range}}{2} = +2.048V$ from ADS9224R datasheet
   Use REFby2 Output pin of ADS9224R to connect to FDA (THS4551) VCOM = 2.048V
3. Find FDA absolute output voltage range for linear operation:
   $0.23V < V_{out} < 4.77V$ from THS4551 output low/high specification for linear operation
4. Find FDA differential output voltage range for linear operation. The general output voltage equations for this circuit:
   $$V_{outMin} = \frac{V_{outDifMin}}{2} + V_{cm}$$
   $$V_{outMax} = \frac{V_{outDifMax}}{2} + V_{cm}$$
   Rearrange the equations and solve for $V_{outDifMin}$ and $V_{outDifMax}$. Find maximum differential output voltage range based on worst case:
   $$V_{outDifMax} = 2 \cdot V_{outMax} - 2 \cdot V_{cm} = 2 \cdot (4.096V) - 2 \cdot (2.048V) = 4.096V$$
   $$V_{outDifMin} = 2 \cdot V_{outMin} - 2 \cdot V_{cm} = 2 \cdot (0.23V) - 2 \cdot (2.048V) = -3.636V$$
   Based on combined worst case, choose $V_{outDifMin}$ = -3.636V and $V_{outDifMax}$ = +3.636V
5. Set FDA gain to 1 V/V
   $$Gain_{FDA} = \frac{R_f}{R_g} = \frac{1.00k\Omega}{1.00k\Omega} = 1V/V$$
6. Select the minimum charge kickback capacitor filter to optimize circuit for fastest settling.
   $C_{sh} = 16pF$ internal sample-and-hold capacitor from ADS9224R datasheet
   Select a capacitor 10x larger than $C_{fil} = 150pF$
7. Optimize RC charge kickback filter resistors R_{fil1}, R_{fil2} and feedback capacitors C_{f1}, C_{f2} for both settling and stability using TINA simulations. This is covered in the transient settling optimization and stability simulation sections.

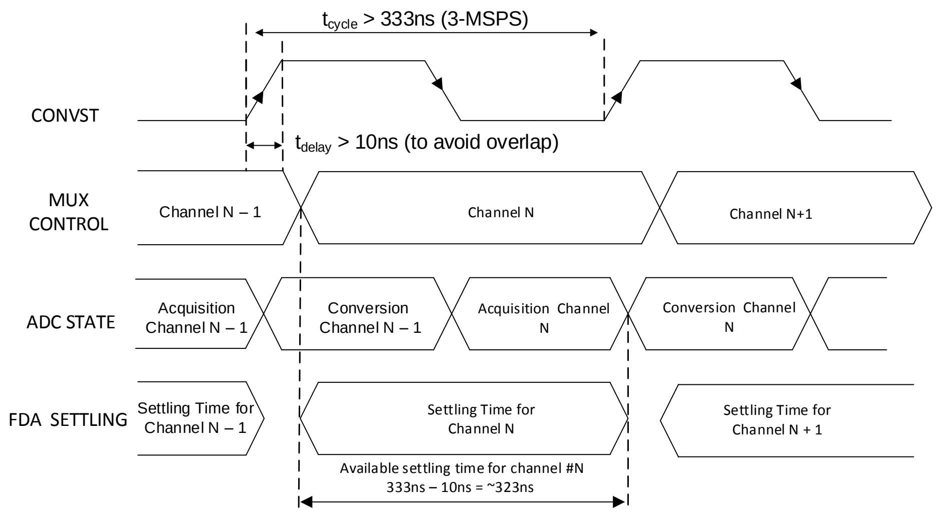
Transient Settling Optimization

TINA simulation is used to optimize the RC kickback filter for stability and transient settling. The transient simulation incorporates two adjacent channels of the multiplexer (TMUX1109). To simulate worst case transient settling during the multiplexer scanning sequence, the two adjacent channels are set to a voltage close to positive full-scale and negative full-scale respectively. The multiplexer drain capacitance and series resistance are modeled in the multiplexer simulation circuit. The sample and hold capacitor of the SAR ADC must settle within the 16-Bit resolution of the SAR ADC during the acquisition period. A simplified schematic of the simulation circuit follows:



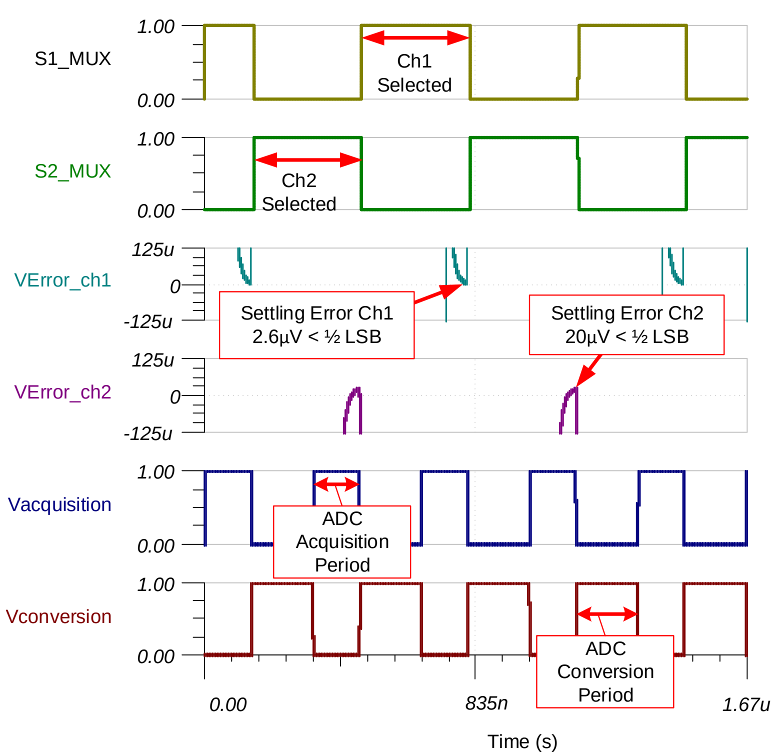
Multiplexer and ADC Control Timing

The following plot shows the ADC conversion control (CONVST) and multiplexer channel control timing. The ADS9224R supports a maximum sampling rate of 3-MSPS or a minimum cycle time of 333ns. To avoid switching channels prior to the rising edge of the CONVST signal, a small delay is implemented in the MUX channel control timing after the CONVST rising edge. Refer to TI design *16-Bit, 400-kSPS, Four-Channel MUX Data Acquisition System for High-Voltage Inputs Reference Design* for detailed theory in the subject.



Transient Settling Results

The following TINA transient simulation shows settling of the FDA, multiplexer, and SAR ADC sample and hold after a full-scale step change between adjacent MUX channels. This type of simulation shows that the sample and hold kickback circuit, and AFE amplifier circuit is properly selected. See *Introduction to SAR ADC Front-end Component Selection* for an explanation of how to select the RC filter for best settling and AC performance.

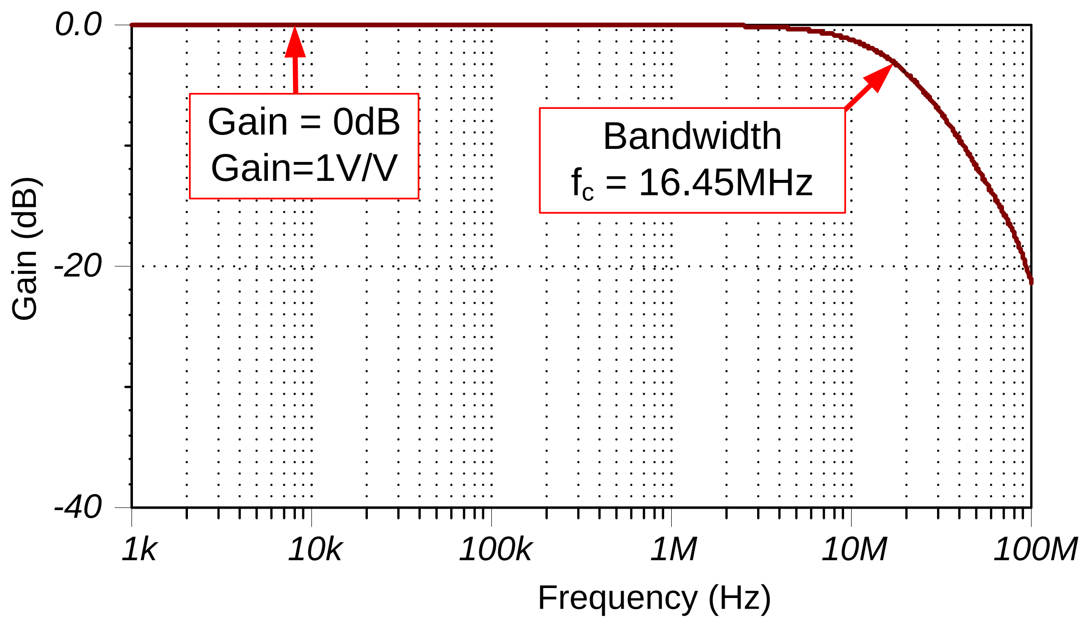


AC Transfer Characteristics

The circuit has a gain of 0-dB (1-V/V) and a simulated frequency bandwidth of 16.45-MHz. Notice that the calculated and simulated bandwidth compare well (calculated = 17.62MHz, simulated = 16.45MHz). See Op Amp Bandwidth for a general overview of bandwidth calculations and simulations.

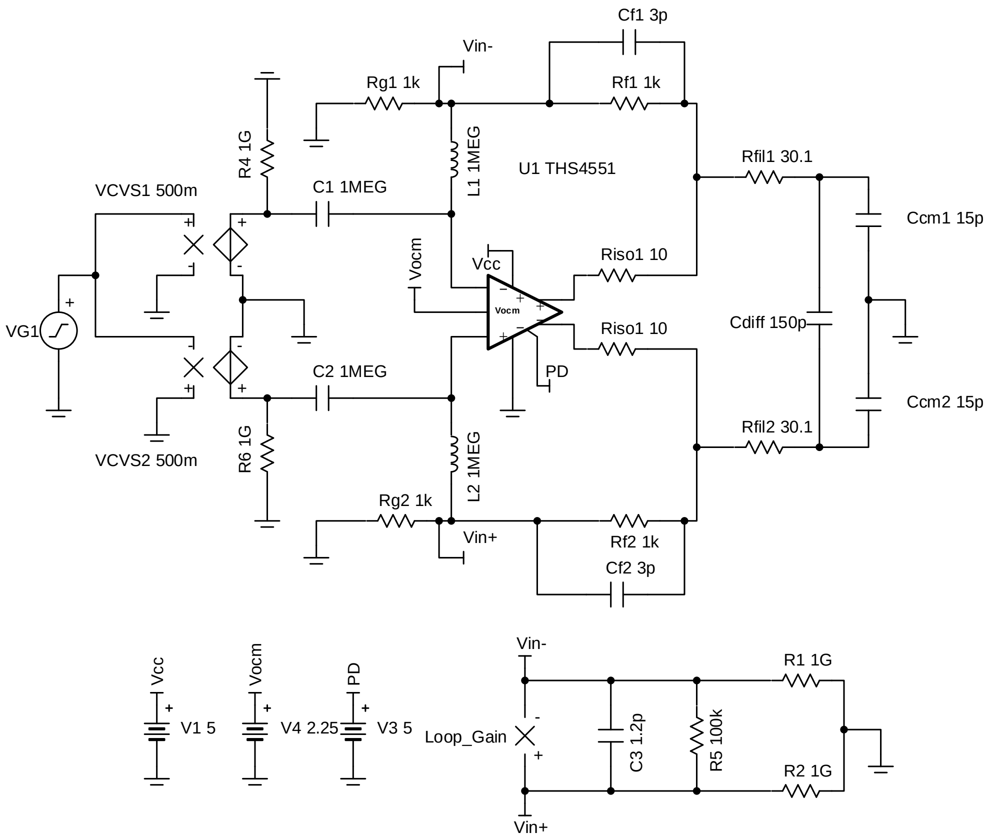
The system bandwidth is set by the output filter:

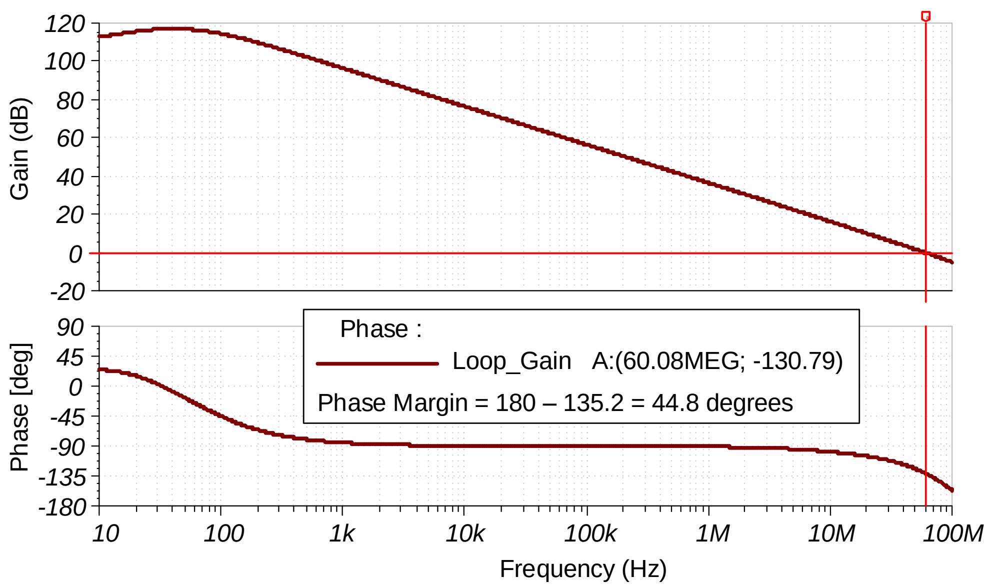
$$f_c = \frac{1}{2\pi(R_{fil1} + R_{fil2})C_{diff}} = \frac{1}{2\pi\left(30.1\Omega + 30.1\Omega\right)\left(150pF\right)} = 17.62MHz$$



Stability Simulation Graph

The following circuit is used in TINA to measure loop gain and verify phase margin using AC analysis in TINA. Resistors RISO = 10Ω are used inside the feedback loop to increase phase margin. The circuit has good stability (approximately 45 degrees of phase margin). See Op Amp Stability for detailed theory on this subject.





Noise Simulation

Simplified noise calculation estimate:

The dominant pole in this data acquisition circuit is in the RC kickback filter:

$$f_c = \frac{1}{2\pi(R_{fil1}+R_{fil2})C_{diff}} = \frac{1}{2\pi\left(30.1\Omega+30.1\Omega\right)\left(150pF\right)} = 17.62MHz$$

Noise of THS4551 FDA referred to ADC input

Noise Gain: $NG = 1 + R_f / R_g = 1 + \frac{1k\Omega}{1k\Omega} = 2V/V$

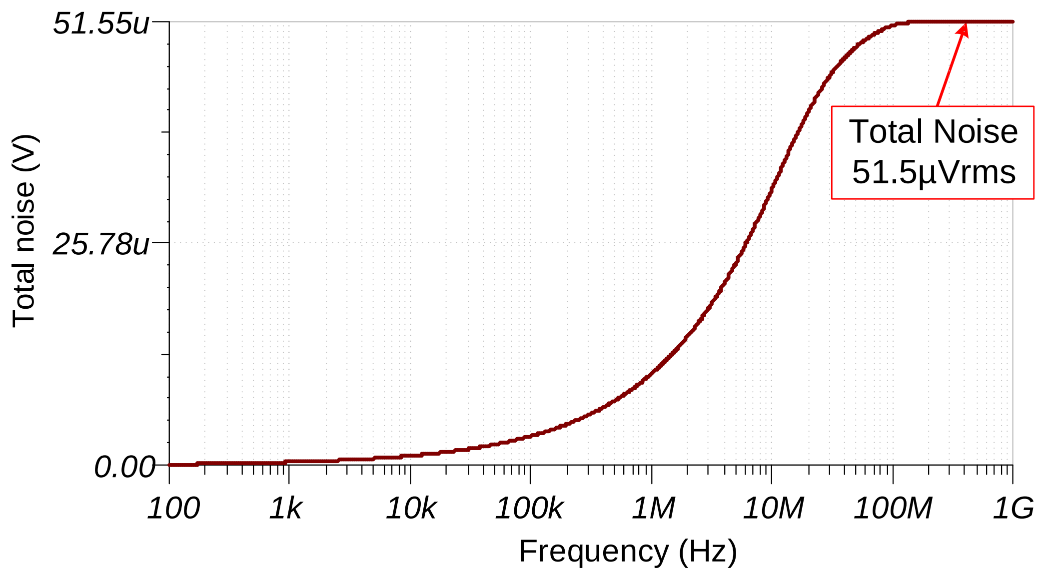
$$e_{noFDA} = \sqrt{\left(e_{nFDA}\cdot NG\right)^2 + 2\left(i_{nFDA}\cdot R_f\right)^2 + 2\left(4kTR_f\cdot NG\right)}$$

$$e_{noFDA} = \sqrt{\left(3.4nV/\sqrt{Hz}\cdot 2.00V/V\right)^2 + 2\left(0.5pA/\sqrt{Hz}\cdot 1k\Omega\right)^2 + 2\left(16.56\cdot 10^{-18}\cdot 2.00V/V\right)}$$

$$e_{noFDA} = 10.629nV/\sqrt{Hz}$$

$$E_{nFDA} = e_{noFDA}\cdot\sqrt{K_n\cdot f_c} = \left(10.629nV/\sqrt{Hz}\right)\sqrt{1.57\cdot 17.62MHz} = 55.90\mu Vrms$$

The following figure shows the TINA simulated total noise for the FDA circuit. See *Calculating the Total Noise for ADC systems* for detailed theory on this subject. Note that the calculated and simulated noise compare well (calculated = 55.9μV_{rms}, simulated = 51.5μV_{rms}).



Design Featured Devices

Device	Key Features	Link	Other Possible Devices
ADS9224R	16-bit resolution, SPI, 3-MSPS sample rate, fully-differential input, integrated 2.5-V reference, dual, simultaneous sampling, low-latency	http://www.ti.com/product/ADS9224R	http://www.ti.com/adcs
THS4551	150-MHz, 3.3-nV / $\sqrt{Hz}$ input voltage noise, fully-differential amplifier	http://www.ti.com/product/THS4551	http://www.ti.com/opamps

Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Link to Key Files

See the Tina files for low-power sensor measurements - http://www.ti.com/lit/zip/SBAC219.

Revision History

Revision	Date	Change
A	November 2018	Downscale title. Updated the schematic in the *Transient Settling Optimization* section.