Circuit for driving a high-voltage SAR with an instrumentation amplifier

Dale Li

<table>
<thead>
<tr>
<th>Input</th>
<th>ADC Input</th>
<th>Digital Output ADS7042</th>
</tr>
</thead>
<tbody>
<tr>
<td>–10V</td>
<td>–10V</td>
<td>8000H</td>
</tr>
<tr>
<td>+10V</td>
<td>+10V</td>
<td>7FFFH</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Power Supplies</th>
<th>AVDD</th>
<th>DVDD</th>
<th>V&lt;sub&gt;ref&lt;/sub&gt;</th>
<th>V&lt;sub&gt;cc&lt;/sub&gt;</th>
<th>V&lt;sub&gt;ee&lt;/sub&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>5.0V</td>
<td>3.0V</td>
<td>5.0V</td>
<td>+15V</td>
<td>–15V</td>
</tr>
</tbody>
</table>

Design Description

Instrumentation amplifiers are optimized for low noise, low offset, low drift, high CMRR and high accuracy. The INA828 instrumentation amplifier performs a differential to single-ended conversion for a ±10-V range. The INA828 has excellent DC performance (that is, offset, drift), as well as good bandwidth. The ADS8568 is ideally suited to work with the INA828 as the ADC can be configured for a ±10-V single-ended input. To achieve the best settling, limit the sampling rate to 200kSPS or lower. For higher sampling rates see Driving High-Voltage SAR ADC with a Buffered Instrumentation Amplifier. Also, this design example uses unity gain (G=1) to translate a ±10-V differential input signal to a ±10-V single-ended output. For smaller input signals or higher gains, see Circuit for Driving an ADC with an Instrumentation Amplifier in High Gain. This circuit implementation is applicable to Industrial Transportation and Analog Input Modules that require precision signal-processing and data-conversion.
Specifications

<table>
<thead>
<tr>
<th>Specification</th>
<th>Goal</th>
<th>Calculated</th>
<th>Simulated</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transient Settling Error</td>
<td>&lt; 1/2 LSB (±152µV)</td>
<td>NA</td>
<td>–105µV</td>
</tr>
<tr>
<td>Noise</td>
<td>&lt; 20µV</td>
<td>103µV</td>
<td>86.6µV</td>
</tr>
</tbody>
</table>

Design Notes
1. The bandwidth of instrumentation amplifiers is typically not enough to drive SAR data converters at higher data rate. In this example, the sampling rate is reduced from 510kSPS to 200kSPS to achieve good settling. For full sampling rate see Driving High-Voltage SAR ADC with a Buffered Instrumentation Amplifier.
2. Check the common mode and output range of the instrumentation amplifier using the Common-Mode Input Range Calculator for Instrumentation Amplifiers software tool.
3. Use a COG type capacitor for \( C_{\text{filt}} \) to minimize distortion.
4. The Precision Labs video series covers methods for selecting the charge bucket circuit \( C_{\text{filt}} \) and \( R_{\text{fil}} \). See the Introduction to SAR ADC Front-End Component Selection for details on this subject.
Component Selection

1. The ADS8568 can accept a ±10-V single-ended input signal. The INA828 is used to translate a ±10-V differential signal to a ±10-V single-ended signal. So the INA828 is in unity gain for this example, and no external gain set resistor $R_g$ is needed. See Circuit for Driving an ADC with an Instrumentation Amplifier in High Gain in cases where the input signal range is small and gain is required.

2. The INA826 reference voltage ($V_{\text{ref}}$) input is used to shift asymmetrical input ranges to match the input range of the ADC. In this case the input range is symmetrical so the $V_{\text{ref}}$ pin is grounded ($V_{\text{ref}} = 0V$). See Circuit for Driving an ADC with an Instrumentation Amplifier in High Gain for an example where the $V_{\text{ref}}$ pin is used to adjust asymmetrical input signals.

3. Use the Common-Mode Input Range Calculator for Instrumentation Amplifiers to determine if the INA828 is violating the common-mode range. The common-mode calculator in the following figure indicates that the output swing is ±14.9V for a 0-V common mode input.

4. Find the value for $C_{\text{filt}}$ and $R_{\text{filt}}$ using TINA SPICE and the methods described in Introduction to SAR ADC Front-End Component Selection. The value of $R_{\text{filt}}$ and $C_{\text{filt}}$ shown in this document will work for these circuits; however, if you use different amplifiers you will have to use TINA SPICE to find new values.
DC Transfer Characteristics

The following graph shows a linear output response for inputs from differential –14.9V to +14.9V. The input range of the ADC is ±10V, so the amplifiers are linear well beyond the required range. See Determining a SAR ADC’s Linear Range when using Instrumentation Amplifiers for detailed theory on this subject. The full-scale range (FSR) of the ADC falls within the linear range of the instrumentation amplifier.

AC Transfer Characteristics

The bandwidth for this circuit is simulated to be 446.75kHz and the gain is 0dB.
Transient ADC Input Settling Simulation (200kSPS)

The following simulation shows settling to a 10-V DC input signal with INA828 and ADS8568. This type of simulation shows that the sample and hold kickback circuit is properly selected to within ½ of a LSB (152µV) at 200kSPS sampling rate on ADS8568. See the ADC Front End Component Selection video series for detailed theory on this subject.

Noise

This section shows a simplified noise calculation for a rough estimate. The bandwidth estimate was taken from the TINA simulation, and the noise density values are from the INA828 50-μV Offset, 7-nV/√Hz Noise, Low-Power, Precision Instrumentation Amplifier data sheet. The Kn factor of 1.22 is used because the filter is second order (the INA and output filter both have a pole).

\[
E_{n,\text{ADC}} = \text{Gain} \cdot \sqrt{e_n^2 + \left(\frac{e_{\text{noise}}}{\text{Gain}}\right)^2} \cdot \sqrt{K_n \cdot T_c}
\]

\[
E_{n,\text{ADC}} = 1 \cdot \sqrt{\left(7 \text{ nV}/\sqrt{\text{Hz}}\right)^2 + \left(90 \text{ nV}/\sqrt{\text{Hz}}\right)^2} \cdot \sqrt{1.22 \cdot 1.08 \text{MHz}} = 103 \mu\text{Vrms}
\]

Note that simulated and calculated are close but not exact (simulated = 86.6μV, calculated = 103μV). The difference is because the INA has gain peaking and the filter order is approximated as two but in reality the INA and filter poles are not exactly aligned.
Design Featured Devices

<table>
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<th>Device</th>
<th>Key Features</th>
<th>Link</th>
<th>Other Possible Devices</th>
</tr>
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<tbody>
<tr>
<td>INA826</td>
<td>Bandwidth 1 MHz (G=1), low noise 18 nV/√Hz, low offset ±40 µV, low offset drift ±0.4 µV/°C, low gain drift 0.1 ppm/°C, (Typical values)</td>
<td><a href="http://www.ti.com/product/INA826">http://www.ti.com/product/INA826</a></td>
<td><a href="http://www.ti.com/inas">http://www.ti.com/inas</a></td>
</tr>
</tbody>
</table>

Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Link to Key Files

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