±12-V voltage sensing circuit with an isolated amplifier and pseudo-differential input SAR ADC

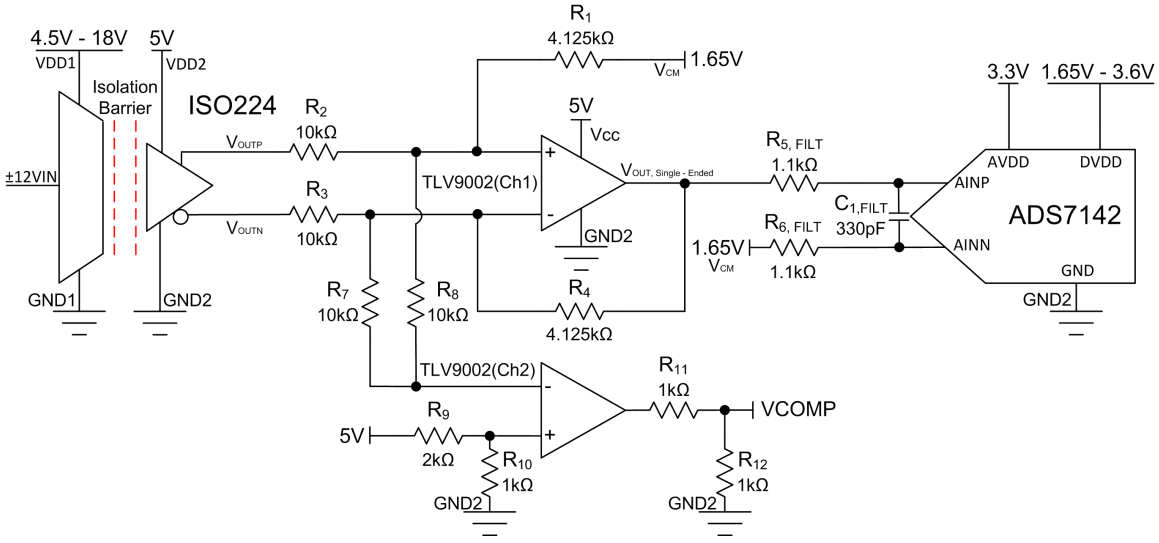
Alex Smith

ISO224 Input Voltage	ISO224 Output (V_{OUTP} - V_{OUTN})	ADS7142 Input (Pseudo-Differential)	ADS7142 Digital Output
+12V	+4V	3.3V	FFF_H
–12V	–4V	0V	000_H

Power Supplies and Reference Voltages			
VDD1	**VDD2 and Vcc**	**AVDD**	**GND**
4.5 V - 18 V	5 V	3.3 V	0 V

Design Description

This circuit performs a ±12-V isolated voltage sensing measurement utilizing the ISO224 isolated amplifier, TLV9002 operational amplifier, and the ADS7142 SAR ADC. The ISO224 can measure single-ended signals of ±12V with a fixed gain of ⅓V/V and produces a ±4-V isolated differential output voltage with an output common-mode voltage of VDD2 / 2. Channel 1 of the TLV9002 conditions the output of the ISO224 to fit the input range of the ADS7142, while Channel 2 monitors the ISO224 fail-safe output. The ADS7142 is a dual-channel ADC with a full-scale input and reference voltage of AVDD which can range from 1.65V to 3.6V. For this cookbook circuit, the ADS7142 dual-channel input will be used in a pseudo-differential configuration which allows for both positive and negative signals to be measured by the ISO224. This circuit is applicable to many high Voltage industrial applications such as *Train Control & Management Systems*, *Analog Input Modules*, and *Inverter & Motor Control*. The equations and explanation of component selection in this design can be customized based on system specifications and needs.



Specifications

Specification	Calculated	Simulated
Transient ADC input settling at 140kSPS	403µV	88µV
Conditioned signal range	0V–3.3V	0V–3.3V
Noise (at the input)	262µV_{RMS}	526µV_{RMS}
Closed-loop bandwidth	175kHz	145kHz

Design Notes

1. The ISO224 was selected due to its wide input range, flexible power configuration, and high accuracy.
2. The ADS7142 was selected due to its very low power, high level of integration, flexible power configurations, and small size.
3. The TLV9002 operational amplifier was selected for its cost optimization, configuration options, and small size.
4. Select low impedance, low noise sources for AVDD, V_{CM}, and the pseudo-differential input to AINN which sets the common-mode voltage of the ADC.
5. Find the ADC full-scale range and common-mode specifications. This is covered in component selection.
6. Select a COG capacitor for C_{FILT} to minimize distortion.
7. For best performance, consider using a 0.1% 20ppm/°C film resistor for $R_{FILT1,2}$ or better, to minimize distortion.
8. *Understanding and Calibrating the Offset and Gain for ADC Systems* covers methods for error analysis. Review the link for methods to minimize gain, offset, drift, and noise errors.
9. The *TI Precision Labs - ADCs* training video series covers methods for selecting the charge bucket circuit R_{FILT} and C_{FILT}. These component values are dependent on the amplifier bandwidth, data converter sampling rate, and data converter design. The values shown here will give good settling and AC performance for the amplifier and data converter in this example. If the design is modified, a different RC filter must be selected. Refer to *Introduction to SAR ADC Front-End Component Selection* for an explanation of how to select the RC filter for best settling and AC performance.

Component Selection

1. Select an isolated amplifier based on the input voltage range and determine the output common-mode voltage and output voltage range:

   The **ISO224** power supplies can be 4.5V to 18V for the high-side power supply, and 4.5V to 5.5V for the low-side power supply. The ISO224 has a ±12-V single-ended input range with a fixed gain of ⅓V/V, yielding ±4-V differential output at a common-mode voltage of VDD2 / 2, +2.5V for this example:

   $$\frac{\pm 12V_{IN,Single-Ended}}{3} = \pm 4V_{OUT,Differential} \text{ @ } 2.5V \left(\frac{V_{DD2}}{2}\right) \text{common-mode}$$

2. Select an ADC with small size and low power:

   The **ADS7142** is a small sized, low power, dual channel ADC that can be used in a pseudo-differential configuration. The max input range is set by the reference voltage and is equal to AVDD, 3.3V for this example:

   $$ADC_{Full-Scale\ Range} = V_{REF} = AVDD = 3.3V$$

   Find the required ADC common-mode voltage for pseudo-differential measurements:

   $$V_{CM} = \frac{V_{REF}}{2} = 1.65V$$

3. Select an operational amplifier that can convert the ±4-V differential, +2.5-V common-mode output of the ISO224 to the 3.3-V pseudo-differential, 1.65-V common-mode input of the ADS7142. Additionally, selecting an operational amplifier with a second channel that can monitor the fail-safe output feature of the ISO224 is preferred:

   The **TLV9002** is a 2 channel, rail-to-rail input and output amplifier optimized for cost sensitive and small size applications.

   Channel 1 is used to convert the ±4-V differential, +2.5-V common-mode output of the ISO224 to a 3.3-V peak pseudo-differential output with a common-mode voltage of 1.65 V. When R1 = R4 and R2 = R3, the transfer function is set by the following equation:

   $$V_{OUT} = V_{OUTP}\left(\frac{R4}{R3}\right) + V_{OUTN}\left(\frac{R1}{R2}\right) + V_{CM}$$

   The signal must be converted from ±4V to 3.3V, this means that the signal must be reduced by a factor of 3.3V/±4V = 3.3V/8V. Substituting V_{CM} with the previously calculated value of 1.65V and setting R2 and R3 to an easy to work with 10 kΩ yields the following equations:

   $$3.3V = 4V\left(\frac{R4}{10k\Omega}\right) + 1.65V \qquad 0V = -4V\left(\frac{R1}{10k\Omega}\right) + 1.65V$$

   Solving for R1 and R4 yields values of 4.125 kΩ.

   Additional information on this topic can be seen in the **Interfacing a Differential-Output (Isolated) Amplifier to a Single-Ended Input ADC** tech note.

   Channel 2 of the TLV9002 is used to monitor the fail-safe output feature of the ISO224. The ISO224 fail-safe output feature becomes active whenever the high-side power supply, VDD1, is missing independent of the input signal on the V_{IN} pin. The TLV9002 channel 2 output, VCOMP, is fed to a GPIO port on the system controller and goes high whenever the Fail-Safe output feature is active. For additional details please see the **Fail-Safe Output Feature** application note.

4. Select R_{1FILT}, R_{2FILT}, and C_{FILT} for settling of the input signal and sample rate of 140kSPS:

   Refine the R_{FILT} and C_{FILT} Values is a TI Precision Labs video showing the methodology for selecting R_{FILT} and C_{FILT}. The final value of 1.1 kΩ and 330pF proved to settle to well below ½ of a least significant bit (LSB) within the acquisition window.

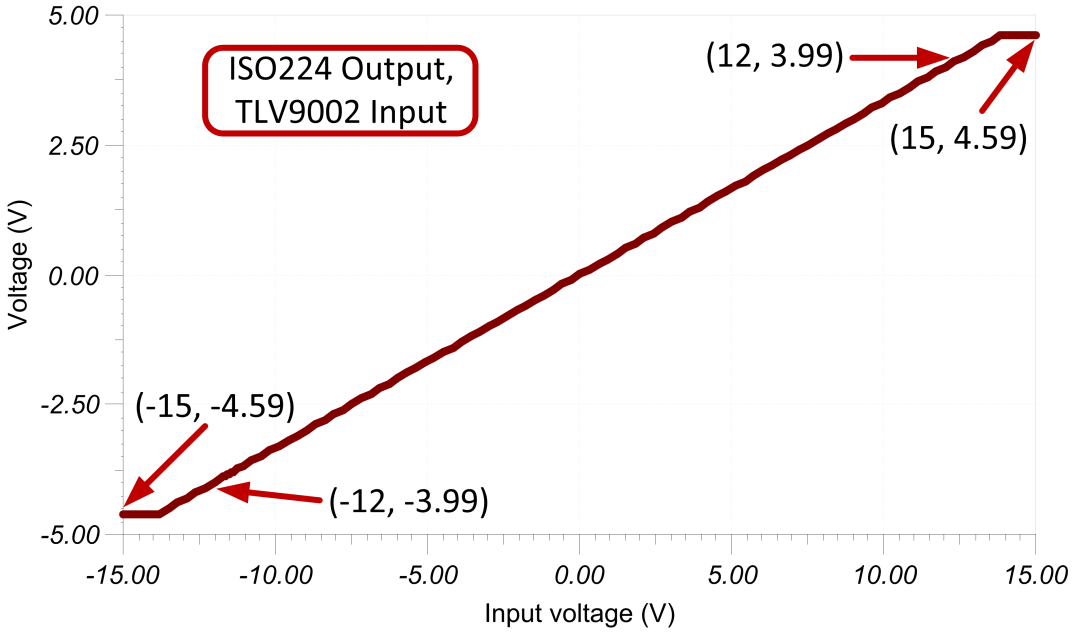
DC Transfer Characteristics

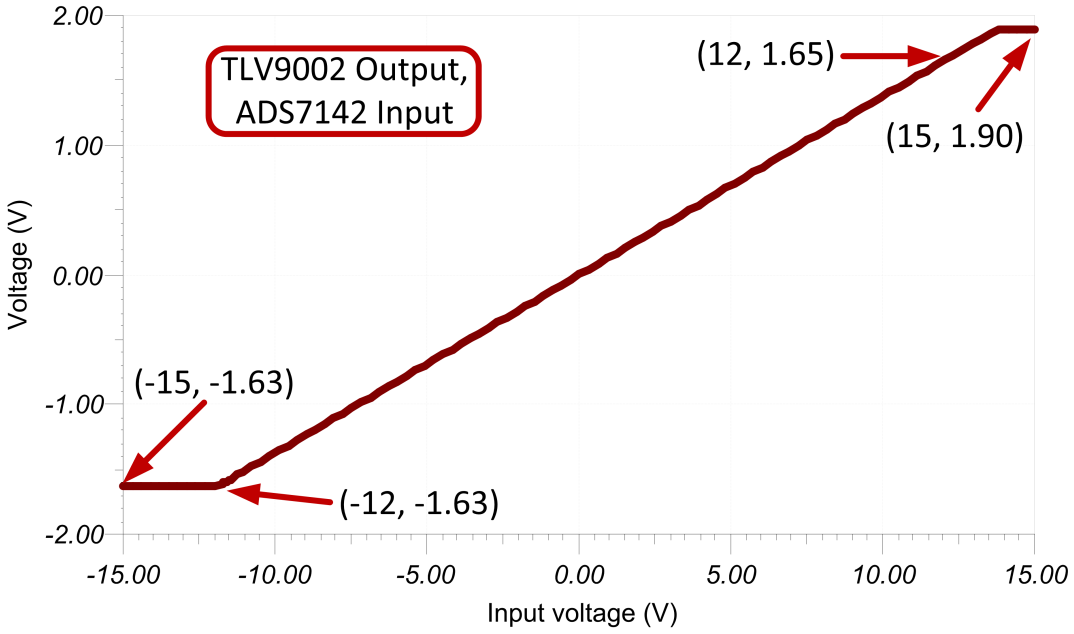
The following graphs show the simulated inputs of the TLV9002 and the ADS7142 from a ±15-V input signal to the ISO224. The ISO224 has a linear output of ±VIN/3 and the input to the TLV9002 can be seen in the first graph. The second graph shows that the TLV9002 further reduces the gain by VIN / 2.43 and shifts the common mode to 1.65V. This results in the full-range ±12-V input signal utilizing the 0V–3.3V full-scale range (FSR) of the ADC with AVDD = VREF = 3.3V.

The following transfer function shows that the gain of the ISO224 and TLV9002 is 1/7.28 V/V.

$$Gain_{ISO224} \cdot Gain_{TLV9002} \cdot V_{IN} = V_{OUT}$$

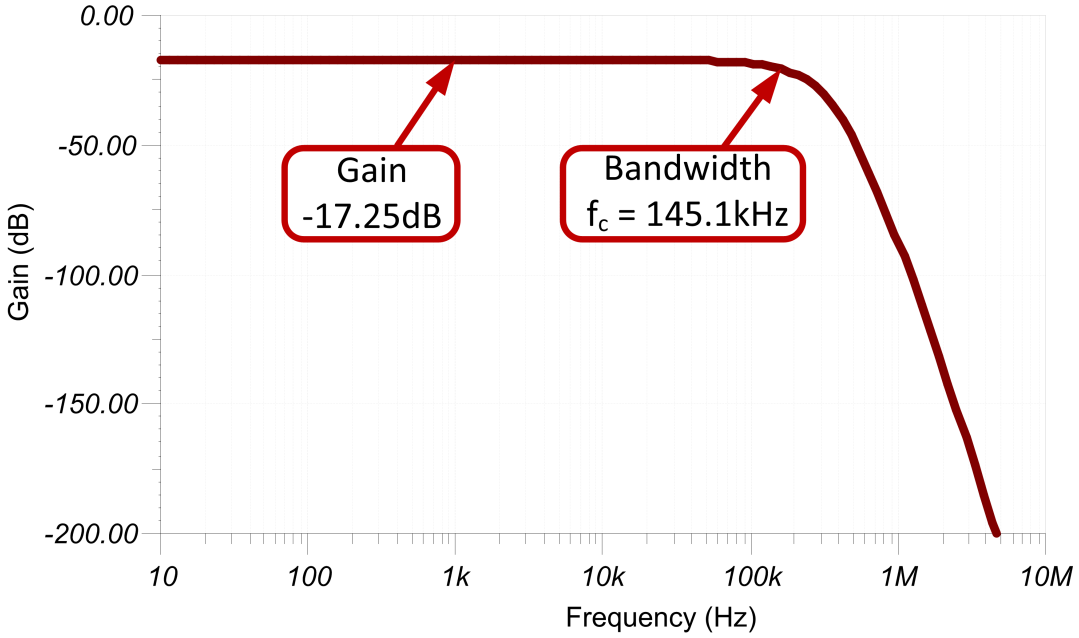
$$\frac{1}{3} \cdot \frac{1}{2.43} \cdot 12V = \frac{1}{7.28} \cdot 12V = 1.65V$$





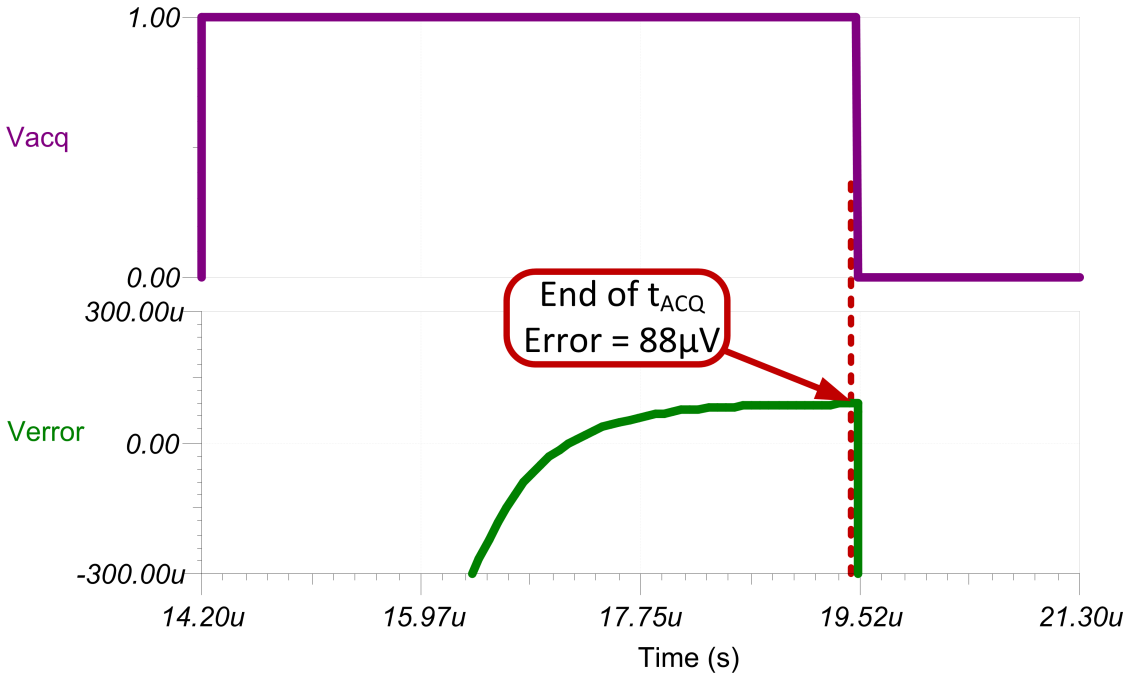
AC Transfer Characteristics

The simulated bandwidth of the signal chain is approximately 145kHz and the gain is –17.25dB which is a linear gain of approximately 0.137V/V (attenuation ratio 1/7.28V/V). This matches the expected gain of the system.



Transient ADC Input Settling Simulation

The following simulation shows the transient settling results with an acquisition time of 5.3µs. The 88µV of noise is well within the 0.5 · LSB limit of 403µV. See *Refine the Rfilt and Cfilt Values* for detailed theory on this subject.



Noise Simulation

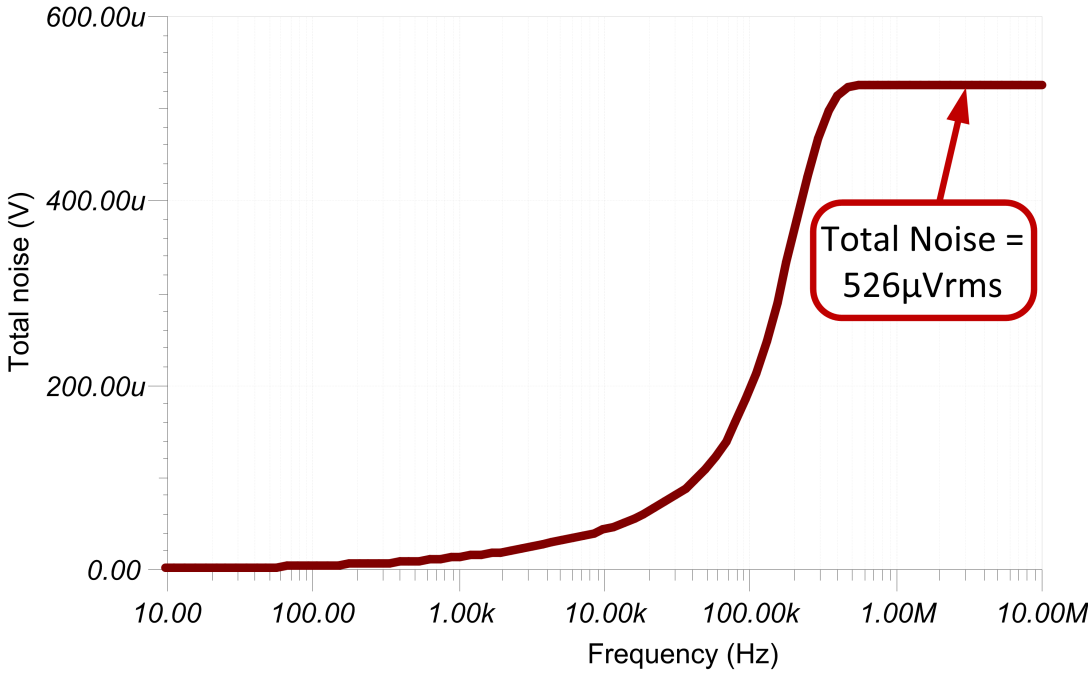
The simulated noise seen at the input of the ADC is greater than the expected calculated noise. This difference is due to noise peaking in the simulation model which is not included in the calculation. The following equations show that the ISO224 noise dominates the signal chain, and that the noise from the TLV9002 is negligible. Refer to *Calculating the Total Noise for ADC Systems* for detailed theory on this subject.

$$E_n = \text{Gain}(e_n)\sqrt{(1.57 \cdot BW)}$$

$$E_{nISO224A} = \frac{1}{3} \cdot \frac{1}{2.43}\left(4\mu V / \sqrt{Hz}\right) \cdot \sqrt{1.57 \cdot 145\,kHz} = 262\mu V_{RMS}$$

$$E_{nTLV9002} = \frac{1}{2.43}\left(27nV / \sqrt{Hz}\right) \cdot \sqrt{1.57 \cdot 145\,kHz} = 5\mu V_{RMS}$$

$$E_{nISO224A+TLV9002} = E_{nISO224A} + E_{nTLV9002} = \sqrt{262^2\,\mu V_{RMS} + 5^2\,\mu V_{RMS}} = 262\mu V_{RMS}$$



Design Featured Devices

Device	Key Features	Link	Similar Devices
ISO224	±12-V single-ended input range, Fixed gain of ⅓, yielding ±4-V differential output, output common-mode voltage of +2.5V, 4.5V to 18-V high-side power supply, 4.5-V to 5.5-V low side power supply, input offset: ±5mV at 25°C, ±42µV/°C max, gain error: ±0.3% at 25°C, ±50ppm/°C maximum, nonlinearity: ±0.01% maximum, ±1ppm/°C, high-input impedance of 1.25MΩ	www.ti.com/product/ISO224	www.ti.com/isoamps
ADS7142	Dual-Channel, full-scale input span and reference set by AVDD, 12-bit performance by default, 16-bit performance with High Precision Mode, very low current consumption of 0.45 µA at 600SPS	www.ti.com/product/ADS7142	http://www.ti.com/PrecisionADCs
TLV9002	Dual-Channel, rail-to-rail input and output amplifier, low broadband noise of 2727nV/√Hz, Low Input Offset Voltage of ±0.04-mV	www.ti.com/product/TLV9002	http://www.ti.com/opamps

Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Link to Key Files

TINA files for Isolated Design - http://www.ti.com/lit/zip/sbac226.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265