Power-supply margining circuit for SMPS using a precision DAC

Uttama Kumar Sahu

Design Goals

<table>
<thead>
<tr>
<th>Power Supply (DAC VDD)</th>
<th>Nominal Output</th>
<th>Margin High</th>
<th>Margin Low</th>
</tr>
</thead>
<tbody>
<tr>
<td>5V</td>
<td>5V</td>
<td>5V + 10%</td>
<td>5V – 10%</td>
</tr>
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</table>

Design Description

A power-supply margining circuit is used for tuning the output of a power converter. This is done either to adjust the offset and drift of the power-supply output or to program a desired value at the output. Adjustable power supplies like LDOs and DC/DC converters provide a feedback or adjust input that is used to set the desired output. A precision voltage output DAC is suitable for controlling the power-supply output linearly. An example power-supply margining circuit is shown in the following figure. Typical applications of power-supply margining is in Test and Measurement, Communications Equipment, and General Purpose Power Supply Modules.

Design Notes

1. Choose a DAC with required resolution, pulldown resistor value, and output range
2. Derive the relationship of the DAC output to $V_{OUT}$
3. Choose $R_1$ based on typical current through the feedback circuit
4. Calculate the start-up or nominal value of $V_{DAC}$, considering the power-down and power-up conditions of the DAC
5. Select $R_2$ and $R_3$ such that the desired start-up output voltage is met along with the DAC output voltage range for the desired tuning range
6. Calculate the margin low and margin high DAC outputs
7. Choose a compensation capacitor to get the desired step response
Design Steps

1. Select the switching DC/DC converter TPS5450 for the calculations. The DAC53608 device is an ultra-low cost, 10-bit, 8-channel unipolar output DAC suitable for such applications.

2. The output voltage of the power supply is given by

\[ V_{\text{OUT}} = V_{\text{REF}} + I_1 R_1 = V_{\text{REF}} + \left( I_2 + I_3 \right) R_1 \]

where

- \( I_1 \) is the current flowing through \( R_1 \)
- \( I_2 \) is the current flowing through \( R_2 \)
- \( I_3 \) is the current flowing through \( R_3 \)

DACs in this application typically include power-down mode, which includes an internal pulldown resistor at the voltage output. Hence, replacing the values of the currents in the previous equation yields:

- When DAC is in power-down mode:

\[ V_{\text{OUT}} = V_{\text{REF}} + \left( V_{\text{REF}} \frac{R_1}{R_2} \right) + \left( \frac{V_{\text{REF}}}{R_3 + R_{\text{PULL-DOWN}}} \right) R_1 \]

- When DAC output is powered-up:

\[ V_{\text{OUT}} = V_{\text{REF}} + \left( V_{\text{REF}} \frac{R_1}{R_2} \right) + \left( \frac{V_{\text{REF}} - V_{\text{DAC}}}{R_3} \right) R_1 \]

For DAC53608, \( R_{\text{PULL-DOWN}} \) is 10kΩ. For the LDO device TPS5450, the value of \( V_{\text{REF}} \) is 1.221V.

3. \( R_1 \) can be calculated with the following method:

The current through the FB pin of the TPS5450 device is negligible. Select \( I_1 \) to be 50µA. So, \( R_1 \) is calculated as follows:

\[ R_1 = \frac{V_{\text{OUT}} - V_{\text{REF}}}{I_1} = 75.6 \text{ kΩ} \]

The nominal value of \( I_1 \) is given by:

- When DAC is in power-down mode:

\[ I_{1-\text{Nom}} = \left( V_{\text{REF}} \frac{R_1}{R_2} \right) + \left( \frac{V_{\text{REF}}}{R_3 + R_{\text{PULL-DOWN}}} \right) \]

- When DAC output is powered-up:

\[ I_{1-\text{Nom}} = \left( V_{\text{REF}} \frac{R_1}{R_2} \right) + \left( \frac{V_{\text{REF}} - V_{\text{DAC}}}{R_3} \right) \]

The values of \( I_1 \) at margin high and margin low outputs are given by:

\[ I_{1-\text{HIGH}} = \frac{V_{\text{OUT-\text{HIGH}}} - V_{\text{REF}}}{R_1} = 56.6\text{µA} \]

\[ I_{1-\text{LOW}} = \frac{V_{\text{OUT-\text{LOW}}} - V_{\text{REF}}}{R_1} = 43.4 \]

4. The nominal, or startup value of \( V_{\text{DAC}} \) is calculated by the following method:

To make sure the 10-kΩ resistor does not impact when the DAC is transitioning from power-down to power-up, the power-up value for the DAC voltage is calculated with:

\[ V_{\text{REF}} \frac{R_1}{R_3 + 10 \text{ kΩ}} = \frac{V_{\text{REF}} - V_{\text{DAC}}}{R_3} \]
The previous equation is further simplified to:

\[ V_{DAC} = V_{REF} \left( \frac{10 \, k\Omega}{R_3 + 10 \, k\Omega} \right) \]

5. The values of \( R_2 \) and \( R_3 \) are calculated as follows:

If the power-up or nominal value of \( V_{DAC} \) is kept at 1/3 of \( V_{REF} \), that is, 407mV, then \( R_3 \) is \( 2 \times 10k\Omega = 20k\Omega \). And, \( R_3 \) can be calculated as:

\[ \frac{V_{REF}}{R_2} + \frac{V_{REF}}{R_3 + 10k\Omega} = 50\mu A \]

Replacing the value of \( R_3 \), calculate \( R_2 = 131.3k\Omega \).

6. Subtracting the margin high and nominal values of \( I_1 \) and the corresponding equations yields:

\[ \frac{V_{REF} - V_{DAC}}{R_3} - \frac{V_{REF}}{R_3 + 10k\Omega} = 6.6\mu A \]

The margin high value of \( V_{DAC} \) is 275mV and similarly, the margin low value is calculated as 539mV using the following equation:

\[ \frac{V_{REF} - V_{DAC}}{R_3 + 10k\Omega} - \frac{V_{REF}}{R_3} = 6.6\mu A \]

7. The step response of this circuit without a compensation capacitor causes the inductor current to reach its limit as shown in the following figure. This kind of surge can take the inductor into saturation. To minimize the surge, a compensation capacitor \( C_1 \) is used as the circuit diagram shows. The value of this capacitance is usually obtained through simulation. A comparative output shows the waveforms with a compensation capacitor of 10nF.

**Output With DAC in Power Down Mode**
Small-Signal Step Response Without Compensation

Small-Signal Step Response With $C_1 = 10\text{nF}$
Design Featured Devices and Alternative Parts

<table>
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<tr>
<th>Device</th>
<th>Key Features</th>
<th>Link</th>
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<tbody>
<tr>
<td>DAC53608</td>
<td>8-channel 10-bit, I2C interface, buffered-voltage-output digital-to-analog converter (DAC)</td>
<td><a href="http://www.ti.com/product/DAC53608">http://www.ti.com/product/DAC53608</a></td>
</tr>
<tr>
<td>DAC60508</td>
<td>8-channel, true 12-bit, SPI, voltage-output DAC With precision internal reference</td>
<td><a href="http://www.ti.com/product/DAC60508">http://www.ti.com/product/DAC60508</a></td>
</tr>
<tr>
<td>DAC8831</td>
<td>16-bit, ultra-low power, voltage output digital to analog converter</td>
<td><a href="http://www.ti.com/product/DAC8831">http://www.ti.com/product/DAC8831</a></td>
</tr>
<tr>
<td>TPS5450</td>
<td>5.5-V to 36-V input, 5-A, 500-kHz step-down converter</td>
<td><a href="http://www.ti.com/product/TPS5450">http://www.ti.com/product/TPS5450</a></td>
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Design References
See *Analog Engineer's Circuit Cookbooks* for TI’s comprehensive circuit library.

Link to Key Files

For direct support from TI Engineers use the E2E community e2e.ti.com

Revision History

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<th>Revision</th>
<th>Date</th>
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<tr>
<td>A</td>
<td>September 2019</td>
<td>Updated the circuit image on the first page.</td>
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