Circuit for differential output from a single-ended precision DAC

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Design Goals

Power Supply	DAC Output	Offset Range
VCC: 10V, VSS: –10V, VDD: 5V	0V to 5V	±5V

Design Description

This single-ended to differential conversion circuit features two operational amplifiers (op amp). It generates a bipolar differential output from a unipolar digital-to-analog converter (DAC) channel. These types of circuits are very useful in low-noise applications like Optical module, Metro data center interconnect, Ultrasound scanners, and X-ray systems. While another design approach using a fully-differential amplifier (FDA) is good for AC performance, the op amp approach will achieve best DC characteristics. Nevertheless, the specific op amp or FDA will impact the comparison of the two topologies.
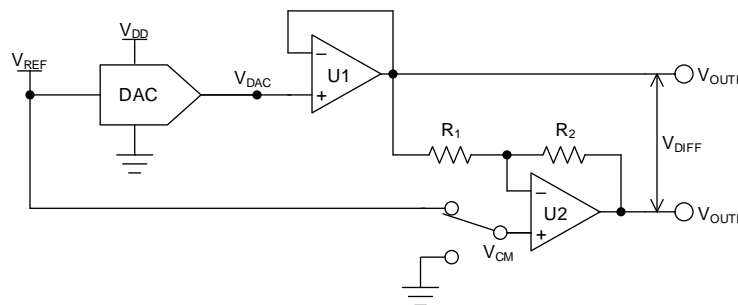
Design Notes

1. Choose a DAC with required resolution and output range
2. Select an op amp to meet the system specifications considering the following key requirements:
   - Swing to rail: For 5-V supply rails it is common to use a rail-to-rail zero-crossover distortion device (for example, OPA320 and OPA365)
   - Offset voltage and drift: One of the advantages of this circuit over the FDA approach is that some op amps can have very good DC performance
   - Bandwidth and quiescent current: Another advantage of this circuit over the FDA approach is that a wide range of op-amp bandwidth and related quiescent currents are available. For lower sampling rate, a low-bandwidth, low-current op amp may be an optimal choice
3. Choose R_1 and R_2 to minimize thermal noise at the output

Design Steps

1. Select a DAC such as DAC80501 that is a 16-bit single channel buffered voltage output DAC with 2.5-V internal reference. The reference output can also be used as the common-mode voltage (V_{CM})

2. Select a low-distortion op amp such as OPA320

3. The DC transfer function of the circuit is described with the following equations:

$$V_{OUTP} = V_{DAC}$$

$$V_{OUTN} = V_{CM}\left(1 + \frac{R_2}{R_1}\right) - V_{DAC}$$

- R_1 and R_2 is chosen as 1kΩ to have a gain of 1 and to minimize noise. Use 0.1% tolerance to minimize gain error.

- The thermal noise contributed by U1 to the differential output has two paths: directly through U1 and with inversion through U2. Both these noise are correlated and hence they will add directly. DAC80501 has an output noise density (e_{n-DAC}) of 74nV/$\sqrt{Hz}$ and OPA320 has a noise density (e_{n-AMP}) of 7nV/$\sqrt{Hz}$. The noise gain of U1 (G_{n-U1}) is 1. So, the total noise density contributed by output of U1 (e_{n-U1}) is given by:

$$e_{n-U1} = 2 \times \sqrt{\left(e_{n-DAC}\right)^2 + \left(e_{n-AMP}\right)^2} = 148.66 nV/\sqrt{Hz}$$

- The thermal noise contributed by the gain resistors R_1 and R_2, (e_{n-R}) is given by:

$$e_{n-R} = \sqrt{4.K.T.(R_1 \| R_2)} = \sqrt{4.(1.38 \times 10^{-23} J/K).(298.15K).(500\Omega)} = 2.87 nV/\sqrt{Hz}$$

- The uncorrelated noise density contributed by U2 (e_{n-U2}) is a combination of the thermal noise of the gain resistors (e_{n-R}), thermal noise of U2 (e_{n-AMP}), and the noise contributed by V_{CM} when fed through the V_{REF} output of DAC80501 (e_{n-VREF}). e_{n-VREF} is 140nV/$\sqrt{Hz}$. The noise gain of U2 (G_{n-U2}), that is, $1+(R_2/R_1)$ is 2. So, e_{n-U2} is written as:

$$e_{n-U2} = \sqrt{\left(e_{n-VREF}.G_{n-U2}\right)^2 + \left(e_{n-AMP}.G_{n-U2}\right)^2 + \left(e_{n-R}.G_{n-U2}\right)^2} = 280.4 nV/\sqrt{Hz}$$

- Finally, combining the noise from U1 and U2, we get the total noise density at the differential output (e_{n-T}):

$$e_{n-T} = \sqrt{\left(e_{n-U1}\right)^2 + \left(e_{n-U2}\right)^2} = 317.37 nV/\sqrt{Hz}$$

The simulated value for the thermal noise at the differential output is shown in the following figure. The simulated value 316.9nV/$\sqrt{Hz}$ is close to the calculated value. The thermal noise for the DAC output and V_{REF} output were emulated with equivalent resistors for noise simulation.
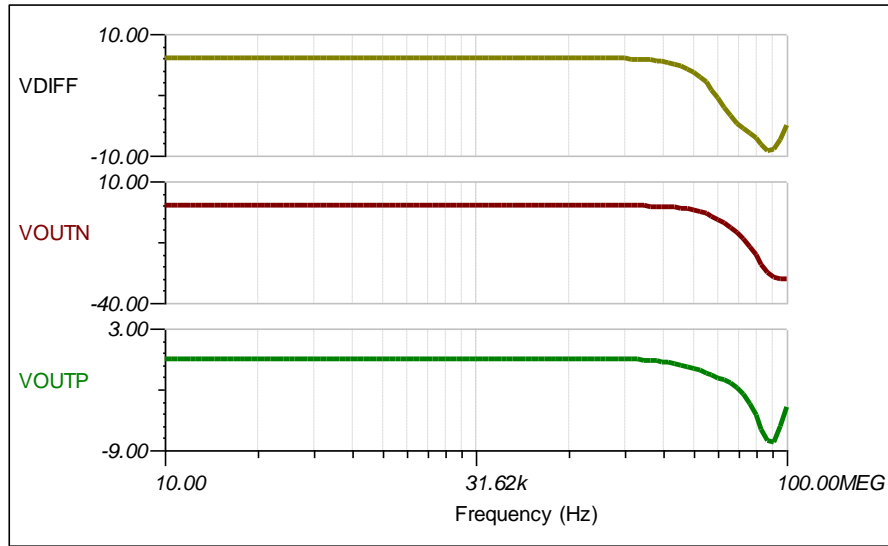
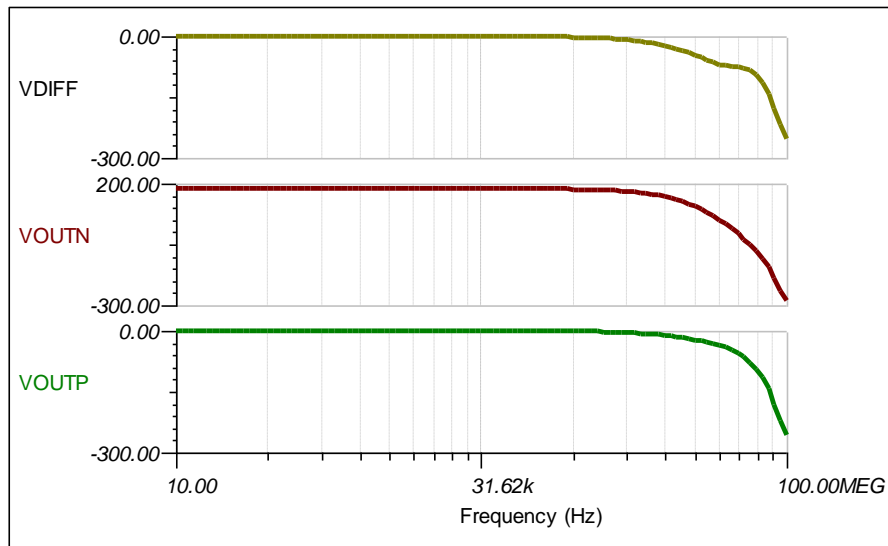## Thermal Noise Density at The Differential Output ($V_{CM} = V_{REF}$)
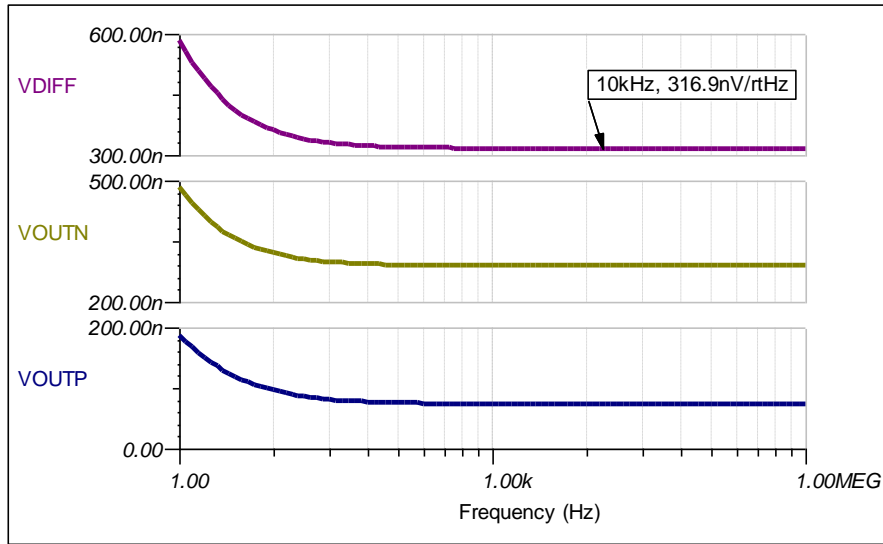
DC Transfer Characteristics ($V_{CM} = 0V$)
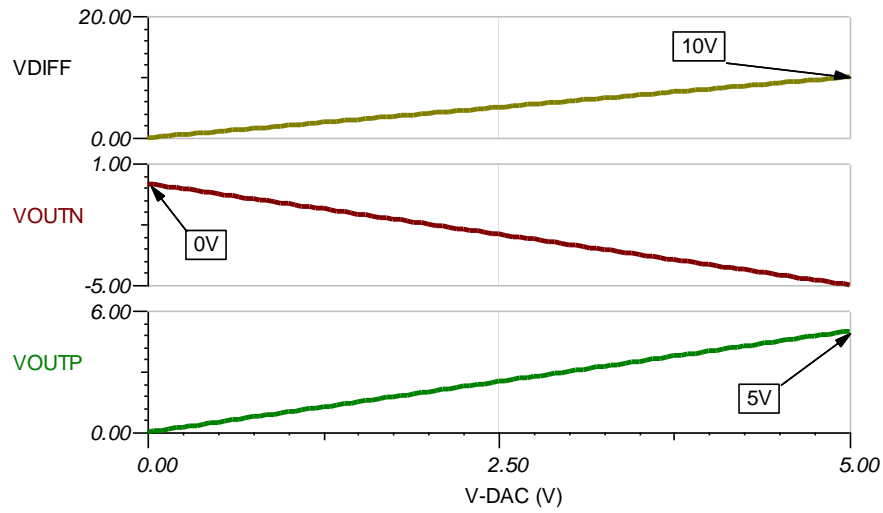
Frequency Response (Amplitude)


Frequency Response (Phase)

Group Delay

Group delay is the time delay between the applied input signal and the output signal. All amplifiers and filters have a group delay. Group delay is highlighted for this circuit because the inverting and noninverting path both have different group delays. This can create distortion for higher frequency signals. See the group delay in time domain plot for additional detail.
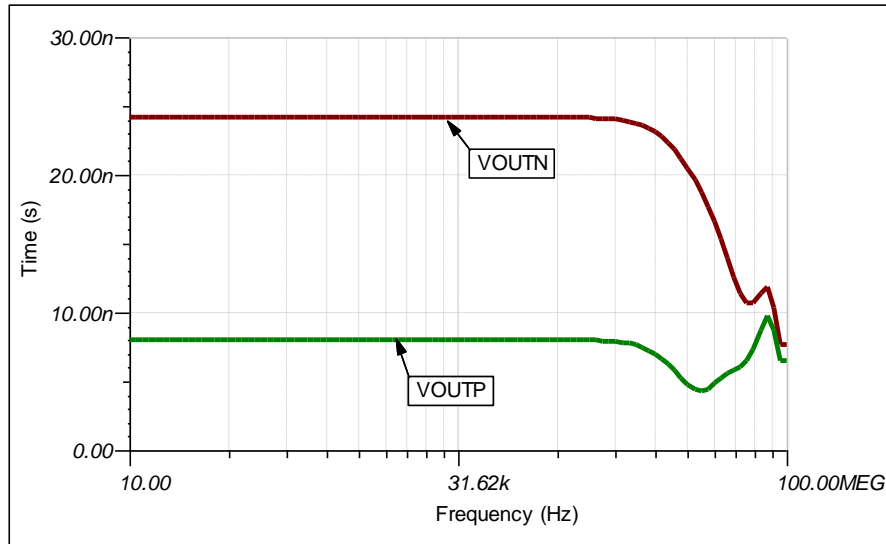
Output Transient Response
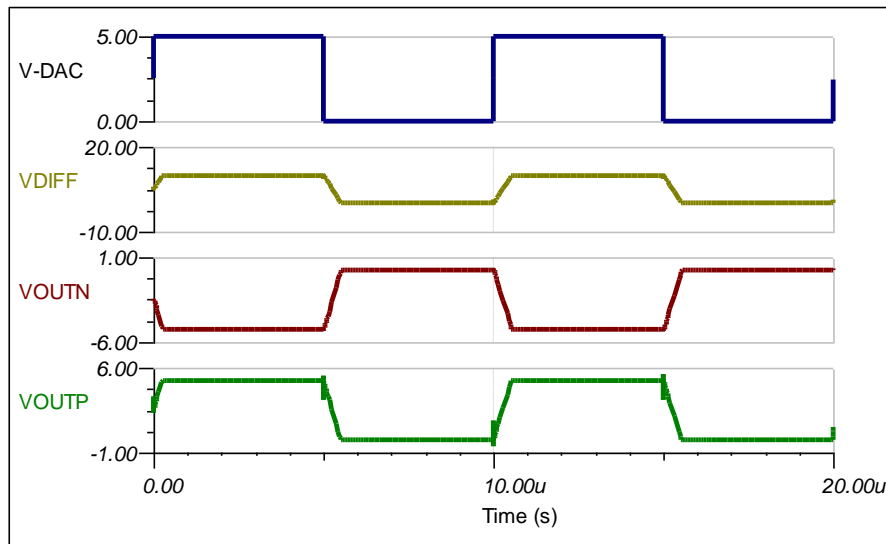
Design Featured Devices and Alternative Parts

Device	Key Features	Link
DAC80501	16-bit, 1-LSB INL, digital-to-analog converter (DAC) with precision internal reference	http://www.ti.com/product/DAC80501
DAC80508	8-channel, true 16-bit, SPI, voltage-output DAC with precision internal reference	http://www.ti.com/product/DAC80508
DAC8562	16-bit, dual-channel, low-power, ultra-low glitch, voltage output DAC with 2.5V, 4ppm/°C reference	http://www.ti.com/product/DAC8562
OPA320	Precision, zero-crossover, 20MHz, 0.9pA Ib, RRIO, CMOS operational amplifier	http://www.ti.com/product/OPA320
OPA365	2.2-V, 50-MHz, low-noise, single-supply rail-to-rail operational amplifier	http://www.ti.com/product/OPA365

Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Link to Key Files

TINA source files – http://www.ti.com/lit/zip/sbam419.

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