# Driving a low-voltage single-ended SAR ADC circuit with high-voltage input

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| Input | ADC Input | Digital Output ADS7056 |
|---|---|---|
| VinMin = 0V | AIN_P = 0V, AIN_M = 0V | $000_H$ or $0_{10}$ |
| VinMax = 10V | AIN_P = 3.3V, AIN_M = 0V | $FFF_H$ or $4096_{10}$ |

| Power Supplies | | |
|---|---|---|
| **Vcc** | **AVDD** | **DVDD** |
| 12V | 3V | 1.65V |

**Design Description**

This design is meant for increases the input range of a low-power SAR ADC by attenuating the input signal to match the full-scale range. The values in the component selection section can be adjusted to allow for a different input voltage range on the amplifier and full-scale range on the ADC. The input signal in this design is first buffered by the OPA192 device, a high-voltage precision amplifier, to avoid gain errors from the signal source impedance. A resistor divider at the output of the OPA192 device is then used to attenuate the signal and is again buffered by the OPA365 device. This wide-bandwidth amplifier allows the ADS7056 device to be used at its max sampling rate of 2.5MSPS. This circuit implementation is applicable to test and measurement, appliances, and factory automation and control. In general, this circuit can be used for most applications where a higher voltage signal needs to interface with a low-voltage single-ended ADC.
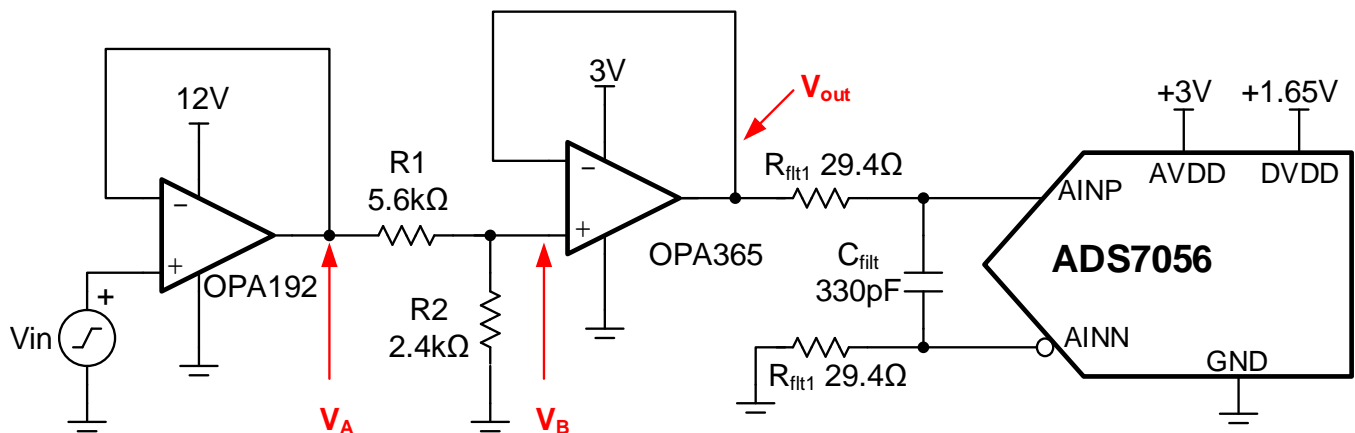
## Specifications

| Specification | Goal | Calculated | Simulated |
|---|---|---|---|
| Transient ADC Input Settling | < 0.5 · LSB = 91.5µV | | 16µV |
| Bandwidth | > 5MHz | 8.09MHz | 7.04MHz |
| Noise | < 0.5 · LSB | 20.85µV$_{RMS}$ | 22.74µV$_{RMS}$ |

### Design Notes

1. The input amplifier (OPA192) needs a common mode range from 0V to 10V. Since the negative supply is grounded, input swing to the negative rail or a rail-to-rail amplifier is required. The OPA365 device has a similar rail-to-rail requirement.

2. The output swing of the amplifiers limits the usable range near ground. A small negative supply (for example, –0.3V) could be used to provide output swing to ground. See *Powering a dual-supply op-amp circuit with one LDO* for a circuit to generate this supply.

3. Select C0G capacitors for Cfilt to minimize distortion.

## Component Selection

1. Find the maximum and minimum output for the linear operation of the input buffer OPA192. Use this with the gain in step 3 to calculate the overall linear range of the OPA192 device.
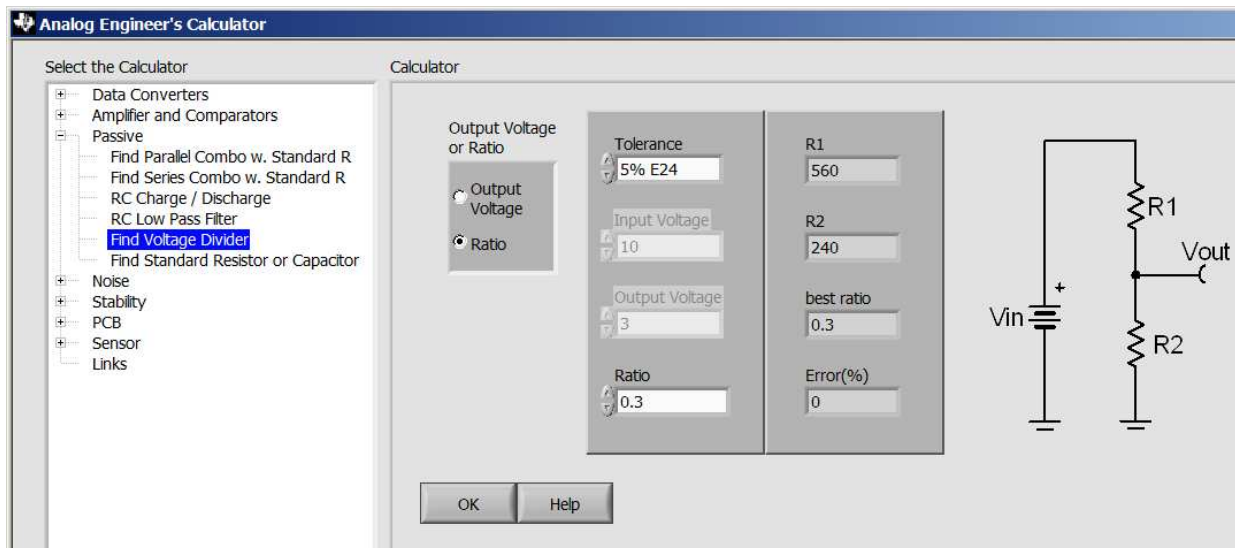
   - $(V-) - 0.1V < V_A < (V+) + 0.1V$ from OPA192 Vcm specification
   - $(V-) + 0.110V < V_A < (V+) - 0.110V$ from OPA192 Vout swing specification
   - $(V-) + 0.3V < V_A < (V+) - 0.3V$ from OPA192 Aol linear region specification
   - Combining the limitations, the overall range is $(V-) + 0.3V < V_A < (V+) - 0.3V$
   - Replacing $(V-) = 0V$ and $(V+) = 12V$ for the OPA192 supplies, the limit is $0.3V < V_A < 11.7V$

2. Find the gain based on input signal and ADC full-scale input range

$$Gain = \frac{V_{ADC(range)}}{V_{in(range)}} = \frac{3V}{10V} = 0.3 \, V \, / \, V$$

3. Find standard resistor values for voltage divider to provide gain. Use the *Analog engineer's calculator* ("Passive\Find Voltage Divider" section) to find standard values for voltage divider ratio.

$$Gain = \frac{R_2}{R_1 + R_2} = \frac{2.4\,k\Omega}{5.6\,k\Omega + 2.4\,k\Omega} = 0.3 \, V \, / \, V$$



4. The linear range for $V_B$ will consist of the range found in step one multiplied by our gain. The range is therefore: $0.09V < V_B < 3.51V$.

5. Maximum and minimum output for linear operation of the OPA365:

   - $(V-) - 0.1V < Vout < (V+) + 0.1V$ from OPA365 Vcm specification
   - $(V-) + 0.02V < Vout < (V+) - 0.02V$ from OPA365 Vout swing specification
   - $(V-) + 0.1V < Vout < (V+) - 0.1V$ from OPA365 Aol linear region specification
   - Combining the limitations, the overall range for OPA365 is $(V-) + 0.1V < Vout < (V+) - 0.1V$
   - Replacing $(V-) = 0V$ and $(V+) = 3V$ for the OPA365 supplies, the limit is $0.1V < V_A < 2.9V$

6. Combining the range from the OPA192 and the OPA365:

   - The linear range seen by the ADC is the worst case of the range of $V_B$ from the OPA192 (see step 4) and Vout from the OPA365 (see step 5).
   - ADC Range: $0.1V < Vout~ < 2.9V$

7. Find Rfilt and Cfilt to allow for settling at 2.5MSPS. See the TI Precision Labs – ADCs: *Refine the Rfilt and Cfilt Values* video showing the algorithm for selecting Rfilt and Cfilt. The final value of $29.4\Omega$ and 330pF proved to settle to well below ½ of a least significant bit (LSB).

## DC Transfer Characteristics

The following graph shows a linear output response for inputs from 0V to 10V. The image shows there is degraded performance towards both AVDD and ground. This is due to the linear ranges of the amplifiers in the *Component Selection* section. To improve performance at these extremes, the power supplies can be adjusted so that the linear range of both amplifiers fall within the full-scale range of the ADC.
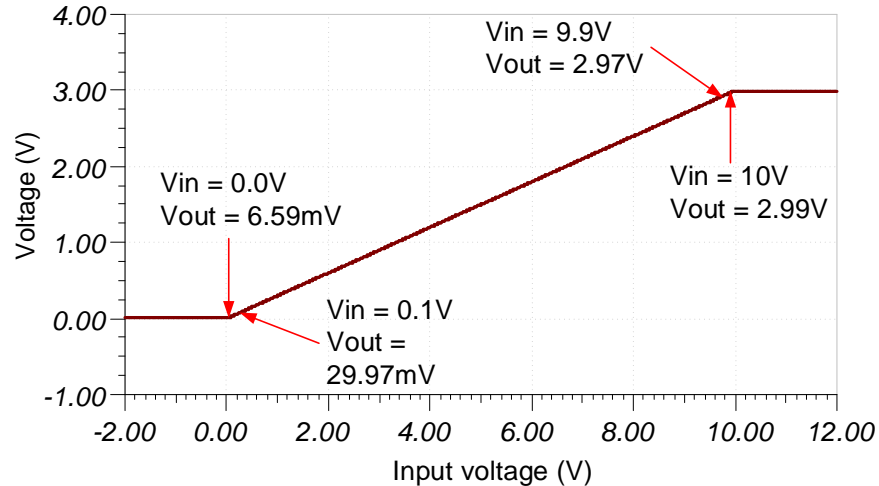


## AC Transfer Characteristics

The bandwidth is simulated at approximately 7MHz at the –3-dB point. The bandwidth is limited by both the OPA192 device and the RC charge bucket circuit (Rfilt and Cfilt). The bandwidth of the RC circuit is shown in the following equation to be 8.2MHz. The OPA192 device has a 10-MHz bandwidth which also affects the overall bandwidth of the circuit. The bandwidth goal was selected to be two times greater than that of the sampling frequency to ensure proper settling. See the *Amplifier Bandwidth* video for more details on this subject.

$$f_c = \frac{1}{2\pi \cdot (2 \cdot 29.4\,\Omega) \cdot (330\,\text{pF})} = 8.2\,\text{MHz}$$
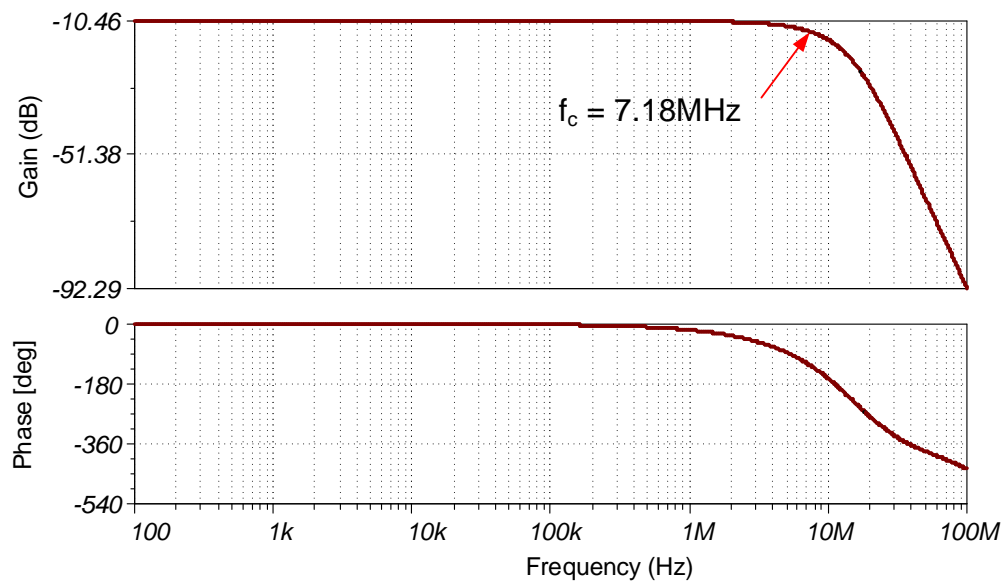
**Transient ADC Input Settling Simulation**

The following simulation shows settling for a 9-V DC input signal. This type of simulation shows that the sample and hold kickback circuit is properly selected to within ½ of a LSB (91.5µV). See the *Introduction to SAR ADC Front-End Component Selection* video for detailed theory on this subject.
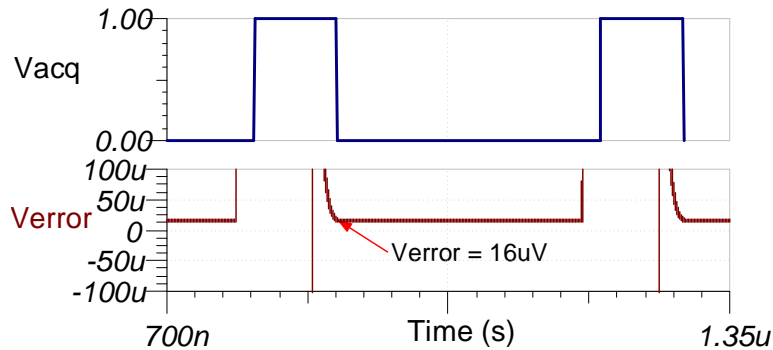


**Noise Simulation**

This section details a simplified noise calculation for a rough estimate. Noise from the OPA192 is attenuated by the resistor divider as shown:

$$e_{nOPA192} = 5.5\,\frac{nV}{\sqrt{Hz}} \cdot 0.3\,\frac{V}{V} = 1.65\,\frac{nV}{\sqrt{Hz}}$$

Resistor divider noise:

$$e_{ndiv} = \sqrt{4\,kTR} = \sqrt{4 \cdot (1.381 \cdot 10^{-23}) \cdot (273 + 25) \cdot 1.68\,k\Omega} = 5.259\,\frac{nV}{\sqrt{Hz}}$$

OPA365 noise density:

$$e_{nOPA365} = 4.5\,\frac{nV}{\sqrt{Hz}}$$

Total noise:

$$e_{nTOT} = \sqrt{e_{nOPA192}^2 + e_{ndiv}^2 + e_{nOPA365}^2} \cdot \sqrt{K_n \cdot f_c}$$

$$e_{nTOT} = \sqrt{\left(1.65\,\frac{nV}{\sqrt{Hz}}\right)^2 + \left(5.259\,\frac{nV}{\sqrt{Hz}}\right)^2 + \left(4.5\,\frac{nV}{\sqrt{Hz}}\right)^2} \cdot \sqrt{1.22 \cdot 7.18\,MHz} = 21.06\,\mu V$$

Note that calculated and simulated values match well. See the *Calculating the Total Noise for ADC Systems* video for detailed theory on this subject.

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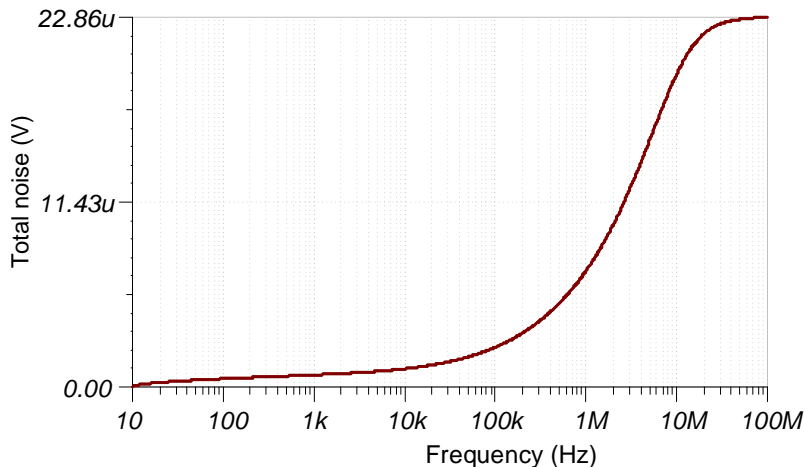
## Measured AC Results (FFT)

This performance was measured on a modified version of the ADS7056EVM with a 2-kHz input sine wave. The AC performance indicates SNR = 74.4dB, and THD = –84.07dB, which matches well with the specified performance of the ADC, SNR = 74.9dB and THD = –85dB. This test was performed at room temperature. See the *Introduction to Frequency Domain* video for more details on this subject.

| Parameter | Data Sheet Specification (Typ) | Measured Result |
|-----------|-------------------------------|-----------------|
| SNR | 74.9dB | 74.4dB |
| THD | –85dB | –84.07dB |

## Design Featured Devices and Alternative Parts

| Device | Key Features | Link | Other Possible Devices |
|---|---|---|---|
| ADS7056 | 14-bit resolution, SPI, 2.5-MSPS sample rate, single-ended input, AVDD/$V_{REF}$ input range 2.35V to 3.6V, DVDD 1.65V to 3.6V | http://www.ti.com/product/ADS7056 | http://www.ti.com/adcs |
| OPA192 | 8-kHz bandwidth, rail-to-rail output, 450-nA supply current, unity gain stable | http://www.ti.com/product/opa192 | http://www.ti.com/opamps |
| OPA365 | 50-MHz bandwidth, rail-to-rail output, zero-crossover, low offset 100-µV, low noise 4.5nV/√Hz, slew rate 25V / µs | http://www.ti.com/product/opa365 | http://www.ti.com/opamps |

### Link to Key Files

TINA source files – http://www.ti.com/lit/zip/SBAC248.

### References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

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