Inverting circuit for high-to-low voltage level translation to drive ADC

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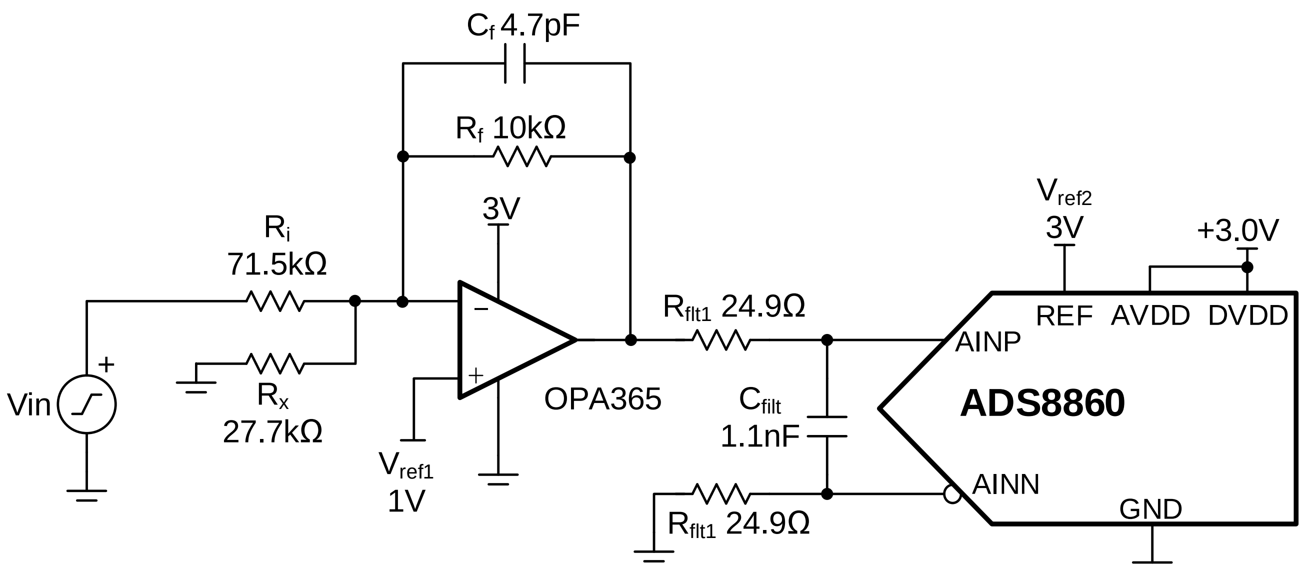
Input	ADC Input	Digital Output ADS8860
–10V	0.1V	0889_H or 2185_d
+10V	2.9V	$F777_H$ or 63351_d

Power Supplies			
Vref1	Vref2	AVDD	DVDD
1V	3V	3V	3V

Design Description

This circuit document describes how to translate a high-voltage signal (for example, ±10V) to low-voltage ADC inputs (for example, 0V to 3V). This circuit does not require any high-voltage supply to operate, but rather uses a voltage divider and level shift to translate the input signal. This circuit shows the OPA365 and ADS8860 devices, but the topology could be applied to many different ADCs. This design can be used a wide range of applications where a high-voltage input needs to be translated such as analog input modules for PLCs,instrumentation (lab, analytical, field and portable), and factory automation and control.



Specifications

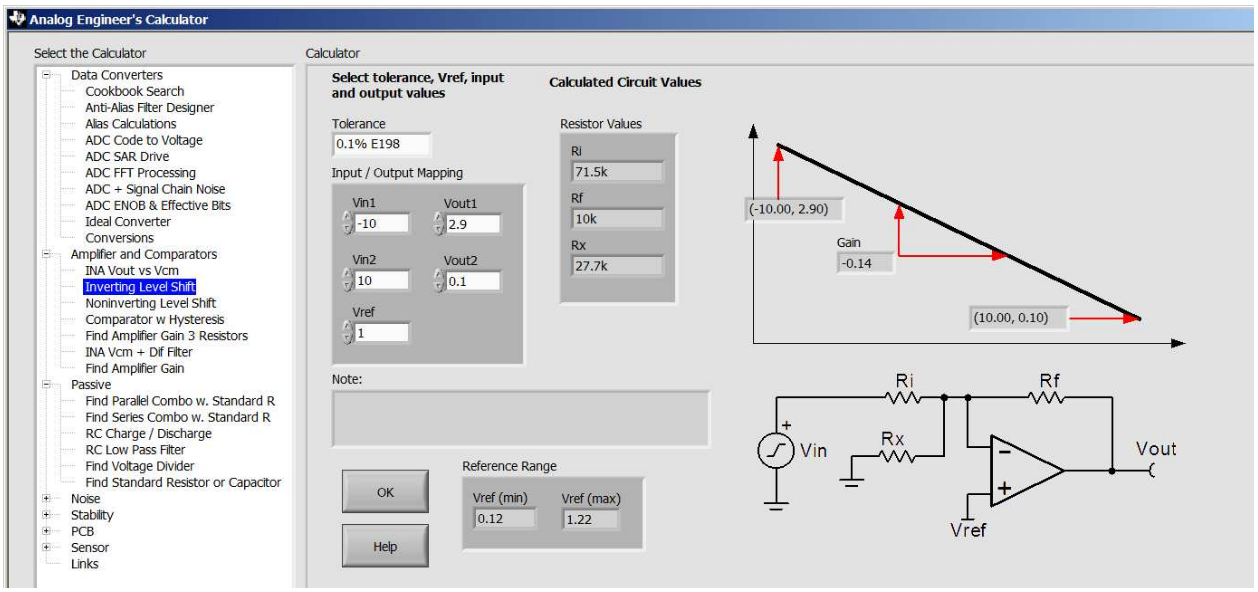
Specification	Goal	Calculated	Simulated
Sampling rate	1MSPS (max sampling rate)		800kSPS
Bandwidth	> 1MHz	Poles at 3.39MHz and 4.92MHz	2.44MHz
Noise	< 1/2 LSB = 38.1µV	29.52µV	31.55µV
Transient settling error	< 1/2 LSB = 38.1µV		–2.2µV

Design Notes

1. The common mode of this circuit is kept at a constant value (Vref1 = 1V in this example). Because the common mode is constant, the amplifier does not need to have a rail-to-rail input or zero crossover distortion. See the TI Precision Labs *Determining a SAR ADC's Linear Range when using Operational Amplifiers* video for more details.
2. Select a C0G type capacitor for Cfilt to minimize distortion.
3. Use 0.1% 20ppm / °C film resistors, or better, to minimize gain error and drift.
4. The input impedance of this circuit is Rin = Ri (71.5kΩ, in this example). For a high-impedance input, use a high-voltage amplifier buffer (for example, Vcc = +15V, and Vee = –15V). Alternatively, the input impedance could be increased by multiplying R_i, R_x, and R_f by the same factor. However, increasing the resistance on all the resistors will impact system noise.
5. The *TI Precision Labs - ADCs* video series covers methods for selecting the charge bucket circuit, Cflt and Rflt. See the *Introduction to SAR ADC Front-End Component Selection* video for details on this subject. In this example, the sampling rate was reduced from 1MSPS to 800kSPS, to improve settling.

Component Selection

1. First select the amplifier input and output range. In this example, the input range is –10V to +10V. The amplifier output range is set according to the ADC input and the amplifier linear output range. The ADC input range in this example is set by the reference voltage and is 3V. The amplifier supply is set to 3V to match the ADC input range. The output of the amplifier cannot swing to the power supply rails because of output swing limitations (that is, the linear range for the OPA365 device is $0.1V < V_{OUT} < 2.9V$). The output range can be adjusted further to provide design margin. For example, $0.2V < V_{OUT} < 2.8V$, provides margin for issues like power-supply variation.
2. The *Analog Engineer's Calculator* can be used in the next step to select component values. Enter the input and output voltages and reference voltage (–10V < Vin < +10V, and 0.1V < Vout < 2.9V). The range of acceptable reference voltages is given at the bottom of the tool (0.12V to 1.22V in this example). In this example, the reference is selected to be 1V. The tool outputs the 0.1% resistors required to map the voltages (R_i = 71.5kΩ, R_x = 27.7kΩ, R_f = 10kΩ).



3. The following equations show the transfer function for the inverting level-shift topology. It is possible to use these equations to solve for the different component values rather than the calculator. To do this, choose a reference value and fix the value of Rf to 10kΩ. Once done, solve for R_i and R_x for two different values of output signal. The algebra for this problem is a little complex, so using the calculator is the suggested method. Use the following equations to verify the transfer function:

$$V_O = -\frac{R_f}{R_i} \cdot V_{IN} + \left(1 + \frac{R_f}{R_i \| R_x}\right) \cdot V_{ref}$$

where

$$R_i \| R_x = \frac{R_i \cdot R_x}{R_i + R_x}$$

Using the values from the calculator:

R_i = 71.5kΩ, R_x = 27.7kΩ, R_f = 10kΩ, V_{ref1} = 1.0V

V_O = –0.1399V • V_{IN} + 1.5009V

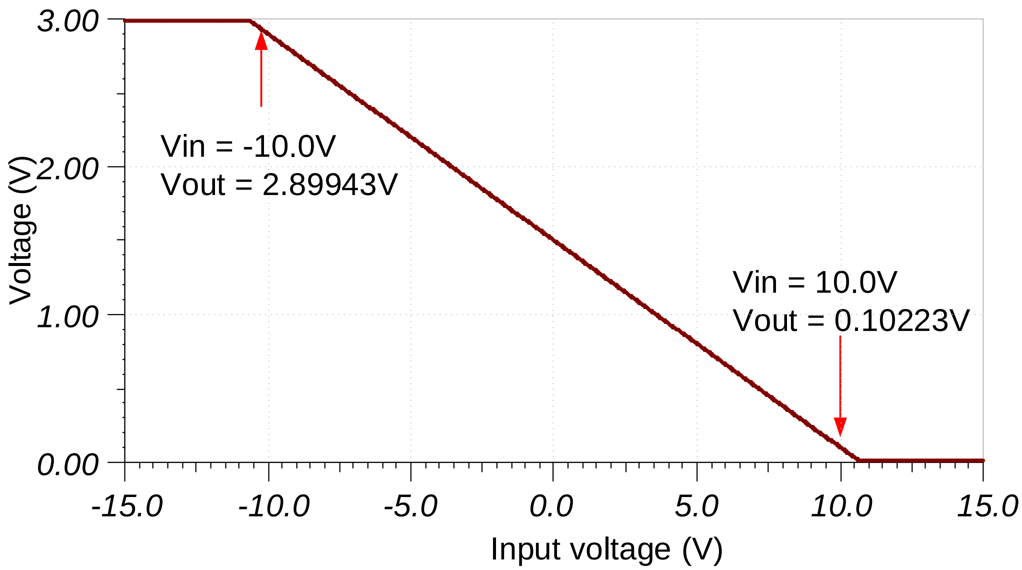
V_O(–10V) = 2.8995V

V_O(+10V) = 0.0123V

4. Find Rfilt and Cfilt to allow for settling at 1MSPS. The *Refine the Rfilt and Cfilt Values* video shows the algorithm for selecting Rfilt and Cfilt. The final value of 24.9Ω and 1.1nF proved to settle to well below ½ of a least significant bit (LSB).

DC Transfer Characteristics

The following graph shows the linear output response for a –10-V to 10-V input. In this case, the amplifier output is approximately 2.9V for a –10-V input and 0.1V for a +10-V input. This design was scaled so that the output range avoids the nonlinear power supply rails by 0.1V. See the *Determining a SAR ADC's Linear Range when using Operational Amplifiers* video for detailed theory on this subject.

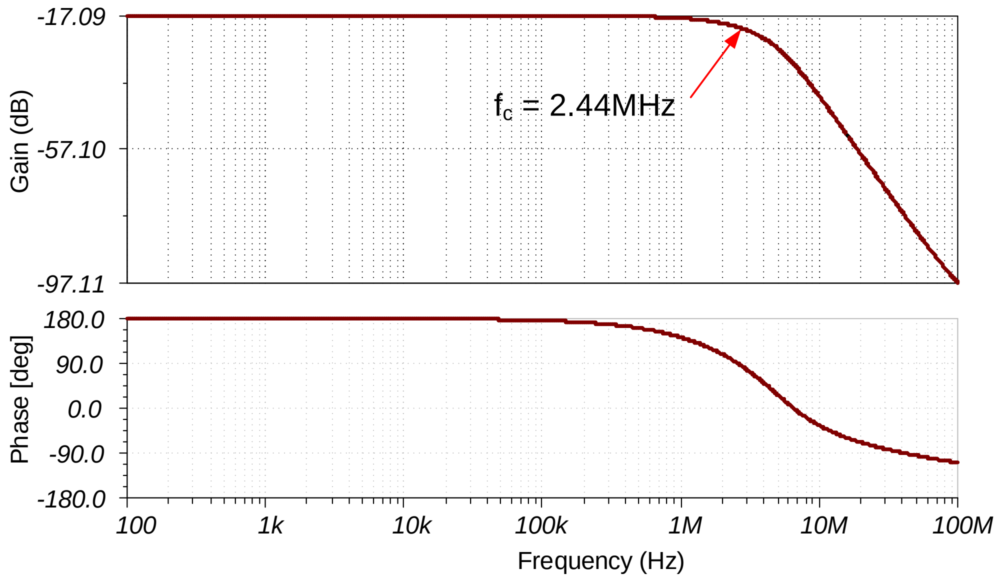


AC Transfer Characteristics

The bandwidth is limited by the Cf • Rf filter (f_{c1} = 3.39MHz) and the output filter (f_{c1} = 4.92MHz). These two poles combine to form a second-order filter with a simulated cutoff frequency at 2.44MHz. See the *Op Amps Bandwidth* video series for more details on this subject.

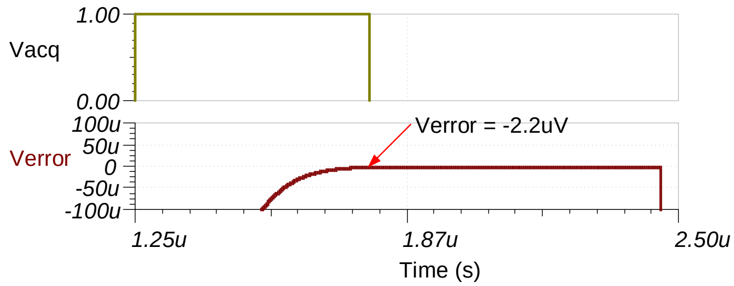
$$f_{c1} = \frac{1}{2\pi \cdot (10\,k\Omega) \cdot (4.7\,pF)} = 3.39\,MHz \text{ from the filter in the feedback network}$$

$$f_{c2} = \frac{1}{2\pi \cdot (2 \cdot 29.4\Omega) \cdot (1.1\,nF)} = 4.92\,MHz \text{ from the output filter}$$



Transient ADC Input Settling Simulation

The following simulation shows settling to a –10-V DC input signal. This type of simulation shows that the sample and hold kickback filter is properly selected. See the *Final SAR ADC Drive Simulations* video for detailed theory on this subject. Note: in this example the amplifier had settling issues, so the sampling rate was decreased from 1MSPS to 800kSPS. Reducing the sampling rate increases the acquisition period to improve settling (t_{acq} = 1 / f_{samp} – t_{conv} = (1/800kSPS) – 710ns = 540ns).



Noise Simulation

The following noise calculation takes into account the thermal noise of the resistor network, the amplifier noise, and the bandwidth limit from the filters. The calculated total noise is 29.52µV and the simulated total noise is 31.55µV. See the *Op Amp Noise Calculation* video for detailed theory on amplifier noise calculations, and the *Calculating the Total Noise for ADC Systems* video for data converter noise.

Noise equivalent input resistor network:

$$R_{eq} = \frac{1}{\frac{1}{R_i} + \frac{1}{R_x} + \frac{1}{R_f}} = \frac{1}{\frac{1}{71.5\,k\Omega} + \frac{1}{27.7\,k\Omega} + \frac{1}{10\,k\Omega}} = 6.67\,k\Omega$$

Resistor network noise:

$$e_{nReq} = \sqrt{4kTR} = \sqrt{4 \cdot (1.381 \cdot 10^{-23}) \cdot (273 + 25) \cdot 6.67\,k\Omega} = 10.48 \frac{nV}{\sqrt{Hz}}$$

OPS365 noise density:

$$e_{nOPA365} = 4.5 \frac{nV}{\sqrt{Hz}}$$

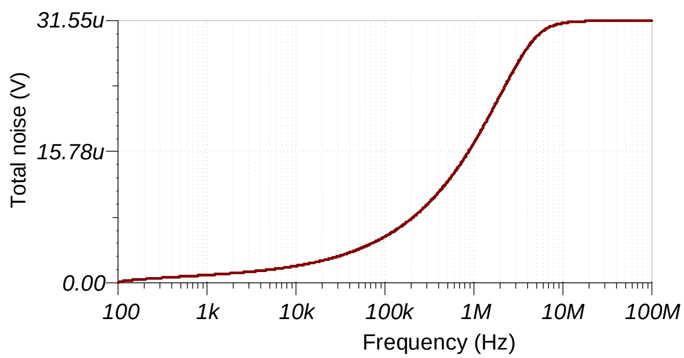
Noise gain:

$$G_n = \frac{R_f}{R_i \,||\, R_x} + 1 = \frac{10\,k\Omega}{(71.5\,k\Omega) \,||\, (27.7\,k\Omega)} + 1 = 1.501$$

Total noise:

$$e_{nTOT} = G_n \cdot \sqrt{e_{nOPA365}^2 + e_{nReq}^2} \cdot \sqrt{K_n \cdot f_c}$$

$$e_{nTOT} = (1.501)\sqrt{\left(4.5 \frac{nV}{\sqrt{Hz}}\right)^2 + \left(10.48 \frac{nV}{\sqrt{Hz}}\right)^2} \cdot \sqrt{1.22 \cdot 2.44\,MHz} = 29.52\,\mu V$$



Design Featured Devices and Alternative Parts

Device	Key Features	Link	Other Possible Devices
ADS8860	16-bit resolution, SPI, 1-MSPS sample rate, single-ended input, Vref input range 2.5V to 5.0V.	http://www.ti.com/product/ADS8860	http://www.ti.com/adcs
OPA365	50-MHz bandwidth, zero crossover distortion topology, rail-to-rail input and output, noise $4.5nV/\sqrt{Hz}$	http://www.ti.com/product/OPA365	http://www.ti.com/opamps

Link to Key Files

TINA source files – http://www.ti.com/lit/zip/sbac251.

References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265