Four-channel, differential input, DAQ front-end circuit with configurable voltage and current inputs

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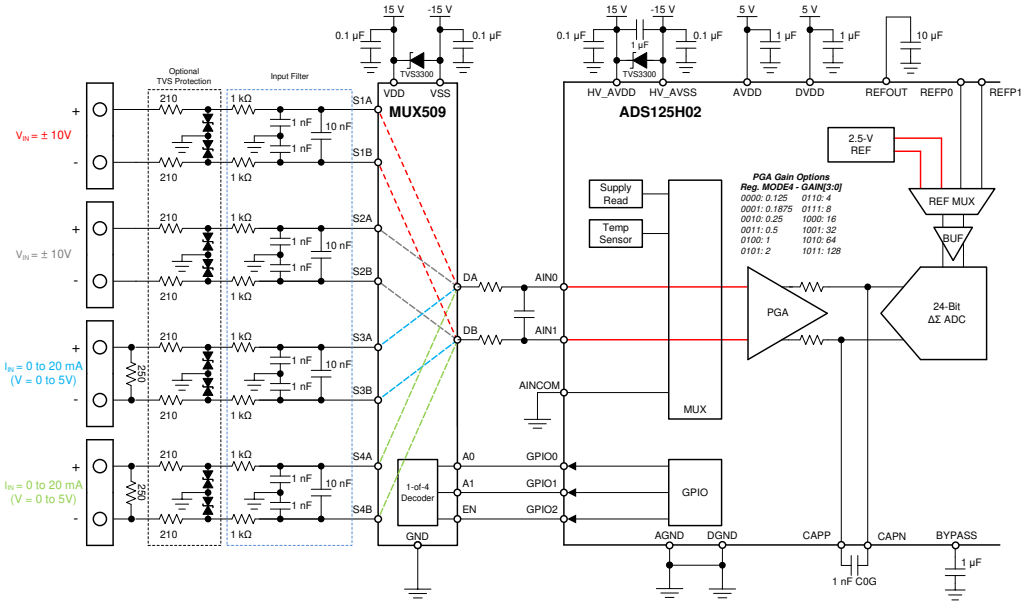
Feature	Value	Units
Number of channels	4	Differential channels
Data rate	≤ 10	kSPS
Voltage input range	±10.0	Volts
Current input range	0 to 20	mA
Voltage accuracy	0.05 typical | 0.10 maximum	%FS
Current accuracy	0.10 typical | 0.20 maximum	%FS

Power Supplies		
AVDD	**HV-AVDD**	**HV-AVSS**
5.0V	15.0V	–15.0V

Design Description

This circuit design describes how to use an ADS125H02 with integrated reference and programmable gain amplifier (PGA) to make voltage and current measurements on various ranges.

This circuit can be used in applications such as *analog input modules* for PLCs, avionics *remote data concentrators*, *lab and field instrumentation*, and other *factory automation* and *test and measurement* applications. Thermocouples and RTD are also common temperature sensors used in similar applications. For more information about making precision ADC measurements with a variety of RTD wiring configurations, see the *A Basic Guide to Thermocouple Measurements Application Report*.



Design Notes

1. Use supply decoupling capacitors for both the analog and digital supplies. For the high-voltage analog supply (HV_AVDD and HV_AVSS), place a 1.0-µF capacitor between the pins and place 0.1-µF capacitors from each supply to the ground plane. Connect 0.1-µF and 10-µF capacitors in parallel at AVDD to the ground plane. Connect a 1.0-µF capacitor from DVDD to the ground plane. Connect a 1.0-µF capacitor from BYPASS to the ground plane. For details on power supply recommendations, see the *ADS125H02 ±20-V Input, 2-Channel, 40- kSPS, 24-Bit, Delta-Sigma ADC With PGA and Voltage Reference Data Sheet*.
2. To minimize input current leakage, connect unused analog inputs to AGND when operating the device with bipolar supplies, or connect unused inputs to AVDD when operating the device with a unipolar supply.
3. Program unused GPIOs as outputs (default setting). If any GPIOs are programmed as inputs, the GPIO must not be allowed to float (unconnected), otherwise AVDD power-supply leakage current may result.
4. Consider adding TVS diodes between the high-voltage supplies (HV_AVDD to HV_AVSS) to provide overvoltage protection and avoid violating the absolute maximum rating of 38V. A TVS diode such as the TVS3300 provides a 33.0-V stand-off voltage (V_R), which is below the 30.0-V supply required, minimizing the current leakage of the diode, but has a typical break-down voltage (V_{BR}) and clamping voltage (V_C) of 35.8 V and 38.0 V, respectively (assuming a peak pulse current I_{PP} of 35.0 A), effectively protecting the ADC from an EOS event. For more details on EOS in ADCs, see *TI Precision Labs: EOS and ESD in ADC*.
5. When possible, use C0G (NPO) ceramic capacitors for input filtering. The dielectric used in these capacitors provides the most stable electrical properties over voltage, frequency, and temperature changes.
6. Input filtering for the ADC inputs and the reference inputs are selected using standard capacitor values and 1% resistor values. For an example design and analysis of these filters, see the *RTD Ratiometric Measurements and Filtering Using the ADS1148 and ADS1248 Family of Devices Application Report*.

Component Selection

1. Identify the system components:
   a. Given the following specifications are:
      - Input voltage range ≤ ±12.0V
      - Two voltage input channels, and two current input channels
      - Data rate ≤ 10 kSPS
      - 0.05%FS accuracy, or better
      - Optimized for cost

   b. Products selected:
      - ADS125H02 is a 24-bit, ±20-V input, delta-sigma ADC with integrated high-input voltage PGA and voltage reference. This device meets the input voltage range, accuracy, and data rate requirements, and it integrates a precision voltage reference, and GPIOs helping in cost optimization.
      - MUX509 is a differential 4:1, 36-V, precision, analog multiplexer. This device enables expanding to 4-channels using a single ADC for cost optimization.
      - Burden resistor:
        A burden resistor converts the current to a limited voltage to do measurements in the current measurement mode, a 250-Ω resistor was selected given the desired current range measurements (0 to 20mA), and a target burden voltage of 5.0V. Using a precision resistor ensures that the resistor does not become the limiting factor for system accuracy, the following specifications can be used as :
        – Accuracy ≤ 0.1%
        – Temperature coefficient ≤ 20 ppm/°C
        – Power rating ≥ 0.5W
      - Alternative and similar devices are listed in *Design Featured Devices*.

2. Perform error analysis calculations:

   A key consideration in the design of an analog input module is the error over the ambient temperature range resulting from the drift of gain, offset, reference voltage, and linearity error. This example shows the results of a Total Unadjusted Error (TUE) analysis that assumes an FS voltage of 10V, and that the initial offset and gain (including reference voltage error) are user calibrated at T_A = 25°C, as well as calibration overtemperature. The following table shows the maximum error, including the drift error of the ADC over the –20°C to 70°C temperature range, before calibration, and after calibration at room temperature, as well as overtemperature.

Maximum Error Before and After Calibration

Specification	Data Sheet Value	Error (ppm) Including ΔT = 90°C	Error (ppm) Assuming Gain and Offset Calibration
Internal VREF initial accuracy (maximum)	0.20%	2000.000	1.325
Internal VREF temperature drift (maximum)	1 ppm/°C	90.000	90.000
Internal VREF temperature hysteresis (70 ppm/105°C)	60 ppm/°C	60.000	60.000
Quantization noise	172.3nV$_{RMS}$	0.017	0.017
Noise	53µV$_{RMS}$	5.300	5.300
INL	0.001%	10.000	10.000
Offset	2500µV	250.000	1.325
Offset temperature drift	2000nV/°C	18.000	18.000
Gain error	0.70%	7000.000	1.325
Gain error temperature drift	4 ppm/°C	360.000	360.000
Total error (root sum of squares) [ppm]		**7294.124**	**376.507**
Total error (root sum of squares) [%FS]		**0.729**	**0.038**

3. Inspecting the data in *Maximum Error Before and After Calibration*, it is evident that the main contributors to the system total error calculations before any calibration is performed are the initial accuracy of the internal voltage reference, the gain error overtemperature, and the offset voltage, resulting in a total error of 0.729%FS. Assuming gain and offset calibration is performed, reducing the gain, offset, the initial accuracy of the reference to levels in the noise, resulting in the error similar to the ADC noise level, 1.325 ppm (assuming average of 16 samples), then the total error can be calculated to be reduced to 0.038%FS. Calibration overtemperature could be performed to improve the full scale accuracy even further.
4. Calculating PGA gain required:

   The PGA gain required is determined by the reference voltage and the input voltage range, which is: ±10V for the voltage measurements and 5.0V for the current measurements, assuming a burden resistor of 250Ω.

$$\text{Gain}_{\text{Voltage}} = \frac{\pm V_{IN\_FSR}}{V_{REF}} = \frac{\pm 10V}{2.5V} = 0.25V / V$$

$$\text{Gain}_{\text{Current}} = \frac{\pm V_{IN\_FSR}}{V_{REF}} = \frac{5.0V}{2.5V} = 0.50V / V$$

5. Verify PGA input limitations:

   As in typical amplifiers the integrated PGA has a maximum allowable input voltage (V_{AINX}), which can be found in the recommended operating conditions table in the *ADS125H02 data sheet*, and it is determined by the PGA gain, the maximum differential input voltage (V_{IN}), and the minimum value of the high-voltage power supply. Maintain the absolute input voltage (V_{AINX}) within the range as shown in the following equation; otherwise, an incorrect conversion data can result:

$$HV\_AVSS + 2.5 + \frac{V_{IN} \times (Gain - 1)}{2} < \mathbf{V_{AINx}} < HV\_AVDD - 2.5 - \frac{V_{IN} \times (Gain - 1)}{2}$$

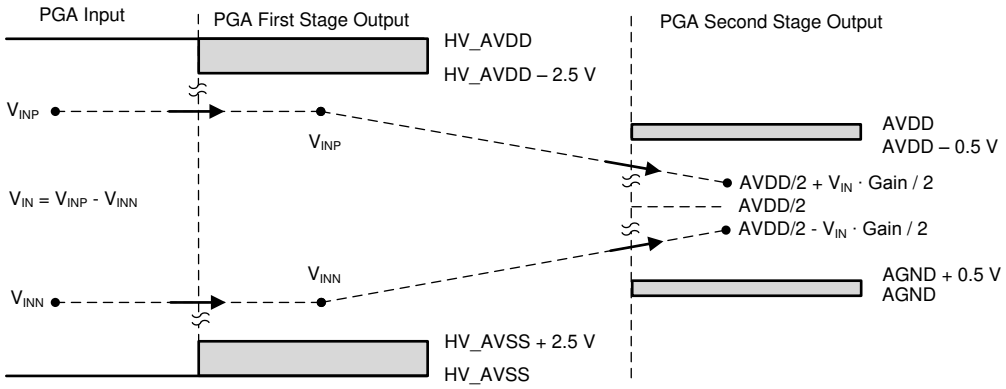
   where

   - For gain < 1, use value = 1 for gain
   - $V_{(AINx)}$ = Input voltage
   - $V_{IN} = V_{AINP} – V_{AINN}$ = Maximum expected differential input voltage

   In both the voltage and current measurements, since the gain < 1, the absolute input voltage must be:

   $–12.5V < V_{AINX} < 12.5V$

   The following image shows the relationship between the PGA input voltage to the PGA output voltage in attenuation mode. The first PGA stage is configured as a unity-gain follower, the second PGA stage attenuates the differential input and shifts the signal common-mode voltage to AVDD / 2 to drive the ADC input.



6. GPIO configuration:

   The ADS125H02 device provides four GPIO pins (GPIO0–GPIO4), two GPIOs are available on dedicated pins and two GPIOs are multiplexed functions with an external reference (REFP1 and REFN1). The GPIO input and output levels are referred to AVDD and AGND, so in this case the logic output levels are set to 5.0V. The following bits in registers 3 and 4 are used to control the GPIOs:

   - GPIO_CON[3:0] bits set the GPIO connection to the designated pin (1 = connected)
   - GPIO_DIR[3:0] bits program the direction of the GPIO as an input (1) or output (0)
   - GPIO_DAT[3:0] bits are the data values for the GPIO

   In this case, set GPIO_CON[3:0] to '0111', and set GPIO_DIR[3:0] to '1000', while the configuration for GPIO_DAT[3:0] will be dependant upon which channel is connected at any given time. The *MUX509 Truth Table and GPIO_DAT Configuration* table shows the configuration of the individual GPIO[x] bits depending on the input channel selected.

MUX509 Truth Table and GPIO_DAT Configuration

EN | GPIO2	A1 | GPIO1	A0 | GPIO0	State
0	1	1	MUX disabled
1	0	0	Channel 1 ON (Voltage)
1	0	1	Channel 2 ON (Voltage)
1	1	0	Channel 3 ON (Current)
1	1	1	Channel 4 ON (Current)

7. Digital filter selection:

   Digital low-pass filters are essential to the functionality of a delta-sigma ADC, which relies on oversampling and noise shaping to push quantization noise out of band. There are a variety of options for digital filters available in the ADS125H02 device. When choosing a digital filter, consider the following tradeoffs:

   - Slower data rates (higher oversampling ratios) have lower noise bandwidth. They are great for noise, but not for data throughput or detection of transient events.
   - The built-in PGA monitors are able to assist in detecting transient events that may affect the conversion results; therefore, the digital filter is generally able to be run at a slower data rate for better noise performance.
   - Higher-order SINC filters have slower settlings times when an input step is applied, but they provide lower noise bandwidth **and** increased notch width for removing common noise signals, such as power line noise which in practice may not occur at exactly 50Hz or 60Hz.
   - Digital filter notches occur at intervals of the SINCx filter data rate, so data rates of 50 SPS, 60 SPS or less are recommended for attenuating power line noise.
   - The 20 SPS FIR filter is unique from the SINCx filters in that it provides simultaneous rejection of 50- and 60-Hz noise and also settles within a single conversion cycle (like the SINC1 filter).

In this application, TI recommends a low-latency 20 SPS using a SINC1 filter, which is shown in the pseudocode example in the following section.

For more information about digital filters in the ADS125H02 device, see the following:

- The *Digital Filter* section of the *ADS125H02 Data Sheet*
- *Digital Filter Types in Delta-Sigma ADCs Application Report*

Register Settings

Configuration Register Settings for Voltage and Current Inputs

Register Address	Register Name	Field	Register Value	Description
05h	MODE3	GPIO_DAT[3:0]	See *MUX509 Truth Table and GPIO_DAT Configuration*	GPIO state (to control the external MUX)
	MODE2	GPIO_DIR[3:0]	1000	GPIO[2:0] outputs, GPIO[3] input
	MODE4	GPIO_CON[3:0]	0111	GPI0[2:0] connected GPIO[3] disconnected
10h	MODE4	MUX[2:0]	000	Internal MUX
10h	MODE4	GAIN[3:0]	0010 or 0011	PGA - Gains for voltage and current measurements, respectively
02h	MODE0	DR[4:0]	00100	Data rate: 20 SPS
02h	MODE0	FILTER[2:0]	000	Digital filter: SINC1

Pseudocode Example

The following pseudocode sequence shows the required steps to set up the device and the microcontroller that interfaces to the ADC to take subsequent readings from the ADS125H0x device for both voltage and current measurements. The dedicated $\overline{\text{DRDY}}$ pin indicates the availability of new conversion data. Pseudocode is shown without the use of the STATUS byte and CRC data verification. Download the *ADS125H02 Example C Code* from the ADS125H02 product folder or access it directly with the following link: *ADS125H02 Example C Code*.

Generic Pseudocode

```
Init:
{
    Configure microcontroller for SPI master, mode 1 (CPOL = 0, CPHA = 1), SCLK freq = 8 MHz
    Configure microcontroller GPIO for /DRDY as a falling edge triggered interrupt input

    Set CS1 low;
    Send 06h 00h A9h 00h;    // RESET command to ensure proper reset after power-up
    Set CS1 high;

    // DELAY

    Set CS1 low;
    Send 46h 10h 82h 00h;    // WREG to REF: Enable and select the internal 2.5V reference
    Set CS1 high;

    // NOTE: not necessary to issue a WREG to MODE0 command when using the default register values
    Set CS1 low;
    Send 42h 24h 5Ah 00h;    // WREG to MODE0: Continuous conversion, low-latency filter, 20 SPS
    Set CS1 high;

    Set CS1 low;
    Send 43h 08h 8Bh 00h;    // WREG to MODE1: Continuous conversion, 605us conv. start delay
    Set CS1 high;

    Set CS1 low;
    Send 44h 77h 9Ah 00h;    // WREG to MODE2: Enable GPIO outputs on GPIO0, GPIO1, and GPIO2
    Set CS1 high;

    Set channelNumber = 1
    Call Gain_Select()
    Call Channel_Select()

    // (OPTIONAL): For verification read back all register settings

    Call Start_New_Conversion()

}

Loop:
{
    Wait for DRDY falling edge interrupt...
    Do you want to switch to the next channel?
    {
        channelNumber = (channelNumber + 1) % 4;
        Call Gain_Select()
        Call Channel_Select()
        Call Start_New_Conversion()
    }

    Call Read_Data()
}

Channel_Select()
{
    // NOTE:
    // A0, A0 and EN are controlled by GPIO0, GPIO1 and GPIO2 respectively
```

```
    // STATUS0 byte is always enabled

    Set CS1 low;

    // WREG to MODE3 register to set GPIO pin levels
    If (channelNumber == 1)
        Send 45h 44h 16h 00h;    // EN=1; A1=A0=0
    ElseIf (channelNumber == 2)
        Send 45h 45h 11h 00h;    // EN=1; A1=0; A0=1
    ElseIf (channelNumber == 3)
        Send 45h 46h 18h 00h;    // EN=1; A1=1; A0=0
    ElseIf (channelNumber == 4)
        Send 45h 47h 1Fh 00h;    // EN=1; A1=A0=1

    Set CS1 high;
}

Gain_Select()
{
    // NOTE:
    // Using gain of 0.25 V/V for channels 1 & 2
    // Using gain of 0.50 V/V for channels 3 & 4
    // Always select AINP = AIN1 and AINN = AIN0 for analog inputs

    Set CS2 low;

    // WREG to MODE4 register to configure PGA gain
    If (channelNumber <= 2)
        Send 50h 02h D5h 00h;    // Gain = 0.25 V/V
    Else
        Send 50h 03h D2h 00h;    // Gain = 0.50 V/V

    Set CS2 high;
}

Start_New_Conversion()
{
    Set CS1 low;
    Send 08h 00h 7Fh 00h;    // START command
    Set CS1 high;
}

Read_Data()
{
    Set CS1 low;

    Send 12h 00h AAh 00h 00h      00h   00h   00h   00h;
    Receive FFh 12h 00h AAh [STATUS] [MSB] [MID] [LSB] [CRC]

    Set CS1 high;

    // Cast, concatenate, and sign-extend 24-bit data to signed 32-bit datatype
    signedValue = (((int32_t) [MSB] << 24) + ((int32_t) [MID] << 16) + ((int32_t) [LSB] << 8)) >>
8;

    // Convert ADC value to voltage (LSBsize = 2*VREF/GAIN)
    // NOTE:
    // Using gain of 0.25 V/V for channels 1 & 2
    // Using gain of 0.50 V/V for channels 3 & 4
    VoltageReading = (LSBsize * signedValue);

    If (channelNumber > 2)
        CurrentReading = (VoltageReading / BurdenResistance);
}
```

Design Featured Devices

Design Featured Devices

Device	Key Features	Link	Other Possible Devices
Analog to Digital Converter (ADC) with Integrated PGA and Voltage Reference			
ADS125H02	24-bit, 40-kSPS, 2-channel delta-sigma ADC with ±20-V input, PGA, IDACs, GPIOs, and VREF	ti.com/product/ADS125H02	Link to similar devices
ADS125H01	24-bit, 40-kSPS, 1-channel delta-sigma ADC with ±20-mV to ±20-V input	ti.com/product/ADS125H01	
Programmable Gain Amplifier (PGA)			
PGA280	4-channel, zero-drift, high voltage, programmable gain amplifier (PGA)	ti.com/product/PGA280	Link to similar devices
PGA281	1-channel, zero-drift, high voltage, programmable gain amplifier (PGA)	ti.com/product/PGA281	
Analog Multiplexer			
MUX509	Differential or dual 4:1, 36.0-V, precision analog multiplexer	x`ti.com/product/MUX509	Link to similar devices
MUX36D04	Differential or dual 4:1, 36.0-V, precision analog multiplexer *Lower leakage current*	ti.com/product/MUX36D04	
TMUX6104	Single-ended 4:1, ±16.5-V, precision analog multiplexer *Lowest leakage current, lowest on-capacitance*	ti.com/product/TMUX6104	
CD4052	Differential or dual 4:1, ±10.0-V analog multiplexer *Lowest cost*	ti.com/product/CD4052B	

Design References

See the *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Power Supply Reference Designs

The ADS125H02 device requires three analog power supplies (high-voltage supplies HV_AVDD and HV_AVSS, and low-voltage analog supply AVDD) and a digital power supply (DVDD). This circuit assumes a bipolar supply (±15.0 V) for HV_AVDD and HV_AVSS, and a 5.0-V supply. The following table shows there are specifications for three reference designs that could be used to provide the power supplies from a 24.0 V nominal input voltage.

		PMP10532	**PMP10516**	**TIDA-00689**
		Schematic Test Results	Schematic Test Results	Schematic Design Guide
V_{IN} range (V)		19.0–30.0V	20.4–28.8V	16.0–32.0V
Input type		DC		
V_{OUT} (V)	**Output 1**	15.0		
	Output 2	–15.0		
	Output 3	5.00		
$I_{OUT(maximum)}$ (A)	**Output 1**	0.200	0.200	0.601
	Output 2	0.200	0.060	0.601
	Output 3	1.000	0.100	0.200
$P_{OUT(maximum)}$ (W)	**Output 1**	3.0	3.0	0.5
	Output 2	3.0	0.9	
	Output 3	5.0	0.5	
Isolation		✓	✓	✓
Total efficiency at V_{IN} = 24V and Maximum I_{OUT}		86.0%	78.8%	44.0%
Footprint		60.0mm × 30.0mm	Approximately 60.0mm × 35.0mm	12.7mm × 40.8mm
Topology		Fly-Buck™	Fly-Buck™ + Linear regulator	Fly-Buck™ + Split rail converter

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