Application Report

High-Speed ADC: How to Properly Terminate Single-ended CMOS Digital Outputs

ABSTRACT

CMOS is a common data output interface for high speed ADCs, and is capable of achieving data transfer frequencies up to 250 MHz. In this application note, the focus is on how to properly terminate and treat single-ended CMOS digital outputs based on sampling speed and load capacitance.

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Trademarks

1 Introduction

High speed ADCs have use the CMOS output data interface for many years, and is a popular implementation for data rates up to 250 MHz. CMOS outputs have the advantage of lower power consumption, when compared to LVDS, but have other considerations that must be accounted for. The CMOS interface is used to represent ADC digital output data by representing 1's (For example: 1.8 V or HIGH) and 0's (0 V or LOW). Due to the nature of the CMOS output, series resistance is required to ensure signal integrity and ADC performance.

TINA, TI's free SPICE-based simulation tool, is used to demonstrate suitable series resistance based on different load capacitances.

2 CMOS RC Properties

Since the CMOS output is driving a metal trace that is ultimately connecting to an input of a receiver (FPGA, ASIC or microcontroller), there is some amount of capacitive load that the ADC CMOS outputs must deal with. The capacitive load we are considering comes from the characteristics of the PCB microstrip trace length, and the input capacitance at the CMOS receiver input. With no effective resistance in place, the CMOS output attempts to charge the capacitance with its entire drive strength. Adding series resistance reduces the instantaneous current that the CMOS driver provides, but also affects the rise time and overshoot/ringing that occurs on each HIGH to LOW transition.

When assuming the CMOS output slew rate is 1 V/ns, and a capacitive load of 5 pF, the current that the CMOS output provides can be calculated by multiplying the capacitance by the change in voltage over the change in time (1 V/1nSec x 5 pF = 5 mA of switching current per bit).

$$\Delta I = C\left(\frac{\Delta v}{\Delta t}\right) = 5pF * \frac{1V}{ns} = 5\ mA \tag{1}$$

Now, multiply that current by the number of outputs switching. For a 16 bit ADC, this is 80 mA (5 mA x 16) which gets "dumped" in the ground plane at the zero crossing or when the bits go from all 0's to all 1's. This large demand in current is the primary culprit of ground bounce which can cause performance degradation. However, adding a series resistance on each CMOS output will reduce this instantaneous current demand.

One other thing that adding a series resistor effects is the rise/fall time of the CMOS output since we are now creating an RC circuit. Care must be taken to ensure that the rise and fall time is sufficient enough for the CMOS levels to settle to the desired state (HIGH to LOW) in given time. This well-known rise time equation will produce the time required for a voltage to rise to 90% of the high value, and fall to 10% of the low value.

$$T_r = 2.2 * RC = 2.2 * 100\Omega * 5pF = 1.1ns \tag{2}$$

3 CMOS Simulations

The following TINA circuits are used to measure the instantaneous current and voltage by the CMOS driver.

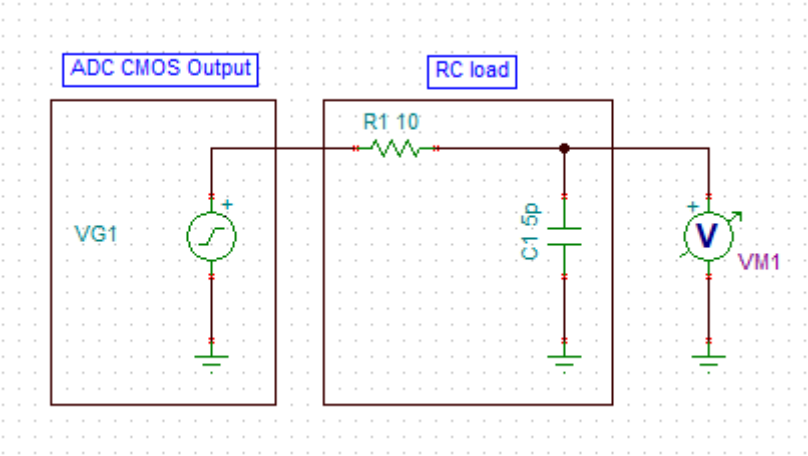

Figure 3-1. Simple CMOS RC voltage model

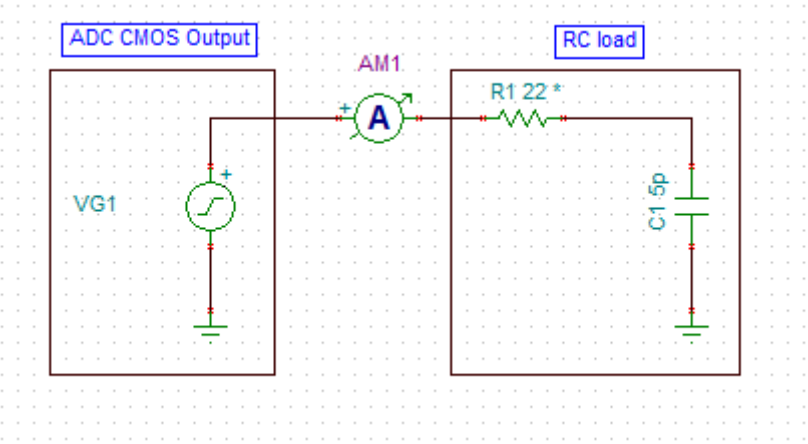

Figure 3-2. Simple CMOS RC instantaneous current model

Ideally, the CMOS signal settles quickly, and have minimal ringing. The simulations take into account different series resistances and with a fixed 5 pF load. An ideal CMOS source with 1 V / 1 nS rise time is used, so the simulations focuses primarily on the time required to settle to 1.8 V and 0 V.

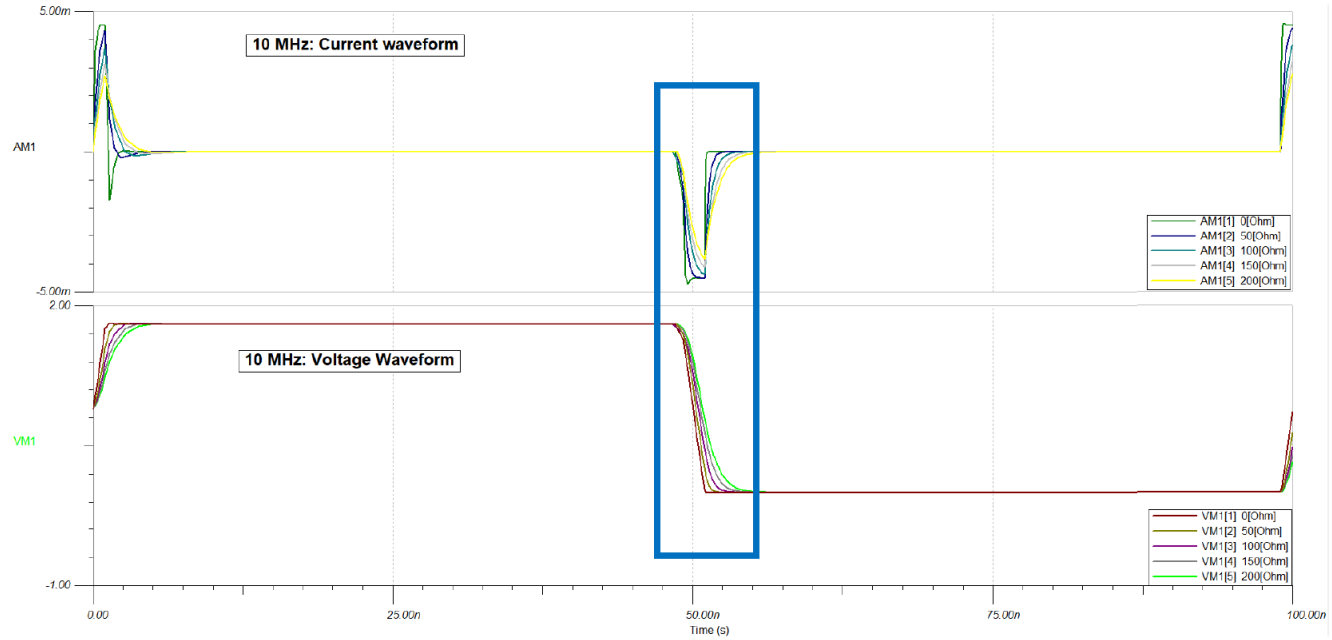

Figure 3-3. Current and Voltage waveforms at 10 MHz. Fixed 5 pF load, varying resistance.

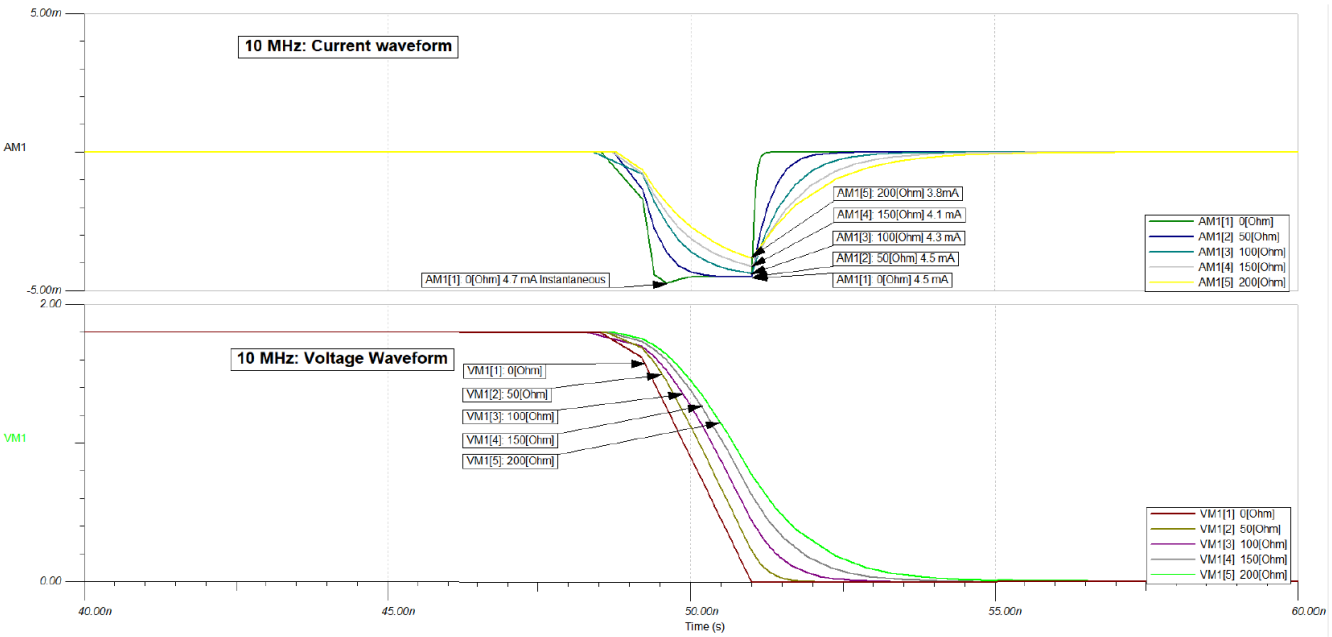

Figure 3-4. Zoom: Current and Voltage waveforms at 10 MHz. Fixed 5 pF load, varying resistance.

From the instantaneos current waveforms, it can be observed that the instantaneous and peak current is reduced as the series resistance is increased from 0 Ω to 200 Ω.

From the voltage waveforms, it can be observed that, as the resistance is increased, the voltage rise/fall times also increase in accordance with the RC constant.

At 65 MHz, the voltage waveforms are able to reasonably settle to the desired state before the next transition, so choosing a higher resistance may be a good choice in order to reduce instantaneous current demand. However, good engineering practice is encouraged to ensure that the interface timing requirements are being met when considering the series resistance value.

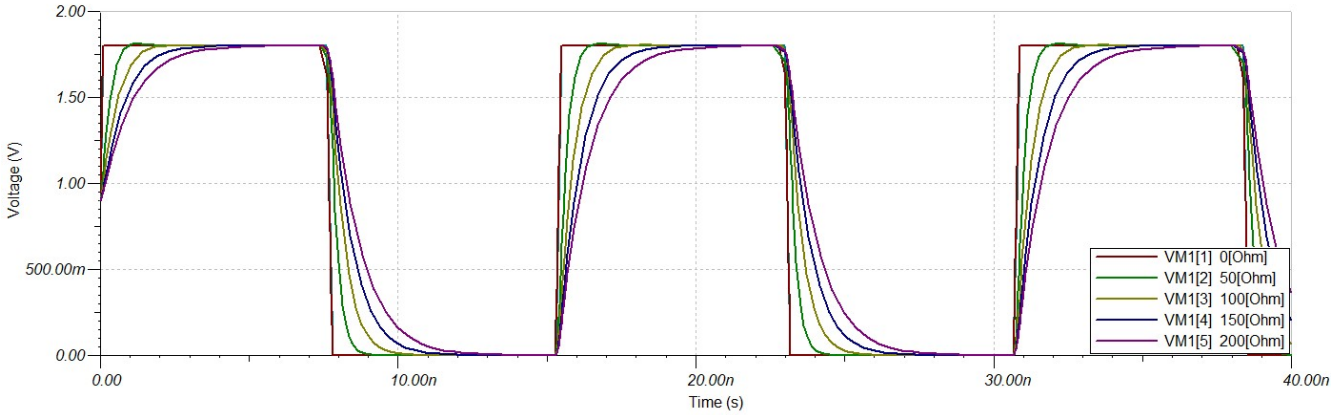

Figure 3-5. 65 MHz CMOS Voltage Waveform. Fixed 5 pF load, varying resistance.

Capacitive loads and series resistance values are more critical at higher CMOS data rates. At 250 MHz (max rate for CMOS), the RC constant can cause significant degradation in the ability to reach the High (1.8 V) and Low (0 V) states. From the simulations, 50 Ω would be the maximum resistance value at 5 pF capacitive load, but the designer would probably want to add additional margin by choosing a lower resistance value.

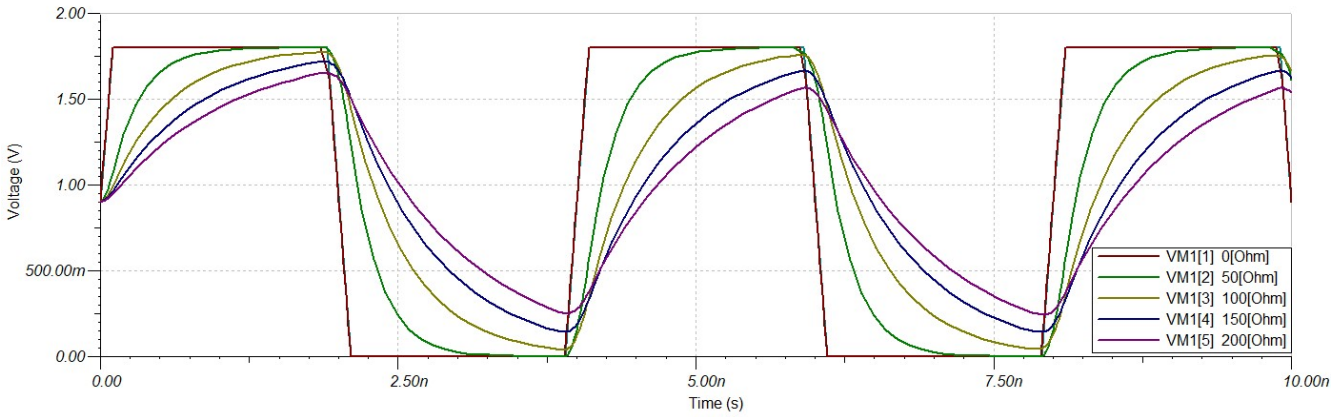

Figure 3-6. 250 MHz CMOS output. Fixed 5 pF load, varying resistance.

To summarize, the signal integrity of the ADC CMOS output is not as susceptible to small variations in RC values at low data rates, but become more critical as data rate increases. Reducing instantaneous/peak current is desired in order to avoid ADC performance degrading situations.

4 Mitigating Parasitic Capacitance

First, consider how the capacitive load can be reduced. Ideally, no capacitive load is desired, but that is not achievable in any realistic situation. To reduce capacitance, we must consider reducing the distance from the ADC CMOS outputs to the reciever inputs. On a PCB, the amount of metal trace corresponds directly to the amount of capacitance. There are calculators available that can help find the capacitance given the trace length,width, dielectric, and so on. For microstrip trace length, each inch of metal trace is approximately 3.3 pF for a 50 Ω impedance controlled trace.

Another consideration is the capacitive load of the CMOS receiver input pin. In most cases, this can range from 3 pF to 7 pF (check with manufacturers datasheet), so choosing the proper device can impact effective load capacitance.

If longer trace lengths are required, it may make sense to use a CMOS buffer. For instance, if the total length of trace is 10 inches long (approximately 33 pF), a CMOS buffer could be placed 2 inches away from the ADC (~6.6 pF of trace capacitance), and the buffer would then drive the remaining capacitance (~26 pF).

5 Summary

The CMOS interface is commonly used with high speed ADCs, and allows for ultra low power data transmission.

However, digital output load capacitance, if too high, can play a direct a effect on the converter's overall AC performance. These bad performance effects or ground bounce, can show up as a higher than normal level offset in the time domain and/or noisy FFT bins down at DC in the frequency domain.

By adding a simple series resistance on each of the digital outputs, this lessens the AC current required by the ADC during the zero crossing transitions.

This small circuit addition will ensure maximum performance of the high speed CMOS output ADC.

For more information on other high-speed data converter topics, please follow this link to TI's training videos.

6 References

- Texas Instruments, *ADC3541 14-bit Ultra-Low-Power High-SNR ADC with 10-MSPS Sampling Rate data sheet*
- Texas Instruments, *ADC3643 Dual, 14-bit, 1-MSPS to 65-MSPS, low-noise, ultra-low-power, analog-to-digital converter (ADC) data sheet*

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