

TLV320ADCx120 Power Consumption Matrix Across Various Usage Scenarios



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Precision ADC

ABSTRACT

This application report details the power consumption of TLV320ADCx120 devices across various usage scenarios.

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1 Introduction

Power consumption on TLV320ADCx120 devices is highly dependent on the usage scenario and features enabled on these devices. The following tables summarize the power consumption based on the following:

- Supply voltage
- Sampling Frequency (FS)
- Number of channels
- DRE enabled or disabled
- Decimation filter options
- Bit clock (BCLK) to Frame sync (FSYNC) ratio
- PLL enabled or disabled
- Converted word length

The tables report the average active current consumed on the Analog Supply, AVDD. This supply includes all the internal analog and digital circuits, but excludes the current consumed by the I/O pins due to its application dependencies. I/O power is dependent upon the following:

- Load capacitance of the system bus interface
- Data output clock rate
- Data conversion output activity
- Bus interface pullups or pulldowns
- Frequency of ADC commands sent by microprocessor

2 Target Mode Power Consumption With PLL Enabled

Table 2-1 describes the typical current consumption of the TLV320ADCx120 when the PLL is enabled with AVDD set to 1.8 V and 3.3 V. The PLL is enabled by:

- Setting the bit field PLL_PDZ in the PWR_CFG register
- Applying a FSYNC and BCLK with the desired sampling rate and BCLK to FSYNC ratio

In this table, when the DRE was enabled, the DRE threshold was set to -36 dB. The current consumption measurements had the Biquad Filters disabled and inputs grounded.

Table 2-1. Typical Current Consumption (PLL Enabled)

SAMPLING FREQUENCY (kHz)	ADC CHANNELS	DRE	DECIMATION FILTERS	BCLK RATIO	WORD LENGTH	AVDD CURRENT AT 3.3 V (mA)	AVDD CURRENT AT 1.8 V (mA)	
8	1	Disabled	Linear Phase	32	24	7.66	7.34	
	2			48		11.52	10.92	
				96		11.56	10.95	
16	1	Disabled	Linear Phase	24	24	7.84	7.56	
			Low Latency			7.91	7.63	
	2		Linear Phase	48		11.88	11.26	
			Low Latency			12.02	11.41	
	2		Linear Phase	96		11.88	11.27	
			Low Latency			12.02	11.41	
	1	Enabled	Linear Phase	24		8.11	7.84	
			Low Latency			8.19	7.91	
			2	Linear Phase		48	12.43	11.82
				Low Latency			12.57	11.95
			2	Linear Phase		96	12.43	11.82
				Low Latency			12.57	11.96
24	1	Disabled	Linear Phase	24	24	7.98	7.70	
			Low Latency			8.12	7.84	
	2		Linear Phase	48		12.08	11.47	
			Low Latency			12.36	11.73	
	2		Linear Phase	96		12.08	11.46	
			Low Latency			12.36	11.75	
	1	Enabled	Linear Phase	24		8.31	8.03	
			Low Latency			8.46	8.17	
			2	Linear Phase		48	12.84	12.23
				Low Latency			13.13	12.51
			2	Linear Phase		96	12.84	12.22
				Low Latency			13.12	12.51

Table 2-1. Typical Current Consumption (PLL Enabled) (continued)

SAMPLING FREQUENCY (kHz)	ADC CHANNELS	DRE	DECIMATION FILTERS	BCLK RATIO	WORD LENGTH	AVDD CURRENT AT 3.3 V (mA)	AVDD CURRENT AT 1.8 V (mA)			
32	1	Disabled	Linear Phase	24	24	8.10	7.82			
			Low Latency			8.10	7.82			
	2		Linear Phase	48		12.27	11.66			
			Low Latency			12.27	11.65			
			Linear Phase	96		12.25	11.67			
			Low Latency			12.28	11.66			
	1		Linear Phase	24		8.49	8.21			
			Low Latency			8.49	8.21			
	2		Linear Phase	48		13.16	12.53			
			Low Latency			13.15	12.53			
			Linear Phase	96		13.17	12.54			
			Low Latency			13.16	12.54			
48	1	Disabled	Linear Phase	24	24	8.39	8.10			
			Low Latency			8.29	8.01			
	2		Linear Phase	48		12.78	12.16			
			Low Latency			12.59	11.97			
			Linear Phase	96		12.81	12.19			
			Low Latency			12.62	12.00			
	1		Linear Phase	24		8.90	8.61			
			Low Latency			8.81	8.52			
	2		Linear Phase	48		14.18	13.55			
			Low Latency			13.99	13.37			
			Linear Phase	96		14.21	13.59			
			Low Latency			14.03	13.40			
96	1	Disabled	Linear Phase	24	24	9.45	9.16			
			Low Latency			9.26	8.97			
	2		Linear Phase	48		15.15	14.51			
			Low Latency			14.75	14.12			
			Linear Phase	96		15.23	14.59			
			Low Latency			14.83	14.20			
	1		Linear Phase	24		10.47	10.18			
			Low Latency			10.27	9.98			
	2		Linear Phase	48		17.13	16.49			
			Low Latency			16.74	16.10			
	192		1	Disabled		Linear Phase	24	24	9.96	9.67
						Low Latency			11.13	10.84
2		Linear Phase	48		15.80	15.16				
		Low Latency			18.12	17.47				
		Linear Phase	96		15.97	15.35				
		Low Latency			18.07	17.66				
1		Linear Phase	24		11.69	11.39				
		Low Latency			13.16	12.86				
384	1	Disabled	Linear Phase	24	24	11.53	11.24			

3 Target Mode Power Consumption with PLL Disabled

Table 3-1 describes the typical current consumption of the TLV320ADCx120 when the PLL is disabled with AVDD set to 1.8 V and 3.3 V. The PLL is disabled by:

- Clearing the bit field PLL_PDZ in the PWR_CFG register
- Applying a controller clock through BCLK, GPIO1, or the GPIx pins
 - If GPIO1 is configured as MCLK, setting the appropriate GPIO1_CFG bit field in the GPIO_CFG0 register
 - If GPIx is configured as MCLK, setting the appropriate GPIx_CFG bit field in the GPI_CFG0 register
- Indicating the controller clock source through DIS_PLL_SLV_CLK_SRC bit field in the CLK_SRC register
- Setting the appropriate MCLK to FSYNC ratio through the MCLK_RATIO_SEL bit field and MCLK_FREQ_SEL_MODE bit field of the CLK_SRC register
- Setting the AUTO_MODE_PLL_DIS bit field and the corresponding MCLK_FREQ_SEL bit field of the MST_CFG0 register

In this table, when the DRE was enabled, the DRE threshold was set to –36 dB. The power consumption measurements had the Biquad Filters disabled and inputs grounded.

Table 3-1. Typical Current Consumption (PLL Disabled)

SAMPLING FREQUENCY (kHz)	MCLK FREQUENCY (MHz)	MCLK RATIO	ADC CHANNELS	DRE	DECIMATION FILTERS	BCLK RATIO	WORD LENGTH	AVDD CURRENT AT 3.3 V (mA)	AVDD CURRENT AT 1.8 V (mA)	
8	12.288	1536	1	Disabled	Linear Phase	32	32	5.68	5.41	
			2			48	24	9.91	9.33	
16	12.288	768	1	Disabled	Linear Phase	24	24	5.67	5.59	
								Enabled	6.13	5.87
				Disabled	Low Latency			5.74	5.66	
								Enabled	6.20	5.94
				Disabled	Ultra-Low Latency			5.63	5.55	
								Enabled	5.90	5.83
			2	Linear Phase	48	Disabled		10.24	9.65	
						Disabled		10.38	9.79	
						Disabled		10.15	9.57	
						Enabled		6.16	5.83	
16	24.576	1536	1	Disabled	Linear Phase	24	24	6.24	6.11	
								Enabled	6.23	5.85
				Disabled	Low Latency			6.50	6.19	
								Enabled	6.16	5.79
				Disabled	Ultra-Low Latency			6.39	6.07	
								Enabled	10.58	9.91
			2	Linear Phase	48	Disabled		11.13	10.46	
						Enabled		10.72	9.97	
						Disabled		Low Latency	10.91	10.60
									Enabled	10.50
						Disabled		Ultra-Low Latency	11.05	10.37
									Enabled	10.59
			2	Linear Phase	96	Disabled		11.11	10.47	
						Enabled		10.73	10.06	
						Disabled		Low Latency	11.28	10.61
									Enabled	10.14
						Disabled		Ultra-Low Latency	10.70	10.38
									Enabled	

Table 3-1. Typical Current Consumption (PLL Disabled) (continued)

SAMPLING FREQUENCY (kHz)	MCLK FREQUENCY (MHz)	MCLK RATIO	ADC CHANNELS	DRE	DECIMATION FILTERS	BCLK RATIO	WORD LENGTH	AVDD CURRENT AT 3.3 V (mA)	AVDD CURRENT AT 1.8 V (mA)					
16	36.864	2304	1	Disabled	Linear Phase	24	24	6.46	6.21					
				Enabled				6.74	6.48					
				Disabled	Low Latency			6.53	6.17					
				Enabled				6.81	6.46					
				Disabled	Ultra-Low Latency			6.42	6.05					
				Enabled				6.70	6.35					
			2	Linear Phase	48	Disabled		10.89	10.09					
						Enabled		11.44	10.63					
				Disabled		Low Latency		11.03	10.23					
				Enabled				11.58	10.79					
				Disabled		Ultra-Low Latency		10.80	10.01					
				Enabled				11.35	10.59					
			2	Linear Phase	96	Disabled		10.90	10.09					
						Enabled		11.45	10.63					
				Disabled		Low Latency		11.04	10.25					
				Enabled				11.59	10.79					
				Disabled		Ultra-Low Latency		10.81	10.02					
				Enabled				11.36	10.56					
24	12.288	512	1	Disabled	Linear Phase	24	24	5.97	5.58					
				Enabled				6.31	5.93					
				Disabled	Low Latency			6.11	5.73					
				Enabled				6.28	6.07					
				Disabled	Ultra-Low Latency			5.93	5.54					
				Enabled				6.27	5.88					
			2	Linear Phase	96	Disabled		10.05	9.69					
						Ultra-Low Latency		64	32	10.35	9.56			
				Linear Phase		24		10.45	9.70					
				Ultra-Low Latency				10.32	9.62					
				1		Linear Phase		32	Disabled	Linear Phase	32	32	6.29	5.95
									Enabled				6.36	6.29
	Disabled	Low Latency	6.44		6.09									
	Enabled		6.52		6.43									
	Disabled	Ultra-Low Latency	6.25		5.91									
	Enabled		6.34		6.25									
	2	Linear Phase	64	Disabled	Linear Phase	64		10.77	10.11					
				Enabled				10.90	10.78					
Disabled		Low Latency		11.06	10.40									
Enabled				12.46	10.81									
Disabled		Ultra-Low Latency		10.32	10.02									
Enabled				10.84	10.49									
2		Linear Phase	128	Disabled	Linear Phase	128	10.79	10.12						
				Enabled			10.91	10.79						
		Disabled		Low Latency	11.07		10.41							
		Enabled			12.32		11.08							
		Disabled		Ultra-Low Latency	10.70		10.04							
		Enabled			10.86		10.70							
24	24.576	1024	1	Disabled	Linear Phase	32	32	6.29	5.95					
				Enabled				6.36	6.29					
				Disabled	Low Latency			6.44	6.09					
				Enabled				6.52	6.43					
				Disabled	Ultra-Low Latency			6.25	5.91					
				Enabled				6.34	6.25					
			2	Linear Phase	64	Disabled		Linear Phase	64	10.77	10.11			
						Enabled				10.90	10.78			
				Disabled		Low Latency		11.06		10.40				
				Enabled				12.46		10.81				
				Disabled		Ultra-Low Latency		10.32		10.02				
				Enabled				10.84		10.49				
			2	Linear Phase	128	Disabled		Linear Phase	128	10.79	10.12			
						Enabled				10.91	10.79			
				Disabled		Low Latency		11.07		10.41				
				Enabled				12.32		11.08				
				Disabled		Ultra-Low Latency		10.70		10.04				
				Enabled				10.86		10.70				

Table 3-1. Typical Current Consumption (PLL Disabled) (continued)

SAMPLING FREQUENCY (kHz)	MCLK FREQUENCY (MHz)	MCLK RATIO	ADC CHANNELS	DRE	DECIMATION FILTERS	BCLK RATIO	WORD LENGTH	AVDD CURRENT AT 3.3 V (mA)	AVDD CURRENT AT 1.8 V (mA)							
24	36.864	1536	1	Disabled	Linear Phase	24	24	6.58	6.20							
				Enabled				6.91	6.53							
				Disabled	Low Latency			6.72	6.35							
				Enabled				7.06	6.68							
				Disabled	Ultra-Low Latency			6.53	6.17							
				Enabled				6.87	6.50							
			2	Linear Phase	48			Disabled	11.09	10.26						
								Enabled	11.72	10.94						
				Disabled				Low Latency	11.37	10.58						
				Enabled					12.03	11.22						
				Disabled				Ultra-Low Latency	11.00	10.22						
				Enabled					11.45	10.89						
		32	12.288	384		1		Disabled	Linear Phase	24	24	6.05	5.65			
								Enabled				6.45	6.05			
								Disabled	Low Latency			6.05	5.65			
								Enabled				6.45	5.99			
								Disabled	Ultra-Low Latency			5.93	5.53			
								Enabled				6.33	5.93			
2	Linear Phase				48	Disabled	10.56	9.84								
							Ultra-Low Latency	9.79	9.36							
	Linear Phase					96	10.57	9.85								
							Ultra-Low Latency	10.33	9.61							
	24.576						768	1	1	Disabled		Linear Phase	24	24	6.40	5.96
										Enabled					6.81	6.37
Disabled		Low Latency	6.40	5.97												
Enabled			6.81	6.38												
Disabled		Ultra-Low Latency	6.29	5.86												
Enabled			6.69	6.27												
2		Linear Phase	48	Disabled	10.97	10.02										
					Enabled	11.76		10.80								
		Disabled		Low Latency	10.73	10.04										
		Enabled			11.59	10.82										
		Disabled		Ultra-Low Latency	10.73	9.82										
		Enabled			11.52	10.60										
24.576	768	768	2	Linear Phase	96	96	24	10.98	10.03							
								Enabled	11.77	10.82						
				Disabled				Low Latency	10.98	10.06						
				Enabled					11.76	10.84						
				Disabled				Ultra-Low Latency	10.74	9.82						
				Enabled					10.27	10.61						

Table 3-1. Typical Current Consumption (PLL Disabled) (continued)

SAMPLING FREQUENCY (kHz)	MCLK FREQUENCY (MHz)	MCLK RATIO	ADC CHANNELS	DRE	DECIMATION FILTERS	BCLK RATIO	WORD LENGTH	AVDD CURRENT AT 3.3 V (mA)	AVDD CURRENT AT 1.8 V (mA)			
48	12.288	256	1	Disabled	Linear Phase	24	24	6.37	5.99			
					Low Latency			6.27	5.89			
					Ultra-Low Latency			6.10	5.72			
	Enabled	Linear Phase		32	6.70	6.35						
		Low Latency			7.22	6.87						
		Ultra-Low Latency			6.60	6.26						
	Disabled	Linear Phase	64		6.43	6.09						
		Low Latency			6.95	6.61						
		Ultra-Low Latency			11.48	10.82						
	24.576	512	2	Disabled	Linear Phase	64	32	11.30	10.63			
					Low Latency			10.95	10.28			
					Ultra-Low Latency			11.51	10.85			
Enabled					Linear Phase	128		11.33	10.66			
					Low Latency			10.98	10.31			
					Ultra-Low Latency			6.78	6.72			
48	36.864	768	1	Disabled	Linear Phase	24	24	7.28	7.24			
					Low Latency			6.71	6.63			
					Ultra-Low Latency			7.26	7.14			
				Enabled	Linear Phase			48	6.55	6.45		
					Low Latency				7.09	6.97		
					Ultra-Low Latency				11.34	11.21		
			Disabled	Linear Phase	96	12.37			12.22			
				Low Latency		11.20			11.02			
				Ultra-Low Latency		12.21			12.03			
				Enabled		Linear Phase		24	10.87	10.68		
						Low Latency			11.88	11.68		
						Ultra-Low Latency			11.36	11.23		
	24.576	256	384	1	Disabled	Linear Phase	32	32	12.37	12.24		
						Low Latency			11.22	11.04		
						Ultra-Low Latency			12.23	12.05		
					Enabled	Linear Phase			24	10.89	10.70	
						Low Latency				11.88	11.70	
						Ultra-Low Latency				7.80	7.45	
		36.864	384	2	Disabled	Linear Phase	48			24	7.60	7.25
						Low Latency					7.25	6.90
						Ultra-Low Latency					7.83	7.80
						Enabled	Linear Phase		24		8.85	8.83
							Low Latency				7.68	7.60
							Ultra-Low Latency				8.70	8.63
96	36.864	384	2	Disabled	Linear Phase	48	24	7.34	7.26			
					Low Latency			8.37	8.28			
					Ultra-Low Latency			13.25	13.17			
				Enabled	Linear Phase			48	12.94		12.76	
					Low Latency				12.25		12.08	
					Ultra-Low Latency							

4 Digital Microphone Power Consumption

Table 4-1 and Table 4-2 describes the typical current consumption of the TLV320ADCx120 when the digital microphone inputs are used with an external PDM modulator 4th and 5th order, respectively. The Digital Microphone is selected by:

- Configuring the corresponding channel for digital microphone input in the CHx_INSRC register
- Configuring the corresponding GPO1 or GPIO1 pin as PDMCLK output in the GPO_CFG0 or GPIO_CFG0 register, respectively.
- Configuring the corresponding GPIx or GPIO1 pin as PDM input in the GPI_CFG0 or GPIO_CFG0 register, respectively

Table 4-1. PDM Typical Current Consumption With an External PDM 4th Order Modulator

PDM CLOCK		6.144 MHz	3.072 MHz	1.536 MHz	0.768 MHz
SAMPLING RATE (kHz)	DIGITAL MICROPHONE CHANNELS	AVDD CURRENT AT 3.3 V (mA)	AVDD CURRENT AT 3.3 V (mA)	AVDD CURRENT AT 3.3 V (mA)	AVDD CURRENT AT 3.3 V (mA)
8	2	3.81	3.70	3.70	3.70
	4	-	4.57	4.56	4.56
16	2	4.14	4.04	4.04	4.03
	4	-	5.16	5.16	5.15
24	2	4.31	4.21	4.21	-
	4	-	5.49	5.48	-
32	2	4.49	4.40	4.40	-
	4	-	5.84	5.84	-
48	2	5.00	4.90	4.91	-
	4	-	7.06	7.07	-
96	2	7.38	7.28	7.32	-
	4	-	10.80	10.86	-
192	2	8.17	8.01	7.98	-
	4	-	11.65	11.62	-

Table 4-2. PDM Typical Current Consumption With an External PDM 5th Order Modulator

PDM CLOCK		6.144 MHz	3.072 MHz	1.536 MHz	0.768 MHz
SAMPLING RATE (kHz)	DIGITAL MICROPHONE CHANNELS	AVDD CURRENT AT 3.3 V (mA)	AVDD CURRENT AT 3.3 V (mA)	AVDD CURRENT AT 3.3 V (mA)	AVDD CURRENT AT 3.3 V (mA)
8	2	3.80	3.71	3.70	3.70
	4	-	4.56	4.57	4.56
16	2	4.13	4.05	4.04	4.03
	4	-	5.17	5.16	5.15
24	2	4.29	4.22	4.21	-
	4	-	5.48	5.49	-
32	2	4.50	4.40	4.40	-
	4	-	5.84	5.84	-
48	2	4.99	4.90	4.91	-
	4	-	7.07	7.08	-
96	2	7.37	7.30	7.33	-
	4	-	10.83	10.85	-
192	2	8.18	8.00	7.97	-
	4	-	11.66	11.58	-

5 Settings for Lowest Power Consumption

To minimize the power consumption of the TLV320ADCx120 devices, ensure that unused modules are disabled, use the lowest sampling rate, bit clock, and controller clock needed by the application, and operate at the lowest AVDD and IOVDD supply voltage possible. The following list summarizes the settings and registers for lowest power operation:

- Operate at the lowest supply voltage possible. AVDD and IOVDD support 1.8-V or 3.3-V supply, independently (AVDD and IOVDD can have different supply voltages).
 - Unused analog inputs, tie to analog ground.
 - Unused digital inputs, tie to digital ground.
 - Unused outputs, leave unconnected.
- Disable unused ADC and PDM channels through the IN_CH_EN register.
- Disable any unused output channel through the ASI_OUT_CH_EN register.
- Disable MICBIAS power, if unused, through the PWR_CFG register.
- Operate at the lowest sample rate possible.
- Disable PLL, if the system supplies a low jitter controller clock. Refer to [Section 3](#) for a description of the settings to disable PLL.
- Disable unused post-processing blocks:
 - Disable Biquad filters, if unused, through the BIQUAD_CFG bit field of the DSP_CFG1 register.
 - Disable DRE, AGC or DRC, if unused in an active channel, through the CHx_DREEN bit field of the CHx_CFG0 register.
- Select ultra-low latency over linear phase decimation filters, if the application allows, through the DECI_FILT bit field of the DSP_CFG0 register.
- Utilize the smallest word length allowed by the application through the ASI_WLEN bit field of the ASI_CFG0 register.

6 Related Documentation

For related documentation see the following:

- TLV320ADC6120
 - Texas Instruments, [TLV320ADC6120 2-Channel, 768-kHz, Burr-Brown™ Audio ADC data sheet](#)
 - Texas Instruments, [TLV320ADC6120 stereo-channel, 768-kHz, Burr-Brown™ audio ADC with 106-dB SNR evaluation module](#)
- TLV320ADC5120
 - Texas Instruments, [TLV320ADC5120 2-Channel, 768-kHz, Burr-Brown™ Audio ADC data sheet](#)
 - Texas Instruments, [TLV320ADC5120 stereo-channel, 768-kHz, Burr-Brown™ audio ADC with 106-dB SNR evaluation module](#)
- TLV320ADC3120
 - Texas Instruments, [TLV320ADC3120 2-Channel, 768-kHz, Burr-Brown™ Audio ADC data sheet](#)
 - Texas Instruments, [TLV320ADC3120 stereo-channel, 768-kHz, Burr-Brown™ audio ADC with 106-dB SNR evaluation module](#)
- Texas Instruments, [ADCx120EVM-PDK User's Guide](#)
- Texas Instruments, [PurePath™ Console](#)

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