

# Configuring and Operating TLV320ADCx120 as Audio Bus Controller



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Precision ADC

## ABSTRACT

The TLV320ADCx120 is a family of dual-channel audio analog-to-digital converters. This device family features a flexible audio serial interface that allows the device to be configured as either a controller or target. This document describes the modes, input parameters, and register coefficients required to configure the TLV320ADCx120 devices as an audio bus controller.

## Table of Contents

<b>Note</b> .....	1
<b>1 Introduction</b> .....	2
<b>2 Controller Mode</b> .....	2
2.1 Controller Mode Configuration Options.....	2
<b>3 Edge Sync for I<sup>2</sup>S and LJF in Controller Mode</b> .....	7
3.1 I <sup>2</sup> S and LJF Standard Bus Formats.....	7
3.2 Support for Non-Standard I <sup>2</sup> S and LJF Bus Formats.....	7
<b>4 Related Documentation</b> .....	9

## List of Figures

Figure 3-1. Default I <sup>2</sup> S Format in Controller Mode (TX_OFFSET = 0).....	7
Figure 3-2. Default LJF Format in Controller Mode (TX_OFFSET = 0).....	7
Figure 3-3. Custom I <sup>2</sup> S Format in Controller Mode (TX_OFFSET = 0).....	8
Figure 3-4. Custom LJF Format in Controller Mode (TX_OFFSET = 0).....	8

## List of Tables

Table 2-1. MCLK Frequency Selection Mode With Supported Frequencies or Ratios.....	2
Table 2-2. Required Input Parameters for Controller mode Auto Clock Configuration with PLL Enabled.....	3
Table 2-3. Supported FSYNC (Multiples or Sub-multiples of 48 kHz) and BCLK Frequencies.....	3
Table 2-4. Supported FSYNC (Multiples or Sub-multiples of 44.1 kHz) and BCLK Frequencies.....	3
Table 2-5. Required Input Parameters for Controller Mode Auto Clock Configuration With PLL Disabled.....	4
Table 2-6. Supported Sample Rates for Auto Clock Configuration With PLL Disabled.....	4

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## Note

TI is transitioning to use more inclusive terminology. Some language may be different than what you would expect to see for certain technology areas.

## 1 Introduction

The TLV320ADCx120 is a family of dual-channel audio analog to digital converters. This device family features a flexible audio serial interface that allows the device to be configured as either a controller or target.

This document describes the modes, input parameters, and register coefficients required to configure the TLV320ADCx120 devices as an audio bus controller.

## 2 Controller Mode

For I<sup>2</sup>S-based digital audio communication protocols, the controller device generates the clocks: bit clock (BCLK) and word clock (WCLK) (or frame synchronization, FSYNC). On the other hand, a target device receives the clocks: BCLK and WCLK (or FSYNC) from an external device. In many applications, a host processor with an advanced digital audio interface can act as the audio bus controller with the TLV320ADCx120 as a target device. However, having the audio ADC as the audio bus controller is advantageous in the following circumstances:

- The host processor or DSP cannot output or generate standard audio clocks. A standard audio clock is an integer multiple of the sample rate that generates the necessary audio serial interface (ASI) FSYNC and BCLK clocks. In this case, an external PLL multiplier generates the appropriate audio clocks.
- To easily synchronize multiple TLV320ADCx120 devices for simultaneous recording across all channels and devices. In this case, one TLV320ADCx120 device is configured as a controller to generate low jitter ASI clocks.
- The host does not have a flexible ASI bus to generate system required audio clocks, but allows these clocks as input when configured as a target device.

The following sections describe the modes, input parameters, or register settings required to configure the device as an audio bus controller.

### 2.1 Controller Mode Configuration Options

The TLV320ADCx120 supports two functional modes when configured as an ASI controller:

- **Auto Clock Generation with Internal PLL enabled.** Enabling the PLL allows the auto clock generator engine to generate a system clock that can be greater than the provided MCLK.
- **Auto Clock Generation with internal PLL disabled.** Disabling the PLL limits the system clock to the MCLK frequency.

The system clock feeds the decimation filters and all the digital signal processing blocks (biquad filters, digital volume control, high pass filters, and so forth). Disabling the PLL limits the amount of digital signal processing available. However, with the low jitter PLL disabled, the performance of the ADC can be degraded based on the jitter from the external clock source. For devices configured as controller mode in high-performance applications, the recommended operating mode is to enable the PLL.

Configuring the TLV320ADCx120 as an ASI controller requires that GPIO1 be configured as the MCLK input in GPIO\_CFG0 (page 0, register 0x21, Bits 7-4). The frequency of MCLK must be one of the supported frequencies or ratios supported by configuring the MCLK\_FREQ\_SEL frequency selection mode (page 0, MST\_CFG0 register 0x13, Bits 2-0), as shown in [Table 2-1](#). Note that when using auto clock generation with internal PLL disabled, MCLK\_RATIO\_SEL (page 0, CLK\_SRC register 0x16, bits 5-3) must also be configured.

**Table 2-1. MCLK Frequency Selection Mode With Supported Frequencies or Ratios**

MCLK FREQUENCY SELECTION MODE	SUPPORTED FREQUENCIES OR RATIOS
MCLK_FREQ_SEL (page 0, MST_CFG0 register 0x13, bits 2-0)	12 MHz, 12.288 MHz, 13 MHz, 16 MHz, 19.2 MHz, 19.68 MHz, 24 MHz, 24.576 MHz
MCLK_RATIO_SEL (page 0, CLK_SRC register 0x16, bits 5-3)	64, 256, 384, 512, 768, 1024, 1536, 2304

### 2.1.1 Auto Clock Configuration With PLL Enabled

The auto clock configuration engine requires four user-provided parameters to generate the proper ASI clocks when the device is configured in controller mode, as shown in [Table 2-2](#).

**Table 2-2. Required Input Parameters for Controller mode Auto Clock Configuration with PLL Enabled**

USER-PROVIDED PARAMETER	REGISTER
MCLK Frequency	Page 0, MST_CFG0 Register 0x13, bits 2-0
Sampling Rate (F <sub>S</sub> ) mode (multiple of 48 kHz or 44.1 kHz)	Page 0, MST_CFG0 Register 0x13, Bit 3
FS_RATE	Page 0, MST_CFG1 Register 0x14, Bits 7-4
FSYNC-to-BCLK Ratio	Page 0, MST_CFG1 Register 0x14, Bits 3-0

#### 2.1.1.1 Supported Sample-Rates

The supported sample-rates and BCLK to FSYNC ratios for multiples and sub-multiples of 48 kHz are shown in [Table 2-3](#).

**Table 2-3. Supported FSYNC (Multiples or Sub-multiples of 48 kHz) and BCLK Frequencies**

BCLK-TO- FSYNC RATIO	BCLK (MHz)								
	FSYNC (8 kHz)	FSYNC (16 kHz)	FSYNC (24 kHz)	FSYNC (32 kHz)	FSYNC (48 kHz)	FSYNC (96 kHz)	FSYNC (192 kHz)	FSYNC (384 kHz)	FSYNC (768 kHz)
16	Reserved	0.256	0.384	0.512	0.768	1.536	3.072	6.144	12.288
24	Reserved	0.384	0.576	0.768	1.152	2.304	4.608	9.216	18.432
32	0.256	0.512	0.768	1.024	1.536	3.072	6.144	12.288	24.576
48	0.384	0.768	1.152	1.536	2.304	4.608	9.216	18.432	Reserved
64	0.512	1.024	1.536	2.048	3.072	6.144	12.288	24.576	Reserved
96	0.768	1.536	2.304	3.072	4.608	9.216	18.432	Reserved	Reserved
128	1.024	2.048	3.072	4.096	6.144	12.288	24.576	Reserved	Reserved
192	1.536	3.072	4.608	6.144	9.216	18.432	Reserved	Reserved	Reserved
256	2.048	4.096	6.144	8.192	12.288	24.576	Reserved	Reserved	Reserved
384	3.072	6.144	9.216	12.288	18.432	Reserved	Reserved	Reserved	Reserved
512	4.096	8.192	12.288	16.384	24.576	Reserved	Reserved	Reserved	Reserved
1024	8.192	16.384	24.576	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
2048	16.384	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

The supported sample-rates and BCLK/FSYNC ratios for multiples and sub-multiples of 44.1kHz are shown in [Table 2-4](#).

**Table 2-4. Supported FSYNC (Multiples or Sub-multiples of 44.1 kHz) and BCLK Frequencies**

BCLK-TO- FSYNC RATIO	BCLK (MHz)								
	FSYNC (7.35 kHz)	FSYNC (14.7 kHz)	FSYNC (22.05 kHz)	FSYNC (29.4 kHz)	FSYNC (44.1 kHz)	FSYNC (88.2 kHz)	FSYNC (176.4 kHz)	FSYNC (352.8 kHz)	FSYNC (705.6 kHz)
16	Reserved	Reserved	0.3528	0.4704	0.7056	1.4112	2.8224	5.6448	11.2896
24	Reserved	0.3528	0.5292	0.7056	1.0584	2.1168	4.2336	8.4672	16.9344
32	Reserved	0.4704	0.7056	0.9408	1.4112	2.8224	5.6448	11.2896	22.5792
48	0.3528	0.7056	1.0584	1.4112	2.1168	4.2336	8.4672	16.9344	Reserved
64	0.4704	0.9408	1.4112	1.8816	2.8224	5.6448	11.2896	22.5792	Reserved
96	0.7056	1.4112	2.1168	2.8224	4.2336	8.4672	16.9344	Reserved	Reserved
128	0.9408	1.8816	2.8224	3.7632	5.6448	11.2896	22.5792	Reserved	Reserved
192	1.4112	2.8224	4.2336	5.6448	8.4672	16.9344	Reserved	Reserved	Reserved
256	1.8816	3.7632	5.6448	7.5264	11.2896	22.5792	Reserved	Reserved	Reserved
384	2.8224	5.6448	8.4672	11.2896	16.9344	Reserved	Reserved	Reserved	Reserved
512	3.7632	7.5264	11.2896	15.0528	22.5792	Reserved	Reserved	Reserved	Reserved

**Table 2-4. Supported FSYNC (Multiples or Sub-multiples of 44.1 kHz) and BCLK Frequencies (continued)**

BCLK-TO-FSYNC RATIO	BCLK (MHz)								
	FSYNC (7.35 kHz)	FSYNC (14.7 kHz)	FSYNC (22.05 kHz)	FSYNC (29.4 kHz)	FSYNC (44.1 kHz)	FSYNC (88.2 kHz)	FSYNC (176.4 kHz)	FSYNC (352.8 kHz)	FSYNC (705.6 kHz)
1024	7.5264	15.0528	22.5792	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
2048	15.0528	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

### 2.1.1.2 Example 12-MHz MCLK

For a 12-MHz MCLK, the following I<sup>2</sup>C script configures the TLV320ADCx120 as controller mode with GPIO1 as MCLK input for a 44.1-kHz or 48-kHz sampling rate:

```
w 9C 21 a0 # configure GPIO1 as MCLK input w 9C 13 80 # configure device as mcontrollerwith MCLK =
12 MHz w 9C 14 48 # FS = 44.1/48k BCLK/ratio = 256
```

### 2.1.2 Auto Clock Detect With PLL Disabled

For the lowest power consumption, it can be desirable to disable the PLL and derive all clocks directly from MCLK. To disable the PLL in auto configuration mode, set bit 5 (AUTO\_MODE\_PLL\_DIS) in MST\_CFG0 (page 0, register 0x13). The required inputs for this mode are found in [Table 2-5](#).

**Table 2-5. Required Input Parameters for Controller Mode Auto Clock Configuration With PLL Disabled**

USER-PROVIDED PARAMETER	REGISTER
FS MODE	Page 0, MST_CFG0 Register 0x13, Bit 3
FS_RATE	Page 0, MST_CFG1 Register 0x14, Bits 7-4
FS_BCLK_RATIO	Page 0, MST_CFG1 Register 0x14, Bits 3-0
MCLK_FREQ_SEL_MODE	Page 0, CLK_SRC Register 0x16, Bit 6
MCLK_RATIO_SEL	Page 0, CLK_SRC Register 0x16, Bits 5-3

#### 2.1.2.1 Supported Sample-Rates

[Table 2-6](#) shows the supported sample-rates with the PLL disabled. As shown in [Table 2-6](#), higher MCLK ratios allow the use of greater number or greater computation of digital processing blocks due to the greater availability of clocks in the system.

**Table 2-6. Supported Sample Rates for Auto Clock Configuration With PLL Disabled**

SAMPLING FREQUENCY (kHz)	MCLK FREQUENCY(MHz)	MCLK RATIO	ADC CHANNELS	DRE	DECIMATION FILTERS	BCLK RATIO	WORD LENGTH	
8	12.288	1536	1	Disabled	Linear Phase	32	32	
					Low Latency			
					Ultra-Low Latency			
			2		Linear Phase	48		24
					Low Latency			
					Ultra-Low Latency			
16	12.288	768	1	Disabled	Linear Phase	24	24	
				Enabled				
				Disabled	Low Latency			
				Enabled				
				Disabled	Ultra-Low Latency			
			Enabled	Ultra-Low Latency				
			2	Disabled	Linear Phase	48		24
					Low Latency			
					Ultra-Low Latency			

**Table 2-6. Supported Sample Rates for Auto Clock Configuration With PLL Disabled (continued)**

SAMPLING FREQUENCY (kHz)	MCLK FREQUENCY(MHz)	MCLK RATIO	ADC CHANNELS	DRE	DECIMATION FILTERS	BCLK RATIO	WORD LENGTH			
16	24.576	1536	1	Disabled	Linear Phase	24	24			
				Enabled						
				Disabled	Low Latency					
				Enabled						
				Disabled	Ultra-Low Latency					
				Enabled						
			2	Disabled	Linear Phase	48				
				Enabled						
				Disabled	Low Latency					
				Enabled						
Disabled	Ultra-Low Latency									
Enabled										
16	36.864	2304	1	Disabled	Linear Phase	24	24			
				Enabled						
				Disabled	Low Latency					
				Enabled						
				Disabled	Ultra-Low Latency					
				Enabled						
			2	Disabled	Linear Phase	48				
				Enabled						
				Disabled	Low Latency					
				Enabled						
Disabled	Ultra-Low Latency									
Enabled										
24	12.288	512	1	Disabled	Linear Phase	32	32			
				Enabled						
				Disabled	Low Latency					
				Enabled						
				Disabled	Ultra-Low Latency					
				Enabled						
			2	Disabled	Linear Phase			64		
				Enabled						
	24	24.576	1024	1	Disabled	Linear Phase			32	32
					Enabled					
					Disabled	Low Latency				
					Enabled					
					Disabled	Ultra-Low Latency				
					Enabled					
2	Disabled			Linear Phase	64					
	Enabled									
	Disabled			Low Latency						
	Enabled									
	Disabled			Ultra-Low Latency						
	Enabled									
24	36.864	1536	1	Disabled	Linear Phase	24	24			
				Enabled						
				Disabled	Low Latency					
				Enabled						
				Disabled	Ultra-Low Latency					
				Enabled						
				2	Disabled			Linear Phase	48	
					Enabled					
			Disabled		Low Latency					
			Enabled							
			Disabled		Ultra-Low Latency					
			Enabled							

**Table 2-6. Supported Sample Rates for Auto Clock Configuration With PLL Disabled (continued)**

SAMPLING FREQUENCY (kHz)	MCLK FREQUENCY(MHz)	MCLK RATIO	ADC CHANNELS	DRE	DECIMATION FILTERS	BCLK RATIO	WORD LENGTH		
32	12.288	384	1	Disabled	Linear Phase	24	24		
				Enabled					
				Disabled	Low Latency				
			Enabled						
			Disabled	Ultra-Low Latency					
			Enabled						
	2	24.576	768	2	Disabled	Linear Phase		48	
					Enabled	Ultra-Low Latency			
					Disabled	Linear Phase		24	
	Enabled			Low Latency					
	Disabled			Ultra-Low Latency					
	Enabled								
2	24.576	768	2	Disabled	Linear Phase	48			
				Enabled	Low Latency				
				Disabled	Ultra-Low Latency				
			Enabled	Linear Phase					
			Disabled	Low Latency					
			Enabled	Ultra-Low Latency					
48	12.288	256	1	Disabled	Linear Phase	32	32		
				Enabled	Low Latency				
				Enabled	Ultra-Low Latency				
				Disabled	Linear Phase	32			
				Enabled	Low Latency				
				Disabled	Ultra-Low Latency				
	Enabled	Linear Phase	64						
	Disabled	Low Latency							
	Enabled	Ultra-Low Latency							
	2	24.576	512	2	Disabled	Linear Phase	48		
					Enabled	Low Latency			
					Disabled	Ultra-Low Latency			
Enabled				Linear Phase					
Disabled				Low Latency					
Enabled				Ultra-Low Latency					
48	36.864	768	1	Disabled	Linear Phase	24	24		
				Enabled	Low Latency				
				Disabled	Ultra-Low Latency				
			Enabled	Linear Phase	48				
			Disabled	Low Latency					
			Disabled	Ultra-Low Latency					
	Enabled	Linear Phase	48						
	Disabled	Low Latency							
	Enabled	Ultra-Low Latency							
	96	24.576	256	1	Disabled	Linear Phase		32	32
					Enabled	Low Latency			
					Enabled	Ultra-Low Latency			
Disabled					Linear Phase	24			
Enabled					Low Latency				
Disabled					Ultra-Low Latency				
Enabled		Linear Phase	48						
Disabled		Low Latency							
Enabled		Ultra-Low Latency							
2		36.864	384	2	Disabled	Linear Phase	48		
					Enabled	Low Latency			
					Disabled	Ultra-Low Latency			
	Enabled			Linear Phase					
	Disabled			Low Latency					
	Enabled			Ultra-Low Latency					

### 2.1.2.2 Example

For a 24.576-MHz or 22.579-MHz MCLK, the following I<sup>2</sup>C script configures the TLV320ADCx120 as controller mode with GPIO1 as MCLK input for the 48-kHz or 44.1-kHz sampling rate, respectively:

```
w 9C 13 a0 # enable controller mode, disable PLL for auto-clock config
w 9C 14 48 # FS = 44.1/48k
BCLK/fsync ratio = 256
w 9C 16 d8 # MCLK is audio root, use MCLK_ratio_sel, MCLK/Fsync ratio = 512
w 9C 21 a0 # configure GPIO1 as MCLK input
```

## 3 Edge Sync for I<sup>2</sup>S and LJF in Controller Mode

In controller mode, TLV320ADCx120 supports the standard I<sup>2</sup>S and LJF bus formats, as well as, non-standard formats. Configurable polarity for BCLK and FSYNC and delay on transmit edge allow support for other non-standard formats.

### 3.1 I<sup>2</sup>S and LJF Standard Bus Formats

In standard I<sup>2</sup>S and LJF bus formats, the FSYNC edge is synchronous to the falling edge of BCLK. Figure 3-1 and Figure 3-2 show the timing diagrams supported by TLV320ADCx120 in I<sup>2</sup>S and LJF mode, respectively.

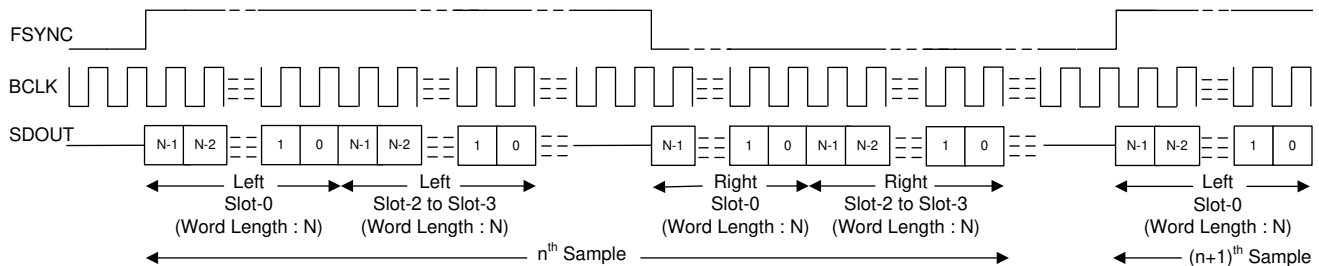


Figure 3-1. Default I<sup>2</sup>S Format in Controller Mode (TX\_OFFSET = 0)

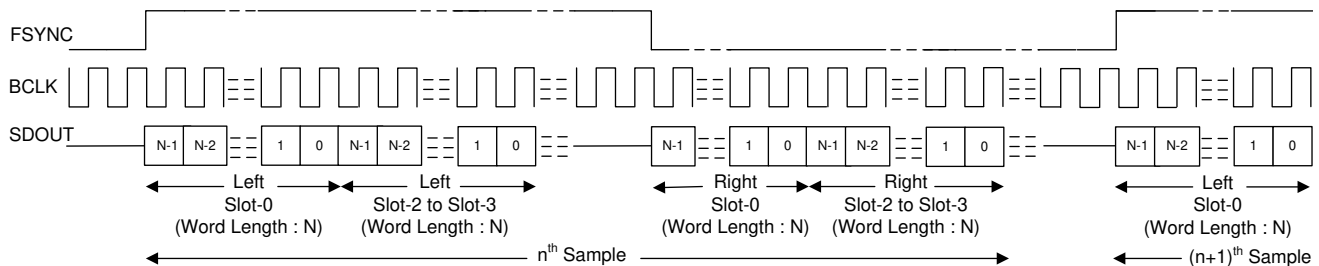


Figure 3-2. Default LJF Format in Controller Mode (TX\_OFFSET = 0)

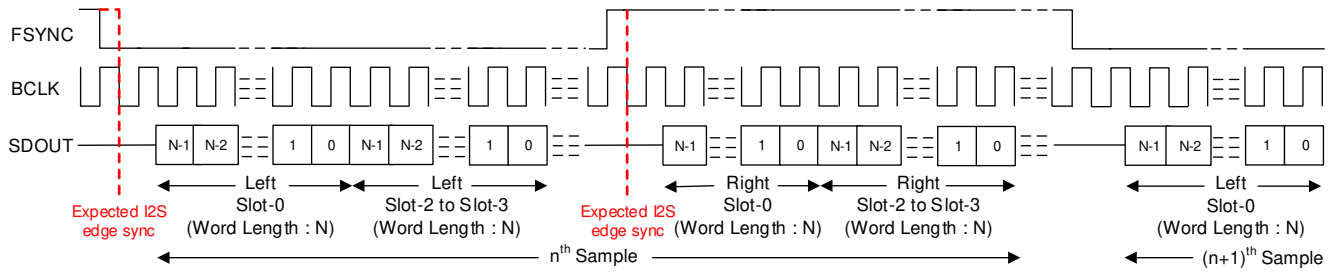
### 3.2 Support for Non-Standard I<sup>2</sup>S and LJF Bus Formats

TLV320ADCx120 devices can also support non-standard I<sup>2</sup>S and LJF bus formats through the configurable option in the following registers:

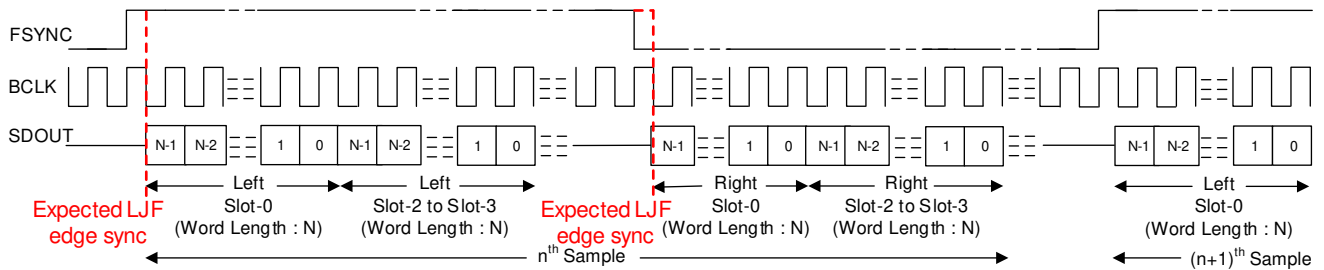
- BCLK\_POL (Page 0, ASI\_CFG0 Register 0x07, Bit 2)
- TX\_EDGE (Page 0, ASI\_CFG0 Register 0x07, Bit 1)
- FSYNC\_POL (Page 0, ASI\_CFG0 Register 0x07, Bit 3)
- TX\_OFFSET (Page 0, ASI\_CFG1 Register 0x08, Bit 4-0)
- INV\_BCLK\_FOR\_FSYNC (Page 0, CLK\_SRC Register 0x16, Bit 1)

Figure 3-3 and Figure 3-4 depict examples for the non-standard I<sup>2</sup>S and LJF bus formats that can be achieved using the following register settings:

- BCLK\_POL (Page 0, ASI\_CFG0 Register 0x07, Bit 2) = 1
- TX\_EDGE (Page 0, ASI\_CFG0 Register 0x07, Bit 1) = 1



**Figure 3-3. Custom I<sup>2</sup>S Format in Controller Mode (TX\_OFFSET = 0)**



**Figure 3-4. Custom LJF Format in Controller Mode (TX\_OFFSET = 0)**



## 4 Related Documentation

For related documentation see the following:

- TLV320ADC6120
  - Texas Instruments, [TLV320ADC6120 2-Channel, 768-kHz, Burr-Brown™ Audio ADC data sheet](#)
  - Texas Instruments, [TLV320ADC6120 stereo-channel, 768-kHz, Burr-Brown™ audio ADC with 106-dB SNR evaluation module](#)
- TLV320ADC5120
  - Texas Instruments, [TLV320ADC5120 2-Channel, 768-kHz, Burr-Brown™ Audio ADC data sheet](#)
  - Texas Instruments, [TLV320ADC5120 stereo-channel, 768-kHz, Burr-Brown™ audio ADC with 106-dB SNR evaluation module](#)
- TLV320ADC3120
  - Texas Instruments, [TLV320ADC3120 2-Channel, 768-kHz, Burr-Brown™ Audio ADC data sheet](#)
  - Texas Instruments, [TLV320ADC3120 stereo-channel, 768-kHz, Burr-Brown™ audio ADC with 106-dB SNR evaluation module](#)
- Texas Instruments, [ADCx120EVM-PDK User's Guide](#)
- Texas Instruments, [PurePath™ Console](#)

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