Application Report

PCM6xx0-Q1 Power Consumption Matrix Across Various Usage Scenario

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ABSTRACT

This application report details the power consumption of PCM6xx0 devices across various usage scenarios.

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Trademarks

1 Introduction

Power consumption on PCM6xx0 devices is highly dependent on the usage scenario and features enabled on these devices. The following tables summarize the power consumption based on the following:

- Supply voltage
- Sampling Frequency (FS)
- Number of channels
- Decimation filter options
- Bit clock (BCLK) to Frame sync (FSYNC) ratio
- PLL enabled or disabled
- Converted word length

The tables report the average active current consumed on the Analog Supply, AVDD. This supply includes all the internal analog and digital circuits, but excludes the current consumed by the I/O pins due to its application dependencies. I/O power is dependent upon the following:

- Load capacitance of the system bus interface
- Data output clock rate
- Data conversion output activity
- Bus interface pullups or pull downs
- Frequency of ADC commands sent by microprocessor

2 Slave Mode Power Consumption with PLL Enabled

Typical Current Consumption (PLL Enabled) describes the typical current consumption of the PCM6xx0 when the PLL is enabled with AVDD set to 3.3 V. The PLL is enabled by:

- Setting the bitfield PLL_PDZ in the PWR_CFG register
- Applying a FSYNC and BCLK with the desired sampling rate and BCLK to FSYNC ratio

The current consumption measurements had the AGC and the Biquad Filters disabled.

Table 2-1. Typical Current Consumption (PLL Enabled)

SAMPLING FREQUENCY (kHz)	ADC CHANNELS	DECIMATION FILTERS	BCLK RATIO	WORD LENGTH	AVDD CURRENT AT 3.3 V (mA)
8	1	Linear Phase	32	32	10.65
		Low Latency			8.56
	2	Linear Phase	48	24	14.40
		Low Latency			13.72
	3	Linear Phase	96		16.88
		Low Latency			18.04
	4	Linear Phase			22.09
		Low Latency			21.98
	5	Linear Phase	144		25.79
		Low Latency			27.70
	6	Linear Phase			31.14
		Low Latency			30.84
16	1	Linear Phase	24	24	10.59
		Low Latency			9.65
	2	Linear Phase	48		12.85
		Low Latency			13.27
	3	Linear Phase	96		19.09
		Low Latency			17.37
	4	Linear Phase			24.03
		Low Latency			23.92
	5	Linear Phase	144		28.69
		Low Latency			27.88
	6	Linear Phase			30.93
		Low Latency			31.40
24	1	Linear Phase	24	24	9.14
		Low Latency			8.89
	2	Linear Phase	48		14.38
		Low Latency			14.39
	3	Linear Phase	96		19.43
		Low Latency			18.09
	4	Linear Phase			21.81
		Low Latency			22.50
	5	Linear Phase	144		28.65
		Low Latency			27.32
	6	Linear Phase			32.91

Table 2-1. Typical Current Consumption (PLL Enabled) (continued)

SAMPLING FREQUENCY (kHz)	ADC CHANNELS	DECIMATION FILTERS	BCLK RATIO	WORD LENGTH	AVDD CURRENT AT 3.3 V (mA)
32	1	Linear Phase	24	24	10.56
		Low Latency			10.24
	2	Linear Phase	48		13.17
		Low Latency			14.42
	3	Linear Phase	96		17.66
		Low Latency			19.77
	4	Linear Phase			22.82
		Low Latency			22.32
	5	Linear Phase	144		29.09
		Low Latency			27.23
	6	Linear Phase			33.62
		Low Latency			31.98
48	1	Linear Phase	24	24	10.07
		Low Latency			11.01
	2	Linear Phase	48		14.92
		Low Latency			15.15
	3	Linear Phase	96		18.69
		Low Latency			19.58
	4	Linear Phase			24.22
		Low Latency			25.25
	5	Linear Phase	144		28.49
		Low Latency			28.65
	6	Linear Phase			34.32
		Low Latency			33.56
44.1	1	Linear Phase	24	24	8.72
	2	Linear Phase	48		15.17
	3	Linear Phase	96		20.04
	4	Linear Phase			25.28
	5	Linear Phase	144		28.05
	6	Linear Phase			34.10
96	1	Linear Phase	24	24	12.00
		Low Latency			12.45
	2	Linear Phase	48		16.58
		Low Latency			17.39
	3	Linear Phase	96		22.11
		Low Latency			21.35
	4	Linear Phase			29.42
		Low Latency			26.91
192	1	Linear Phase	24	24	11.29
		Low Latency			13.14
	2	Linear Phase	48		16.00
		Low Latency			18.28
	3	Linear Phase	96		22.94
		Low Latency			25.05
	4	Linear Phase			27.43
		Low Latency			29.60

Table 2-1. Typical Current Consumption (PLL Enabled) (continued)

SAMPLING FREQUENCY (kHz)	ADC CHANNELS	DECIMATION FILTERS	BCLK RATIO	WORD LENGTH	AVDD CURRENT AT 3.3 V (mA)
384	1	Linear Phase	24	24	13.67
		Low Latency			13.96
	2	Linear Phase	48		20.33
		Low Latency			20.47

3 Slave Mode Power Consumption with PLL Disabled

Typical Current Consumption (PLL Disabled) describes the typical current consumption of the PCM6xx0 when the PLL is disabled with AVDD set to 3.3 V. The PLL is disabled by:

- Clearing the bitfield PLL_PDZ in the PWR_CFG register
- Applying a master clock through BCLK, GPIO1, or the GPIx pins
- If GPIO1 is configured as MCLK, setting the appropriate GPIO1_CFG bitfield in the GPIO_CFG0 register
- Indicating the master clock source through DIS_PLL_SLV_CLK_SRC bitfield in the CLK_SRC register
- Setting the appropriate MCLK to FSYNC ratio through the MCLK_RATIO_SEL bitfield and MCLK_FREQ_SEL_MODE bitfield of the CLK_SRC register
- Setting the AUTO_MODE_PLL_DIS bitfield and the corresponding MCLK_FREQ_SEL bitfield of the MST_CFG0 register

The current consumption measurements had the AGC and the Biquad Filters disabled.

Table 3-1. Typical Current Consumption (PLL Disabled)

SAMPLING FREQUENCY (kHz)	MCLK FREQUENCY(MHz)	MCLK RATIO	ADC CHANNELS	DECIMATION FILTERS	BCLK RATIO	WORD LENGTH	AVDD CURRENT AT 3.3V (mA)
8	12.288	1536	1	Linear Phase	32	32	7.15
			2		48	24	11.45
			3		96		14.95
			4				20.76
			5		144		23.56
			6		144		27.95
16	12.288	768	1	Linear Phase	24	24	8.18
				Low Latency			8.21
				Ultra-Low Latency			8.73
			2	Linear Phase	48		11.98
				Low Latency			12.64
				Ultra-Low Latency			10.71
			3	Linear Phase	96		16.64
				Low Latency			17.06
				Ultra-Low Latency			16.77
			4	Linear Phase			19.06
				Low Latency			20.99
				Ultra-Low Latency			18.96
			5	Linear Phase	144		23.25
				Low Latency			23.71
				Ultra-Low Latency			22.71
			6	Linear Phase			28.62
				Low Latency			28.57
				Ultra-Low Latency			27.32

Table 3-1. Typical Current Consumption (PLL Disabled) (continued)

SAMPLING FREQUENCY (kHz)	MCLK FREQUENCY(MHz)	MCLK RATIO	ADC CHANNELS	DECIMATION FILTERS	BCLK RATIO	WORD LENGTH	AVDD CURRENT AT 3.3V (mA)
16	24.576	1536	1	Linear Phase	24	24	8.53
				Low Latency			7.91
				Ultra-Low Latency			8.08
			2	Linear Phase	48		12.74
				Low Latency			13.34
				Ultra-Low Latency			13.35
			3	Linear Phase	96		16.02
				Low Latency			16.15
				Ultra-Low Latency			17.17
			4	Linear Phase			21.53
				Low Latency			21.98
				Ultra-Low Latency			19.91
			5	Linear Phase	144		25.77
				Low Latency			26.18
				Ultra-Low Latency			24.08
			6	Linear Phase	192	32	30.32
				Low Latency			30.67
				Ultra-Low Latency			28.59
16	36.864	2304	1	Linear Phase	24	24	7.78
				Low Latency			9.43
				Ultra-Low Latency			7.56
			2	Linear Phase	48		12.70
				Low Latency			11.86
				Ultra-Low Latency			12.54
			3	Linear Phase	96		16.47
				Low Latency			18.33
				Ultra-Low Latency			16.02
			4	Linear Phase			21.77
				Low Latency			21.18
				Ultra-Low Latency			22.35
			5	Linear Phase	144		25.70
				Low Latency			25.45
				Ultra-Low Latency			26.54
			6	Linear Phase			30.67
				Low Latency			31.44
				Ultra-Low Latency			29.69

Table 3-1. Typical Current Consumption (PLL Disabled) (continued)

SAMPLING FREQUENCY (kHz)	MCLK FREQUENCY(MHz)	MCLK RATIO	ADC CHANNELS	DECIMATION FILTERS	BCLK RATIO	WORD LENGTH	AVDD CURRENT AT 3.3V (mA)
24	12.288	512	1	Linear Phase	24	24	8.44
				Low Latency			7.03
				Ultra-Low Latency			6.61
			2	Linear Phase	48		13.08
				Low Latency			12.48
				Ultra-Low Latency	64	32	11.14
			3	Linear Phase	96	24	16.59
				Low Latency			15.20
				Ultra-Low Latency			17.17
			4	Linear Phase			18.89
				Low Latency			20.84
				Ultra-Low Latency			20.50
			5	Linear Phase	144		23.01
				Low Latency			24.74
				Ultra-Low Latency			24.75
			6	Linear Phase	192	32	27.52
				Low Latency			28.47
				Ultra-Low Latency			27.9
	24.576	1024	1	Linear Phase	32	32	8.03
				Low Latency			7.74
				Ultra-Low Latency			8.33
			2	Linear Phase	64		13.53
				Low Latency			11.87
				Ultra-Low Latency			13.55
			3	Linear Phase	128		17.23
				Low Latency			18.33
				Ultra-Low Latency			15.93
			4	Linear Phase			21.82
				Low Latency			20.81
				Ultra-Low Latency			21.46
			5	Linear Phase	192		24.61
				Low Latency			25.04
				Ultra-Low Latency			26.59
			6	Linear Phase			29.65
				Low Latency			30.13
				Ultra-Low Latency			28.37
24	36.864	1536	1	Linear Phase	24	24	8.58
				Low Latency			9.84
				Ultra-Low Latency			8.08
			2	Linear Phase	48		14.00
				Low Latency			13.77
				Ultra-Low Latency			13.00
			3	Linear Phase	96		17.42
				Low Latency			17.37
				Ultra-Low Latency			18.34
			4	Linear Phase			22.98
				Low Latency			22.62
				Ultra-Low Latency			23.00
			5	Linear Phase	144		27.30
				Low Latency			26.04
				Ultra-Low Latency			27.16
			6	Linear Phase	192	32	31.47
				Low Latency			31.44
				Ultra-Low Latency			29.87

Table 3-1. Typical Current Consumption (PLL Disabled) (continued)

SAMPLING FREQUENCY (kHz)	MCLK FREQUENCY(MHz)	MCLK RATIO	ADC CHANNELS	DECIMATION FILTERS	BCLK RATIO	WORD LENGTH	AVDD CURRENT AT 3.3V (mA)
32	12.288	384	1	Linear Phase	24	24	7.01
				Low Latency			6.87
				Ultra-Low Latency			8.91
			2	Linear Phase	48		12.72
				Low Latency			11.84
				Ultra-Low Latency	64	32	12.27
			3	Linear Phase	96	24	17.2
				Low Latency			15.68
				Ultra-Low Latency			14.93
			4	Linear Phase			18.81
				Low Latency			18.74
				Ultra-Low Latency			19.38
			5	Linear Phase	144		23.14
				Low Latency			22.82
				Ultra-Low Latency			23.30
			6	Linear Phase			27.97
				Low Latency			27.45
				Ultra-Low Latency			26.46
	24.576	768	1	Linear Phase	24		8.01
				Low Latency			9.45
				Ultra-Low Latency			8.02
			2	Linear Phase	48		13.02
				Low Latency			13.60
				Ultra-Low Latency			13.47
			3	Linear Phase	96		16.33
				Low Latency			16.60
				Ultra-Low Latency			16.69
			4	Linear Phase			20.66
				Low Latency			22.70
				Ultra-Low Latency			22.25
			5	Linear Phase	144		25.14
				Low Latency			26.46
				Ultra-Low Latency			26.18
			6	Linear Phase	192		29.94
				Low Latency			30.62
				Ultra-Low Latency			28.63

Table 3-1. Typical Current Consumption (PLL Disabled) (continued)

SAMPLING FREQUENCY (kHz)	MCLK FREQUENCY(MHz)	MCLK RATIO	ADC CHANNELS	DECIMATION FILTERS	BCLK RATIO	WORD LENGTH	AVDD CURRENT AT 3.3V (mA)
48	12.288	256	1	Linear Phase	24	24	9.27
				Low Latency			8.72
				Ultra-Low Latency			8.41
			2	Linear Phase	48		11.85
				Low Latency			11.58
				Ultra-Low Latency			12.85
			3	Linear Phase	96		16.71
				Low Latency			15.86
				Ultra-Low Latency			16.92
			4	Linear Phase			20.88
				Low Latency			21.05
				Ultra-Low Latency			20.94
			5	Linear Phase	144		24.65
				Low Latency			22.79
				Ultra-Low Latency			23.02
			6	Linear Phase	192	32	26.93
				Low Latency			28.74
				Ultra-Low Latency			26.82
	24.576	512	1	Linear Phase	32	32	9.07
				Low Latency			8.72
				Ultra-Low Latency			9.27
			2	Linear Phase	64		13.30
				Low Latency			14.31
				Ultra-Low Latency			13.82
			3	Linear Phase	128		19.15
				Low Latency			17.38
				Ultra-Low Latency			16.97
			4	Linear Phase			20.88
				Low Latency			23.07
				Ultra-Low Latency			22.72
			5	Linear Phase	192		24.73
				Low Latency			24.87
				Ultra-Low Latency			25.84
			6	Linear Phase			28.49
				Low Latency			28.74
				Ultra-Low Latency			30.60
48	36.864	768	1	Linear Phase	24	24	9.62
				Low Latency			8.17
				Ultra-Low Latency			7.66
			2	Linear Phase	48		14.83
				Low Latency			14.27
				Ultra-Low Latency			12.52
			3	Linear Phase	96		17.65
				Low Latency			18.89
				Ultra-Low Latency			18.15
			4	Linear Phase			23.67
				Low Latency			24.07
				Ultra-Low Latency			23.05
			5	Linear Phase	144		26.94
				Low Latency			28.46
				Ultra-Low Latency			27.75
			6	Linear Phase	192	32	31.00
				Low Latency			31.84
				Ultra-Low Latency			30.01

Table 3-1. Typical Current Consumption (PLL Disabled) (continued)

SAMPLING FREQUENCY (kHz)	MCLK FREQUENCY(MHz)	MCLK RATIO	ADC CHANNELS	DECIMATION FILTERS	BCLK RATIO	WORD LENGTH	AVDD CURRENT AT 3.3V (mA)
96	24.576	256	1	Linear Phase	32	32	11.09
				Low Latency			10.84
				Ultra-Low Latency			9.48
			2	Linear Phase	64		13.52
				Low Latency			13.10
				Ultra-Low Latency			12.98
			3	Linear Phase	128		18.47
				Low Latency			17.31
				Ultra-Low Latency			19.00
			4	Linear Phase			23.06
				Low Latency			21.55
				Ultra-Low Latency			20.95
			5	Linear Phase	192		26.64
				Low Latency			24.94
				Ultra-Low Latency			26.97
			6	Linear Phase			30.36
				Low Latency			28.78
				Ultra-Low Latency			30.77
	36.864	384	1	Linear Phase	24	24	9.49
				Low Latency			11.22
				Ultra-Low Latency			8.70
			2	Linear Phase	48		15.24
				Low Latency			16.04
				Ultra-Low Latency			14.93
			3	Linear Phase	96		21.05
				Low Latency			21.13
				Ultra-Low Latency			19.03
			4	Linear Phase			23.43
				Low Latency			23.08
				Ultra-Low Latency			25.09
			5	Linear Phase	144		27.44
				Low Latency			27.94
				Ultra-Low Latency			27.54
			6	Linear Phase			32.05
				Low Latency			32.87
				Ultra-Low Latency			32.29
192	12.288	64	1	Linear Phase	24	24	9.44
				Low Latency			8.92
				Ultra-Low Latency			9.20
			2	Linear Phase	48		11.27
				Low Latency			11.83
				Ultra-Low Latency			13.52
			3	Linear Phase	96		15.41
				Low Latency			16.34
				Ultra-Low Latency			15.52
			4	Linear Phase			19.46
			5	Linear Phase	144		25.19
				Low Latency			24.56
				Ultra-Low Latency			24.54
			6	Linear Phase	192	32	29.20
				Low Latency			28.44
				Ultra-Low Latency			27.25

4 Digital Microphone Power Consumption

Table 4-1 and Table 4-2 describes the typical current consumption of the PCM6480 when the digital microphone inputs are used with an external PDM modulator 4th and 5th order, respectively. PCM6480 supports up to 4 PDM channels. The Digital Microphone is selected by:

- Configuring the corresponding channel for digital microphone input in the CHx_INSRC field in the CHx_CFG0 register.
- Configuring the corresponding GPIOx pin as PDMCLK output in the appropriate GPIO_CFGx register.
- Configuring the corresponding GPIx pin as PDM input in the appropriate GPI_CFGx register.

Table 4-1. PDM Typical Current Consumption With an External PDM 4th Order Modulator

PDM CLOCK		6.144 MHz	3.072 MHz	1.536 MHz	0.768 MHz
SAMPLING RATE (kHz)	DIGITAL MICROPHONE CHANNELS	AVDD CURRENT AT 3.3 V (mA)	AVDD CURRENT AT 3.3 V (mA)	AVDD CURRENT AT 3.3 V (mA)	AVDD CURRENT AT 3.3 V (mA)
8	2	6.36	6.31	6.28	6.26
	4	7.74	7.68	7.65	7.62
16	2	6.69	6.65	6.62	6.60
	4	8.36	8.30	8.29	8.23
24	2	6.66	6.60	6.58	-
	4	8.27	8.22	8.18	-
32	2	6.91	6.88	6.84	-
	4	8.72	8.69	8.63	-
48	2	7.46	7.42	7.37	-
	4	9.94	9.90	9.84	-
96	2	10.10	10.02	9.96	-
	4	13.99	13.88	13.79	-
192	2	10.10	10.01	9.93	-
	4	14.08	13.96	13.83	-

Table 4-2. PDM Typical Current Consumption With an External PDM 5th Order Modulator

PDM CLOCK		6.144 MHz	3.072 MHz	1.536 MHz	0.768 MHz
SAMPLING RATE (kHz)	DIGITAL MICROPHONE CHANNELS	AVDD CURRENT AT 3.3 V (mA)	AVDD CURRENT AT 3.3 V (mA)	AVDD CURRENT AT 3.3 V (mA)	AVDD CURRENT AT 3.3 V (mA)
8	2	6.36	6.31	6.28	6.27
	4	7.73	7.68	7.65	7.64
16	2	6.69	6.65	6.63	6.61
	4	8.36	8.33	8.30	8.27
24	2	6.66	6.62	6.59	-
	4	8.25	8.23	8.18	-
32	2	6.91	6.89	6.84	-
	4	8.71	8.70	8.64	-
48	2	7.47	7.42	7.38	-
	4	9.97	9.91	9.85	-
96	2	10.11	10.03	9.97	-
	4	14.01	13.89	13.79	-
192	2	10.12	10.02	9.93	-
	4	14.12	13.97	13.82	-

5 MICBIAS Power Consumption

Table 5-1 and Table 5-2 describes the typical current consumption of the PCM6xx0 when the MICBIAS is turned on and a load is connected externally to the MICBIAS pin. Sampling frequency = 48KHz , BCLK/Fs = 192 , ADC and PLL are turned ON. The MICBIAS is turned on and programmed by:

- Configuring the required voltage for MICBIAS in MBIAS_VAL field in the BIAS_CFG register.
- Setting the MICBIAS_PDz bit in the PWR_CFG register.

Table 5-1. MICBIAS Typical Current Consumption for PCM62x0 with Load Connected from 0mA to 80mA

MICBIAS VOLTAGE (V)	LOAD CONNECTED TO MICBIAS (mA)	BSTVDD CURRENT at 3.3V (mA)
5	0	6.94
	5	18.02
	10	30.45
	15	40.48
	20	51.29
	25	63.07
	30	75.45
	35	86.33
	40	97.33
	45	108.19
	50	119.22
	55	130.32
	60	143.29
	65	154.66
	70	166.01
	75	177.28
	80	188.77
5.5	0	8.02
	5	19.74
	10	32.78
	15	44.21
	20	55.35
	25	68.57
	30	81.84
	35	93.68
	40	105.47
	45	117.26
	50	129.15
	55	141.23
	60	155.25
	65	167.50
	70	179.92
	75	192.27
	80	204.74

Table 5-1. MICBIAS Typical Current Consumption for PCM62x0 with Load Connected from 0mA to 80mA (continued)

MICBIAS VOLTAGE (V)	LOAD CONNECTED TO MICBIAS (mA)	BSTVDD CURRENT at 3.3V (mA)
6	0	8.77
	5	21.68
	10	35.64
	15	47.88
	20	59.70
	25	74.25
	30	87.31
	35	101.15
	40	113.83
	45	126.62
	50	139.61
	55	152.56
	60	165.48
	65	178.64
	70	194.21
	75	207.71
	80	221.16
6.5	0	9.37
	5	23.19
	10	37.92
	15	50.81
	20	64.41
	25	80.00
	30	93.81
	35	107.36
	40	122.40
	45	136.18
	50	150.09
	55	164.00
	60	178.09
	65	192.25
	70	206.39
	75	223.52
	80	238.16

Table 5-1. MICBIAS Typical Current Consumption for PCM62x0 with Load Connected from 0mA to 80mA (continued)

MICBIAS VOLTAGE (V)	LOAD CONNECTED TO MICBIAS (mA)	BSTVDD CURRENT at 3.3V (mA)
7	0	10.03
	5	25.16
	10	40.87
	15	54.34
	20	69.18
	25	85.89
	30	100.65
	35	115.01
	40	129.59
	45	144.27
	50	158.94
	55	175.76
	60	190.95
	65	206.20
	70	221.44
	75	237.00
	80	252.61
7.5	0	10.53
	5	26.73
	10	43.10
	15	57.18
	20	74.18
	25	90.76
	30	106.16
	35	122.79
	40	138.46
	45	154.04
	50	169.89
	55	185.78
	60	201.83
	65	220.47
	70	236.93
	75	253.61
	80	270.29

Table 5-1. MICBIAS Typical Current Consumption for PCM62x0 with Load Connected from 0mA to 80mA (continued)

MICBIAS VOLTAGE (V)	LOAD CONNECTED TO MICBIAS (mA)	BSTVDD CURRENT at 3.3V (mA)
8	0	10.86
	5	28.22
	10	45.71
	15	60.36
	20	78.25
	25	96.66
	30	113.03
	35	129.23
	40	145.66
	45	162.30
	50	180.86
	55	197.88
	60	215.09
	65	232.36
	70	249.97
	75	267.63
	80	288.62
8.5	0	11.07
	5	30.00
	10	47.64
	15	62.76
	20	83.30
	25	101.49
	30	118.51
	35	135.74
	40	154.68
	45	172.36
	50	190.14
	55	208.15
	60	226.22
	65	247.24
	70	265.90
	75	284.88
	80	303.99

Table 5-1. MICBIAS Typical Current Consumption for PCM62x0 with Load Connected from 0mA to 80mA (continued)

MICBIAS VOLTAGE (V)	LOAD CONNECTED TO MICBIAS (mA)	BSTVDD CURRENT at 3.3V (mA)
9	0	11.07
	5	31.23
	10	49.48
	15	66.21
	20	87.39
	25	107.22
	30	125.38
	35	143.60
	40	162.01
	45	180.55
	50	201.27
	55	220.40
	60	239.70
	65	259.31
	70	279.18
	75	299.21
	80	322.93

Table 5-2. MICBIAS Typical Current Consumption for PCM63x0 with Load Connected from 0mA to 80mA

MICBIAS VOLTAGE (V)	LOAD CONNECTED TO MICBIAS (mA)	HVDD CURRENT (mA) HVDD = MICBIAS VOLTAGE (Column 1) + 0.6V
5	0	0.00
	5	5.15
	10	10.20
	15	15.27
	20	20.45
	25	25.42
	30	30.59
	35	35.57
	40	40.67
	45	45.78
	50	50.79
	55	55.85
	60	61.00
	65	66.06
	70	71.04
	75	76.18
	80	81.25

Table 5-2. MICBIAS Typical Current Consumption for PCM63x0 with Load Connected from 0mA to 80mA (continued)

MICBIAS VOLTAGE (V)	LOAD CONNECTED TO MICBIAS (mA)	HVDD CURRENT (mA) HVDD = MICBIAS VOLTAGE (Column 1) + 0.6V
5.5	0	0.10
	5	5.14
	10	10.33
	15	15.32
	20	20.38
	25	25.55
	30	30.57
	35	35.61
	40	40.74
	45	45.75
	50	50.87
	55	55.91
	60	61.03
	65	66.01
	70	71.13
	75	76.24
	80	81.21
6	0	0.05
	5	5.27
	10	10.37
	15	15.35
	20	20.50
	25	25.52
	30	30.66
	35	35.74
	40	40.69
	45	45.84
	50	50.86
	55	55.94
	60	61.07
	65	66.14
	70	71.11
	75	76.26
	80	81.34

Table 5-2. MICBIAS Typical Current Consumption for PCM63x0 with Load Connected from 0mA to 80mA (continued)

MICBIAS VOLTAGE (V)	LOAD CONNECTED TO MICBIAS (mA)	HVDD CURRENT (mA) HVDD = MICBIAS VOLTAGE (Column 1) + 0.6V
6.5	0	0.15
	5	5.24
	10	10.30
	15	15.44
	20	20.53
	25	25.54
	30	30.58
	35	35.76
	40	40.82
	45	45.80
	50	50.92
	55	55.98
	60	61.00
	65	66.17
	70	71.15
	75	76.26
	80	81.26
7	0	0.15
	5	5.26
	10	10.40
	15	15.50
	20	20.49
	25	25.62
	30	30.64
	35	35.78
	40	40.77
	45	45.90
	50	51.00
	55	55.97
	60	61.09
	65	66.21
	70	71.23
	75	76.26
	80	81.37

Table 5-2. MICBIAS Typical Current Consumption for PCM63x0 with Load Connected from 0mA to 80mA (continued)

MICBIAS VOLTAGE (V)	LOAD CONNECTED TO MICBIAS (mA)	HVDD CURRENT (mA) HVDD = MICBIAS VOLTAGE (Column 1) + 0.6V
7.5	0	0.16
	5	5.27
	10	10.45
	15	15.44
	20	20.60
	25	25.59
	30	30.76
	35	35.72
	40	40.89
	45	45.87
	50	50.93
	55	56.09
	60	61.12
	65	66.15
	70	71.30
	75	76.35
	80	81.37
8	0	0.30
	5	5.32
	10	10.45
	15	15.56
	20	20.53
	25	25.72
	30	30.80
	35	35.84
	40	40.84
	45	45.98
	50	51.01
	55	56.04
	60	61.15
	65	66.18
	70	71.24
	75	76.29
	80	81.44

Table 5-2. MICBIAS Typical Current Consumption for PCM63x0 with Load Connected from 0mA to 80mA (continued)

MICBIAS VOLTAGE (V)	LOAD CONNECTED TO MICBIAS (mA)	HVDD CURRENT (mA) HVDD = MICBIAS VOLTAGE (Column 1) + 0.6V
8.5	0	0.22
	5	5.42
	10	10.48
	15	15.50
	20	20.65
	25	25.67
	30	30.71
	35	35.79
	40	40.94
	45	45.93
	50	50.99
	55	56.07
	60	61.22
	65	66.21
	70	71.29
	75	76.31
	80	81.49
9	0	0.26
	5	5.46
	10	10.50
	15	15.54
	20	20.68
	25	25.76
	30	30.78
	35	35.92
	40	40.90
	45	46.04
	50	51.13
	55	56.09
	60	61.26
	65	66.24
	70	71.35
	75	76.35
	80	81.52

6 Settings for Lowest Power Consumption

To minimize the power consumption of the PCM6xx0 devices, ensure that unused modules are disabled, use the lowest sampling rate, bit clock, and master clock needed by the application, and operate at the lowest AVDD and IOVDD supply voltage possible. The following list summarizes the settings and registers for lowest power operation:

- Operate at the lowest supply voltage possible. IOVDD supports 1.8 V or 3.3 V supply, independently AVDD supports 3.3-V supply (AVDD and IOVDD can have different supply voltages).
  - Unused analog inputs, tie to analog ground.
  - Unused digital inputs, tie to digital ground.
  - Unused outputs, leave unconnected.
- Disable unused ADC and PDM channels through the IN_CH_EN register.
- Disable any unused output channel through the ASI_OUT_CH_EN register.
- Disable MICBIAS power, if unused, through the PWR_CFG register.
- Operate at the lowest sample rate possible.
- Disable PLL, if the system supplies a low jitter master clock. Refer to *Section 3* for a description of the settings to disable PLL.
- Disable unused post-processing blocks:
  - Disable Biquad filters, if unused, through the BIQUAD_CFG bitfield of the DSP_CFG1 register.
  - Disable AGC, if unused in an active channel, through the CHx_AGCEN bitfield of the CHx_CFG0 register.
- Select ultra-low latency over linear phase decimation filters, if the application allows, through the DECI_FILT bitfield of the DSP_CFG0 register.
- Use the smallest word length allowed by the application through the ASI_WLEN bitfield of the ASI_CFG0 register.

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (May 2021) to Revision A (September 2021)	Page
• Added Digital Microphone Power Consumption Data	12
• Added MICBIAS Power Consumption Data	13

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