Application Note

Analog Front-End Design With Texas Instruments' Tooling Landscape

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ABSTRACT

The performance of a data acquisition system is primarily characterized by its bandwidth and SNR. The most critical and typically most valuable component in such systems is the analog-to-digital converter (ADC). Designers select the ADC according to their needs in terms of Effective Number of Bits (ENOB), sample rate, and likely a few more key parameters such as power consumption or package options. For space-applications radiation hardness is another important selection criteria which adds another level of cost.

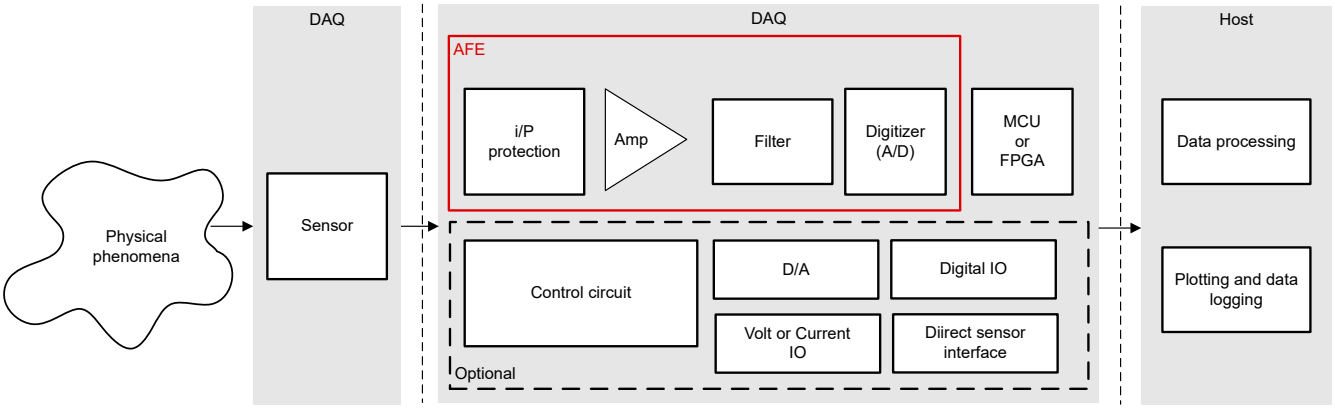

Figure 1-1. Analog Front-End in a Typical Data Acquisition System

After the selection of the ADC designers must then develop an analog front-end that conditions the input signal in a way so the ADC can really perform at its specified level. Such conditioning includes amplification or attenuation plus level shifting of the signal to meet the full differential and common-mode input range of the ADC. At the same time the analog front-end circuit must keep the noise floor low and avoid any non-linearity within the signal bandwidth of interest. Stability analysis must show enough margin, the input impedance must be high enough and the output drive capability must be strong enough to meet the settling time requirement of the sample and hold capacitor of the ADC.

In short, designers face a multi-dimensional design challenge they typically have to solve in an iterative development effort. To succeed quickly it is important to have a good starting point, a good idea on what variables to tune to reach the design goal, and even greater tools that allow designers to analyze all aspects of each design iteration effectively.

This application note describes how to get to such starting point quickly and how TI's products and tools assist designers to tune the design effectively with the help of a concrete design example.

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1 Component and Topology Selection - Finding a Good Starting Point Quickly

The following chapters use an example design described by Table 1-1.

Table 1-1. Design Goal Parameters of Example Analog Front-End

Parameter	Design Goal
Channel Count	8
Bandwidth and Sampling Rate	40 kHz, > 100 ksps
Input Full Scale Range (FSR)	±10-V FSR
Common-Mode Voltage	About 0 V common mode
Target Resolution, ENOB	> 16 bit
Input Impedance (Z_{IN}) Target	> 100 kΩ
Radiation hardness	TID: > 50 krad, SEL: > 60 (MeV × cm^2/mg)

The *TI Space Products Guide*, *Space-Grade Data Converters* section shows that the ADS1278-SP best fits these requirements.

Precision ADCs (≤ 10 MSPS)

Part Number[1]	Military Spec	Qualification Level	TID Char. (krad)	TID RLAT (krad)	SEL (MeV•cm^2/mg)	Res. (Bits)	Sample Rate (Max) (kSPS)	# of Ch	Multi-Ch Config.	SNR (dB)	INL (Max) (± LSB)	Input Type	Ref. Voltage (V)	Power (Typ) (mW)	Type	Package Group	ECCN[2]
ADC128S1020QML-SP	5962-07227	QMLV-RHA	100	100	120	12	1000	8	Multiplexed	72	1.1	Single ended	Supply	2.3	SAR	CFP, Die	EAR99†
ADS1278-SP	–	TI Space Grade	75	50	68	24	128	8	Simultaneous	111	201.4	Differential	External	530	ΔΣ	CQFP	EAR99‡
ADS1282-SP	5962-14231	QMLV-RHA	50	50	60	32	4	2	Multiplexed	130	–	Differential	External	25	ΔΣ	CFP	EAR99‡

Figure 1-1. TI's Space-Grade Precision ADCs Listed in TI's Space Product Guide

The next step is to identify the right ADC driver. For best noise immunity and linearity a fully differential amplifier (FDA) is preferred.

To identify the right product, the minimum unity gain bandwidth of such FDA must be understood. The ANALOG-ENGINEER'S CALCULATOR provides great assistance here.

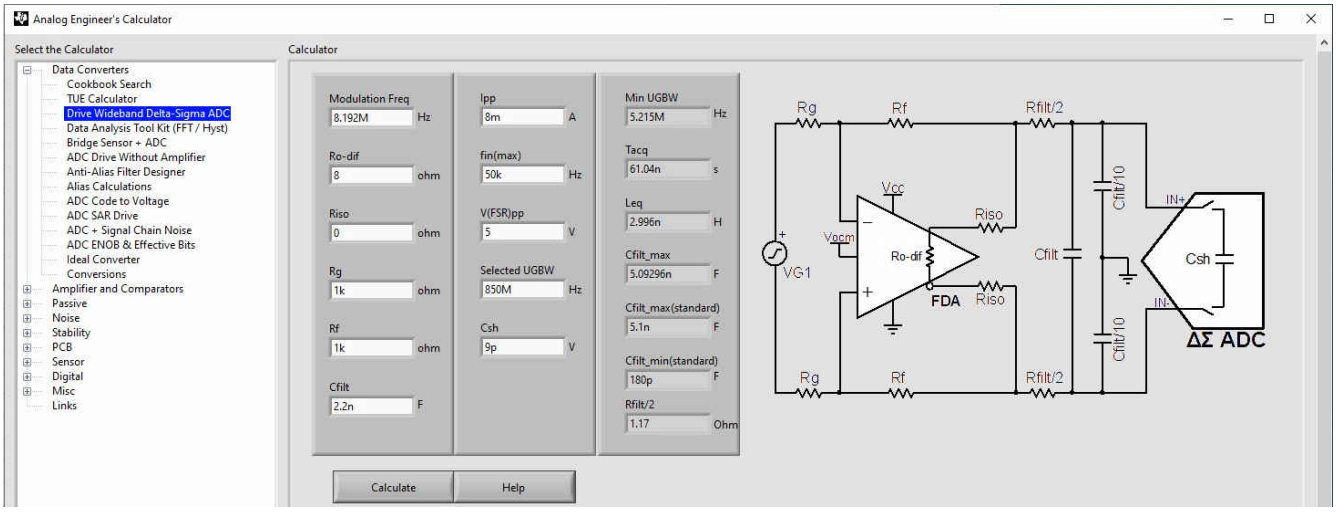


Figure 1-2. ANALOG-ENGINEER'S CALCULATOR – Drive Wideband Delta-Sigma ADC

Figure 1-2 illustrates that the *Data Converters* menu offers the *Drive Wideband Delta-Sigma ADC* item. The reference schematic in the figure shows all relevant component values. The white fields must be entered by the user, the gray fields are the resulting values. The very first variable to define is the minimum unity gain bandwidth (UGBW). In other words, up to what frequency must the gain of the amplifier be equal or greater than one. Since the ADC will cut off any information above the Nyquist or sample frequency divided by two, it is sufficient if the UGBW of the amplifier is about two-thirds of the sampling frequency. For example, for a sample rate of 1 kHz, look at a minimum UGBW of 636.6 Hz.

The selected ADC in the example of this report is a sigma-delta ADC. It is important to remember that a sigma-delta ADC is a one-bit ADC at the provided modulation frequency. The actual sample rate is only the frequency the full sample words come out of it. The relevant frequency for the AFE design is the modulation frequency which is much higher.

Due to the flexibility and complexity of modern ADCs it is not always straightforward to read the modulation frequency from the data sheet. The ADS1278-SP provides different operating modes that allow for different master clock rates. Figure 1-3 shows the actual modulation frequency is just one-fourth of the master clock. In the example, the ADS1278-SP operates in High-Speed mode: 128 ksps, f_{CLK} is 32.786 MHz. F_{CLK} divided by four results in 8.192 MHz for the actual modulation frequency.

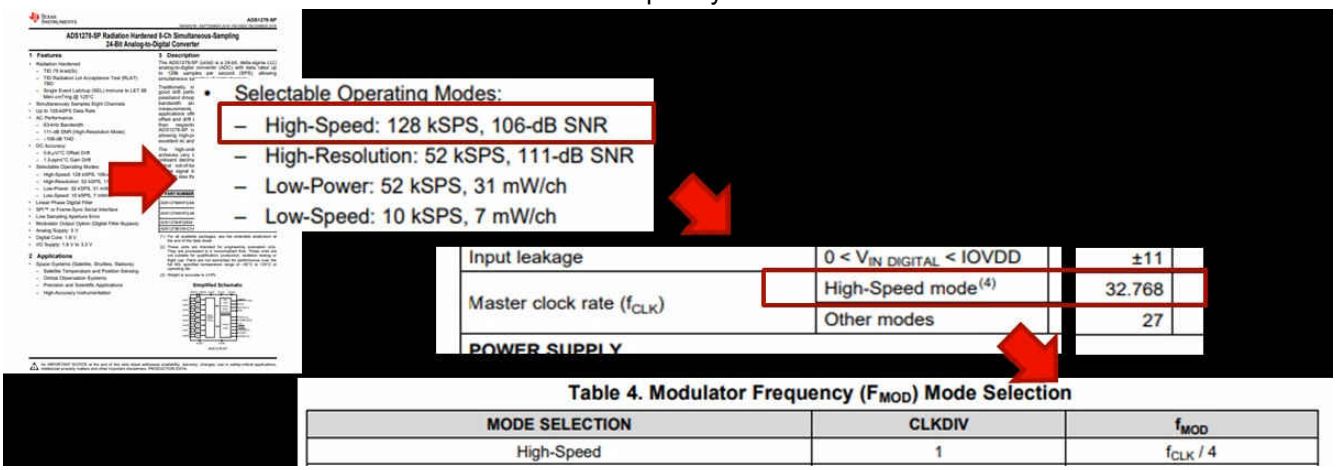


Figure 1-3. Reading the Modulation Frequency From the ADS1278-SP Data Sheet

Figure 1-4 shows that entering the modulation frequency of "*8.192M*" (8.192 MHz) into the **ANALOG-ENGINEER'S CALCULATOR** determines a minimum UGBW of "5.215M" (5.215 MHz).

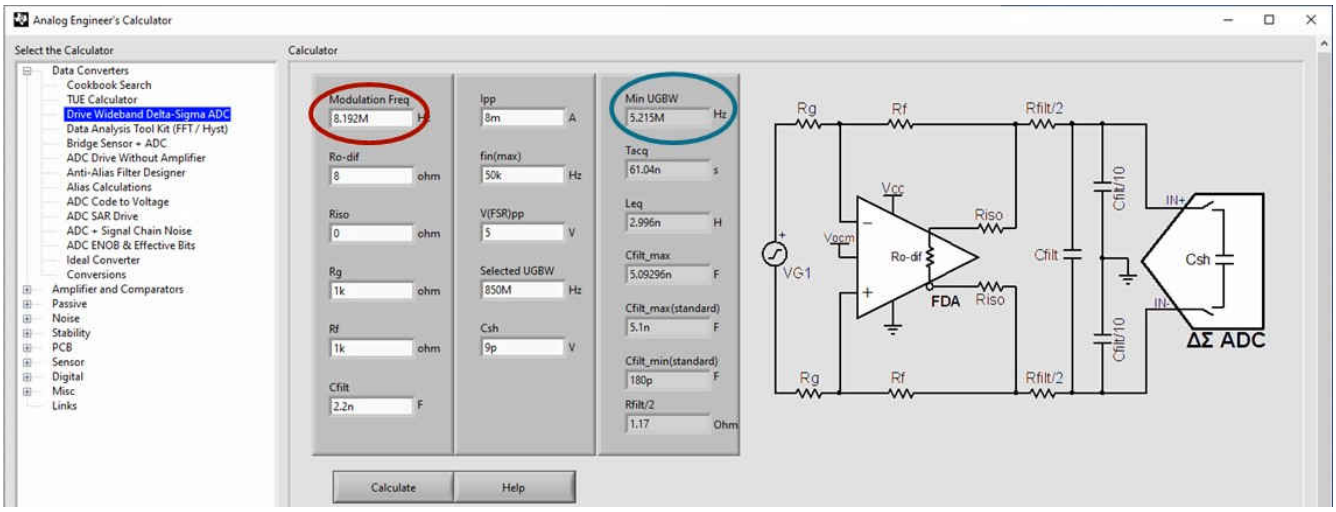
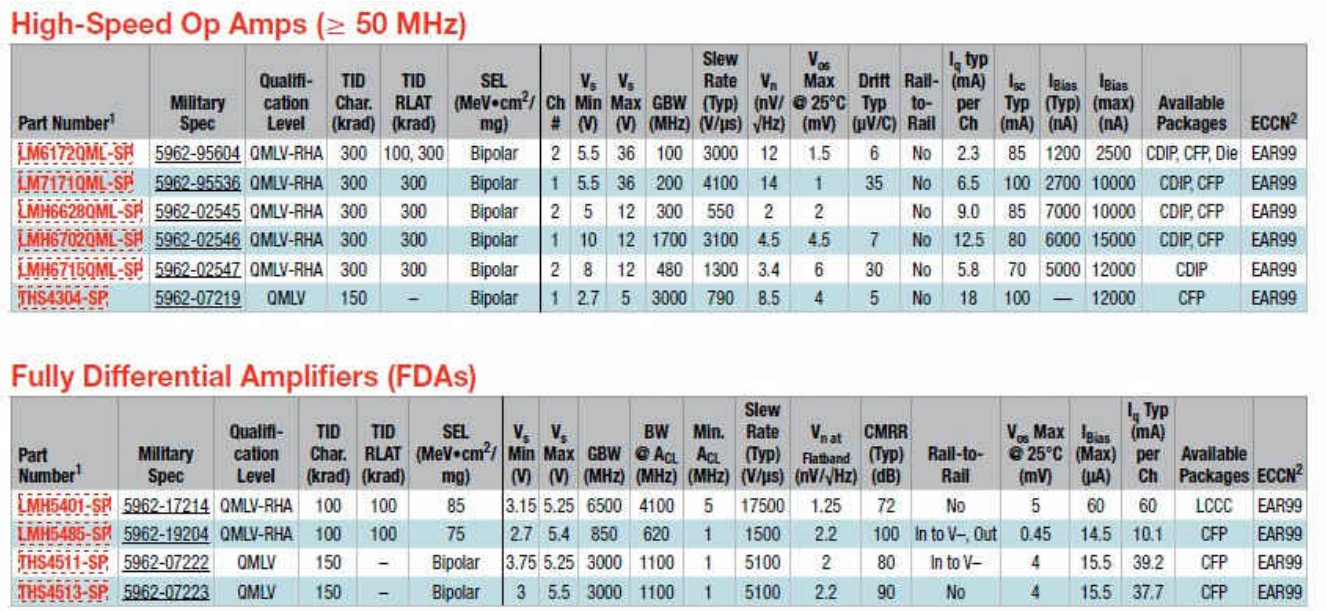


Figure 1-4. Using ANALOG-ENGINEER'S CALCULATOR to Determine the Minimum Unity Gain Bandwidth of the FDA

Figure 1-5 illustrates the TI space product guide showing four FDAs. All four provide more than sufficient UGBW. As an example for this report, the lowest one (LMH5485-SP) with 850-MHz UGBW is selected.



High-Speed Op Amps (≥ 50 MHz)

Part Number[1]	Military Spec	Qualification Level	TID Char. (krad)	TID RLAT (krad)	SEL (MeV•cm²/mg)	Ch #	V_S Min (V)	V_S Max (V)	GBW (MHz)	Slew Rate (Typ) (V/µs)	V_n (nV/√Hz)	V_{os} Max @ 25°C (mV)	Drift Typ (µV/C)	Rail-to-Rail	I_Q typ (mA) per Ch	I_{sc} Typ (mA)	I_{Bias} (Typ) (nA)	I_{Bias} (max) (nA)	Available Packages	ECCN[2]
LM6172QML-SP	5962-95604	QMLV-RHA	300	100, 300	Bipolar	2	5.5	36	100	3000	12	1.5	6	No	2.3	85	1200	2500	CDIP, CFP, Die	EAR99
LM7171QML-SP	5962-95536	QMLV-RHA	300	300	Bipolar	1	5.5	36	200	4100	14	1	35	No	6.5	100	2700	10000	CDIP, CFP	EAR99
LMH6628QML-SP	5962-02545	QMLV-RHA	300	300	Bipolar	2	5	12	300	550	2	2		No	9.0	85	7000	10000	CDIP, CFP	EAR99
LMH6702QML-SP	5962-02546	QMLV-RHA	300	300	Bipolar	1	10	12	1700	3100	4.5	4.5	7	No	12.5	80	6000	15000	CDIP, CFP	EAR99
LMH6715QML-SP	5962-02547	QMLV-RHA	300	300	Bipolar	2	8	12	480	1300	3.4	6	30	No	5.8	70	5000	12000	CDIP	EAR99
THS4304-SP	5962-07219	QMLV	150	–	Bipolar	1	2.7	5	3000	790	8.5	4	5	No	18	100	—	12000	CFP	EAR99

Fully Differential Amplifiers (FDAs)

Part Number[1]	Military Spec	Qualification Level	TID Char. (krad)	TID RLAT (krad)	SEL (MeV•cm²/mg)	V_S Min (V)	V_S Max (V)	GBW (MHz)	BW @ A_{CL} (MHz)	Min. A_{CL} (MHz)	Slew Rate (Typ) (V/µs)	$V_{n\,at\,Flatband}$ (nV/√Hz)	CMRR (Typ) (dB)	Rail-to-Rail	V_{os} Max @ 25°C (mV)	I_{Bias} (Max) (µA)	I_Q Typ (mA) per Ch	Available Packages	ECCN[2]
LMH5401-SP	5962-17214	QMLV-RHA	100	100	85	3.15	5.25	6500	4100	5	17500	1.25	72	No	5	60	60	LCCC	EAR99
LMH5485-SP	5962-19204	QMLV-RHA	100	100	75	2.7	5.4	850	620	1	1500	2.2	100	In to V–, Out	0.45	14.5	10.1	CFP	EAR99
THS4511-SP	5962-07222	QMLV	150	–	Bipolar	3.75	5.25	3000	1100	1	5100	2	80	In to V–	4	15.5	39.2	CFP	EAR99
THS4513-SP	5962-07223	QMLV	150	–	Bipolar	3	5.5	3000	1100	1	5100	2.2	90	No	4	15.5	37.7	CFP	EAR99

Figure 1-5. Selecting the Best Fitting FDA from TI's Space Product Guide

With that selection it is now possible to *fill* the rest of the white fields in the ANALOG-ENGINEER'S CALCULATOR, see Figure 1-6.

Parameter	Description
Ro-dif	**Ro-dif** is the "open-loop output impedance". The *LMH5485-SP Radiation Hardened Assured (RHA) Negative Rail Input, Rail-to-Rail Output, Precision, 850 MHz Fully Differential Amplifier* data sheet provides only the *closed-loop output impedance* = 0.1 Ω. The *Small-Signal Frequency Response vs Gain* graph in the *Typical Characteristics: 5 V Single Supply* section of the *LMH5485-SP* data sheet provides the gain versus frequency curve. For the modulation frequency of 8.192 MHz, the graph shows about 38 dB, that is, about 80. With the relation of *closed-loop output impedance* × *open-loop gain* = *open loop output impedance* Ro-dif calculates as follows: 90 × 0.1 Ω = 8 Ω. Enter "8" (8 Ω) for the Ro-dif field.
Riso	**Riso** is typically tuned to a small value. Here "0" (0 Ω) is used.
Rg and Rf	**Rg and Rf** must be the same for unity gain. "1k" (1 kΩ) is typically a good starting point.
I_{PP}	The *LMH5485-SP* data sheet allows for up to 75 mA of output current. An unnecessarily high output current would cause power loss and heating of the FDA which may cause a drift from the optimal working point. A value of "8m" (8 mA) is enough to make calculations in this example.
fin	The required bandwidth is 40 kHz. With some margin, "50k" (50 kHz) is a good selection here.
UGBW	The **UGBW** of FDA is "859M" (850 MHz).
CSH	Use **CSH** from the *Equivalent Analog Input Circuitry* image in the *ADS1278-SP Radiation Hardened 8-Ch Simultaneous-Sampling 24-Bit Analog-to-Digital Converter* data sheet: "9p" (9 pF).
CFILT	Prior defining leaves **CFILT** as the last entries - press the *Calculate* button to obtain the updated values for **Cfilt_min** "180p" (180 pF) and **Cfilt_max** "5.1n" (5.1 nF). Use "2.2n" (2.2 nF) as the value somewhat in between 5 nF and 180 pF.

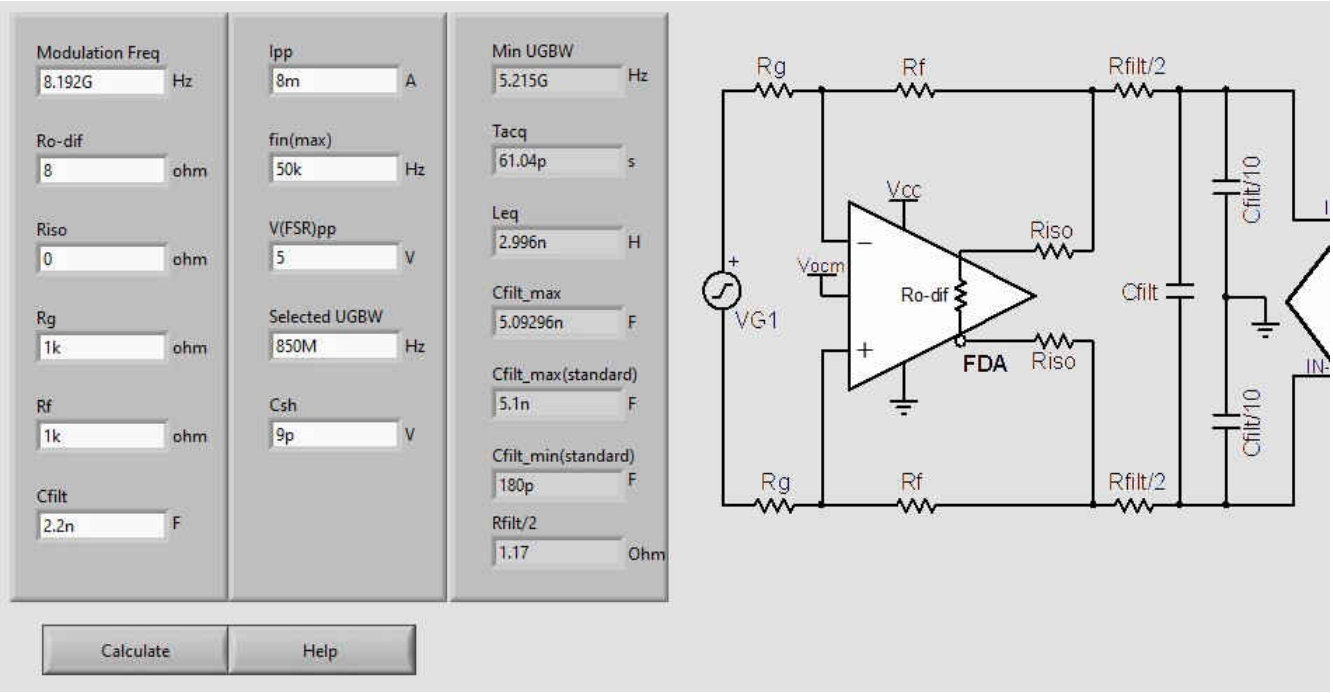


Figure 1-6. User Defined And Calculated Values For The Reference Schematic With LMH5485-SP and ADS1278-SP to Meet the Example Design Targets

In this chapter the best fitting ADC and ADC-driver was selected with the help of the *TI Space Products Guide* and the ANALOG-ENGINEER'S CALCULATOR was used to determine its supporting circuitry, including all component values. Further, a basic understanding of the circuit and the role of each of the active and passive components was developed.

2 Verification

This chapter shows how to verify the example design towards the desired design goals with the help of both the TINA TI Simulator tool and the ANALOG-ENGINEER'S CALCULATOR. The section also shows how to verify that the signal chain performs to the full differential and common-mode input range of the ADC. Then the total noise performance and the linearity are observed to determine if the ENOB target can be met, followed by a stability analysis and verification of the input impedance. Finally, the chapter provides proof that the circuit meets the settling time requirement of the sample and hold capacitor of the ADC.

2.1 Detailed Design Procedure – Verification of the Time Domain Response

As Figure 2-1 shows, before the verification analysis can start, the design must first complete the attenuation and input buffer stage. The important design goals to remember here are a single-ended ±10-V input signal is translated into a ± 2.5-V differential signal for the ADC input and the input impedance must be > 100 kΩ.

For the input buffer, the LMP7704-SP device was selected. The resistor divider network of the attenuation stage brings the signal level down by a factor of four. The input signal generator VG1 is set to 240-kHz sine wave with ±10-V amplitude.

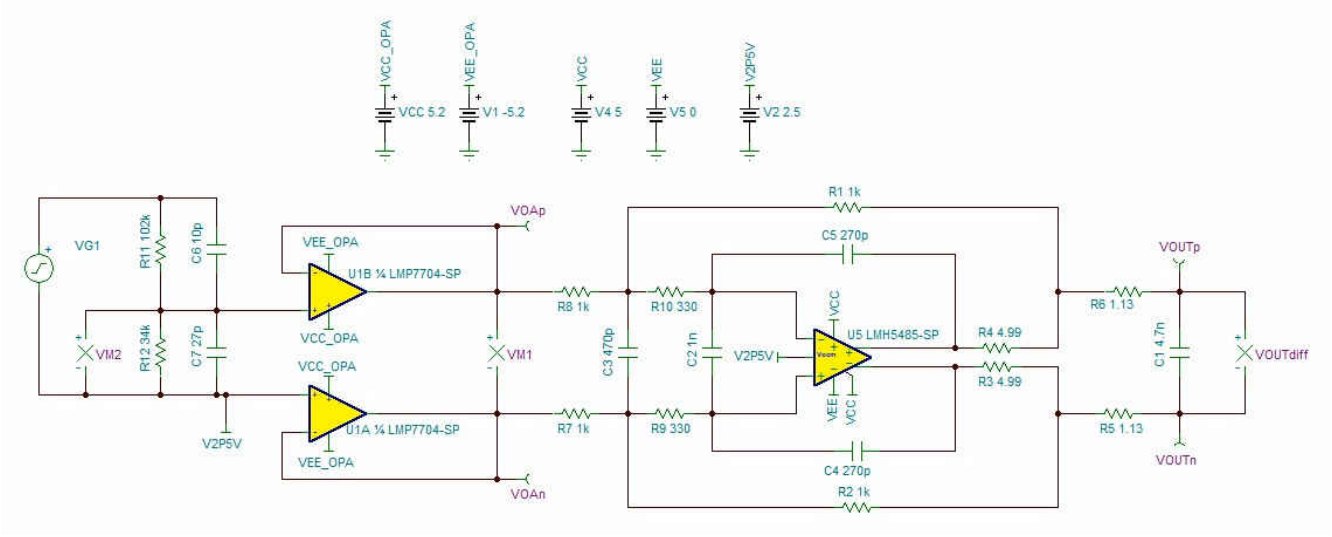


Figure 2-1. Addition of Attenuation Stage and Input Buffer Stage to the FDA Circuit

Figure 2-2 shows the selection of *Transient…* in the *Analysis* menu of TINA-TI and setting the simulation window from "0" to "100u" (100 µs).

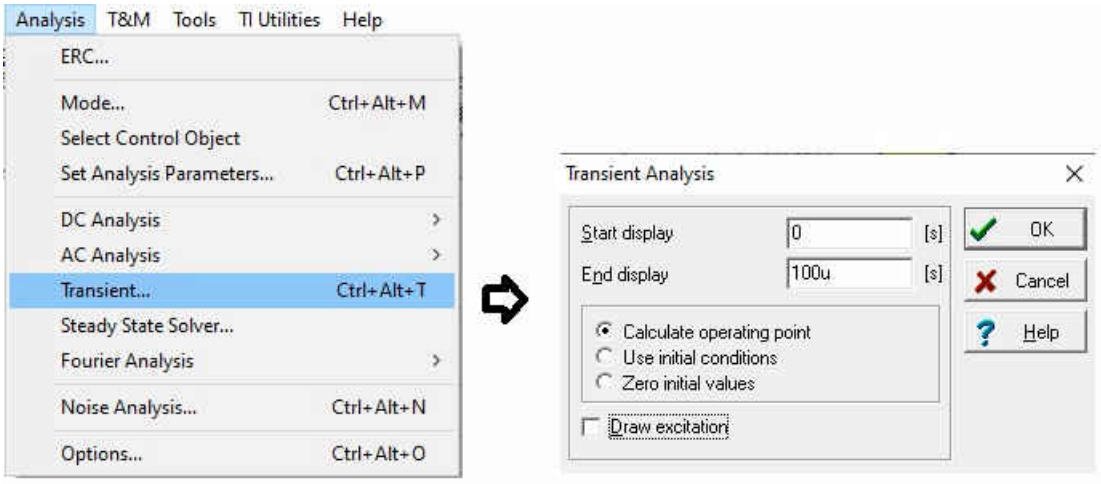


Figure 2-2. Running the Transient Analysis From 0 to 100 µs

The returned waveform in Figure 2-3 shows that the single-ended input signal with an amplitude of 10 V results into a differential output signal with an amplitude of 2.5 V. This amplitude takes advantage of the full input voltage range of the ADC for the best possible resolution.

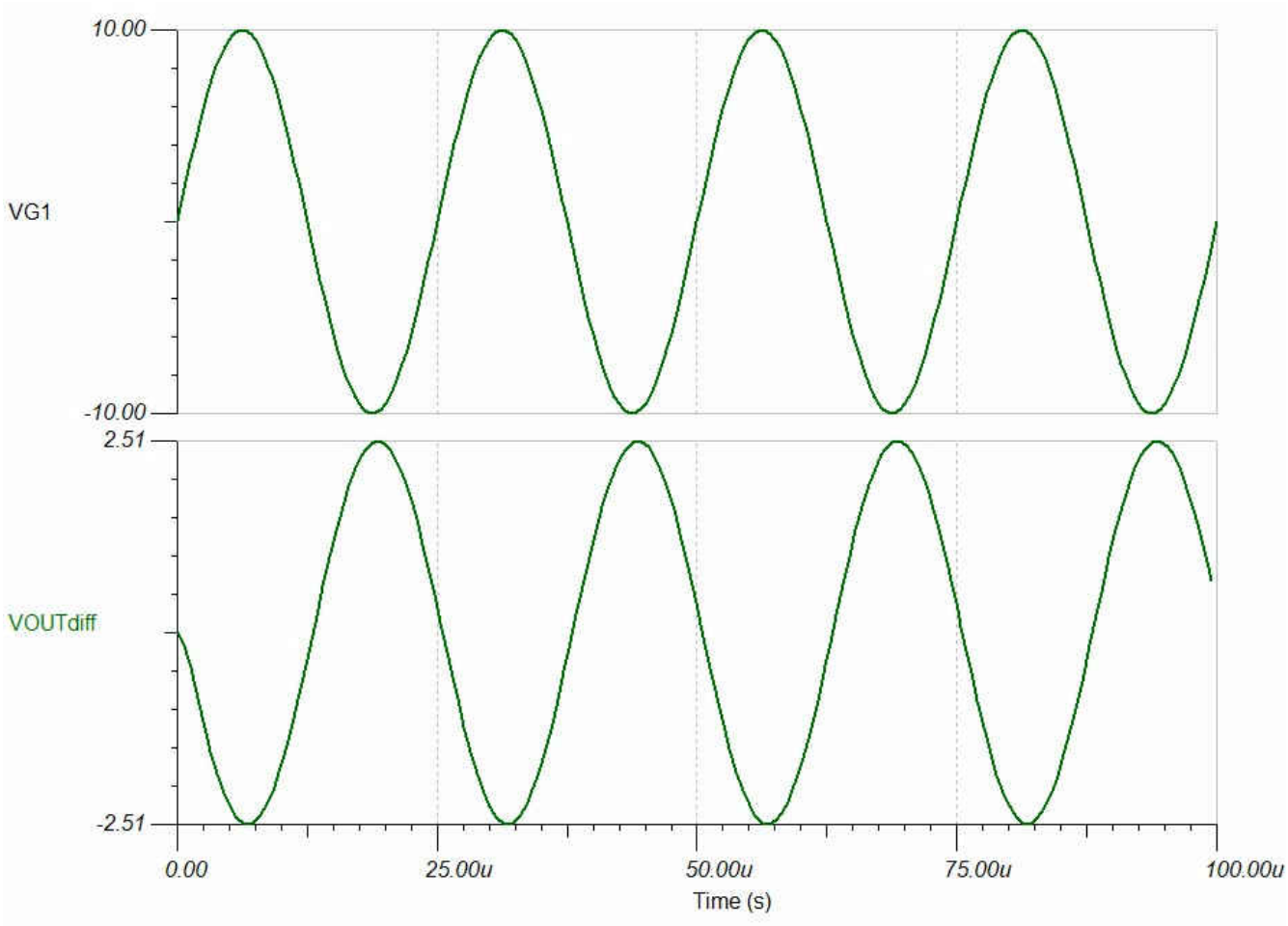


Figure 2-3. Simulation of FDA Output Voltage VOUTdiff Versus Input Signal VG1

2.2 Analysis of Total Noise

To accomplish 16 ENOBs it is fundamental that the signal is significantly stronger than the noise floor of the AFE system. In other words, the SNR value must be high enough.

The ANALOG-ENGINEER'S CALCULATOR provides an easy way to determine the total SNR of the AFE system. Using the ANALOG-ENGINEER'S CALCULATOR, Figure 2-4 illustrates the selection of *ADC + Signal Chain Noise* from the *Data Converters* menu.

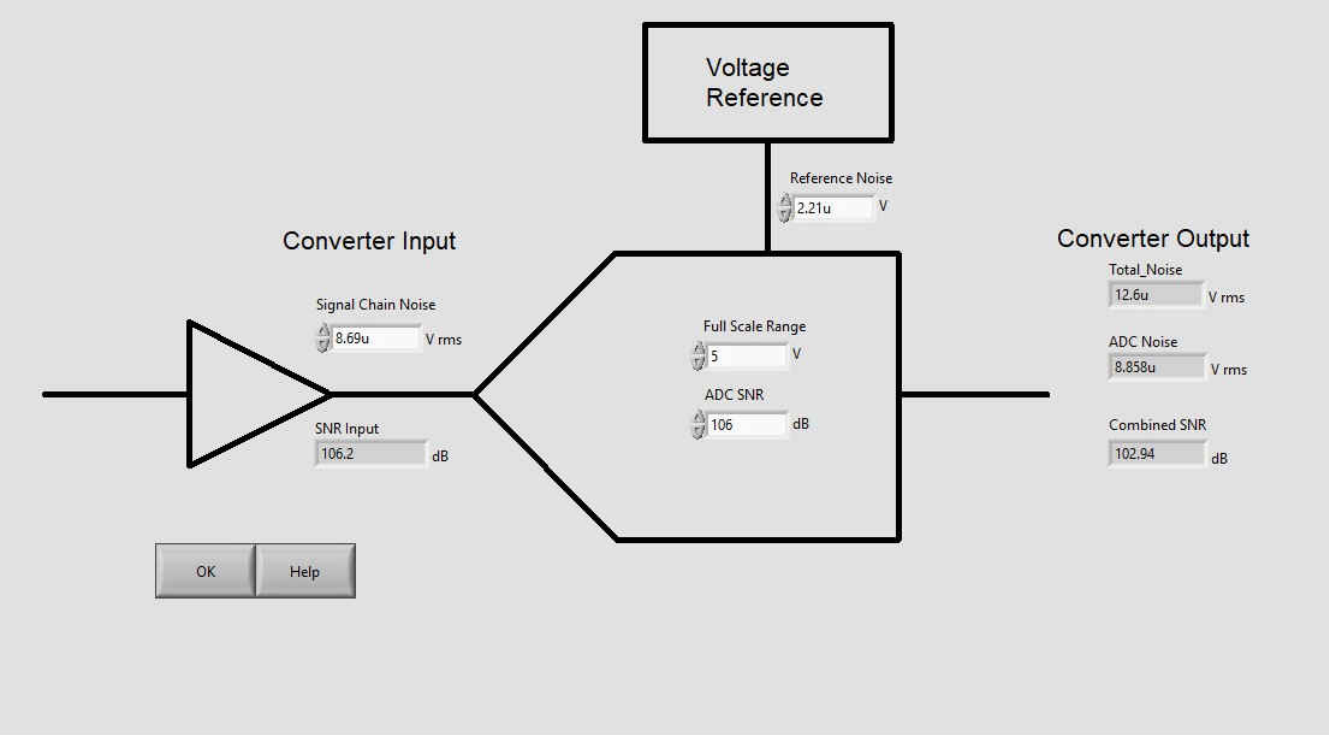


Figure 2-4. 'ADC + Signal Chain Noise' Analysis in ANALOG-ENGINEER'S CALCULATOR

The *Full Range Scale* is 5 V and the ADC SNR value is read from the *ADS1278-SP Radiation Hardened 8-Ch Simultaneous-Sampling 24-Bit Analog-to-Digital Converter* data sheet. The value for the *Signal Chain Noise* at the converter input requires a bit more effort. Use the TINA-TI simulator to analyze the schematic from Figure 2-1 for its total noise, reference Figure 2-5 and Figure 2-6.

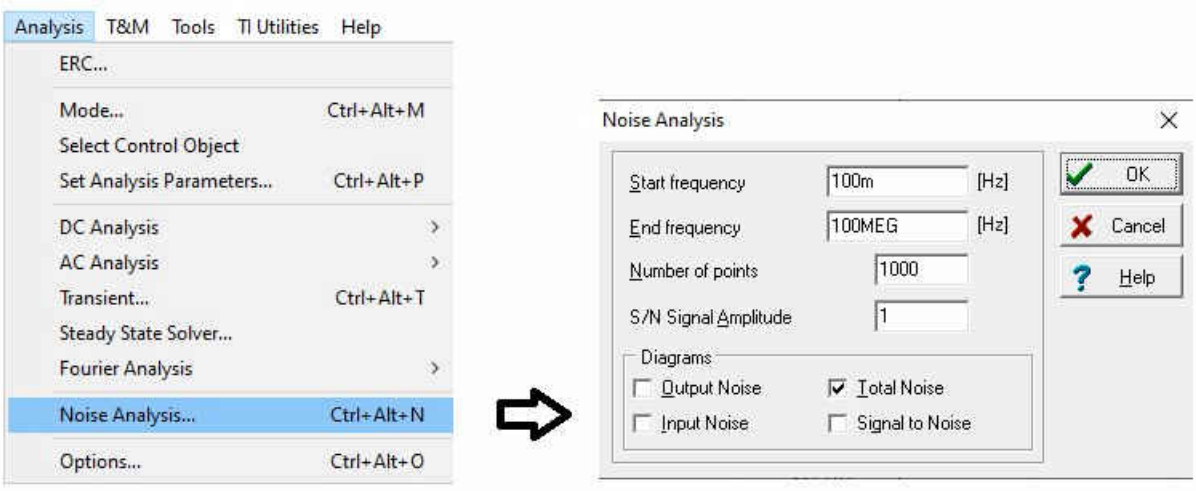


Figure 2-5. Select 'Noise Analysis' and Check 'Total Noise' in Tina-TI Simulator

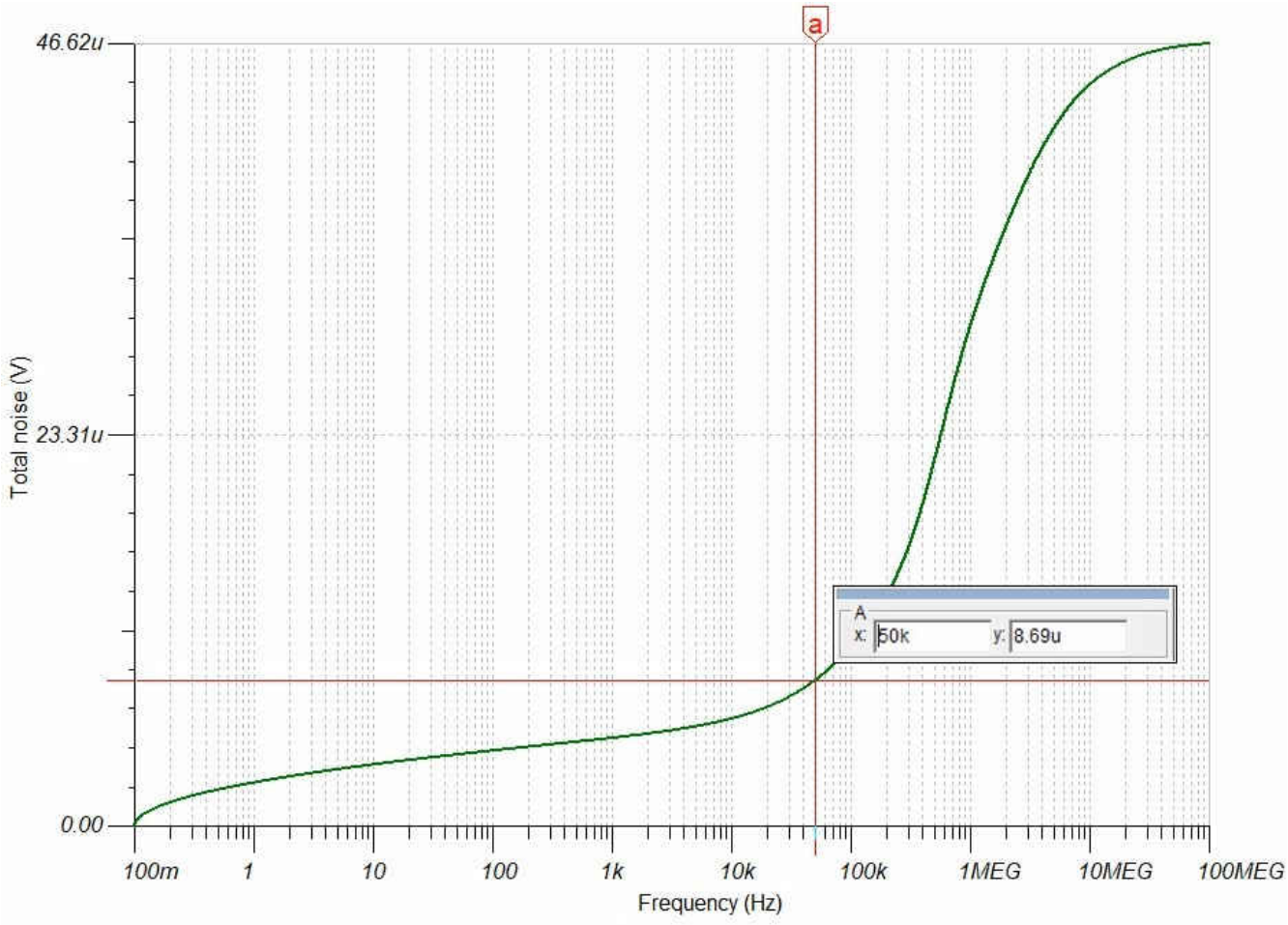


Figure 2-6. Total Noise Result of the Analog Input Circuit to the ADC

At 50 kHz - the highest frequency of interest with margin – TINA-TI returns 8.69 µV which can be entered into the ANALOG-ENGINEER'S CALCULATOR as shown in Figure 2-4.

The noise level for the voltage reference can be identified in a similar way with TINA-TI or simply read from the data sheet if just a regular shunt voltage reference device is used. For demonstration purposes, "2.21u" (2.21 µV) is chosen. After selecting the *OK* button, the tool returns 102.94 dB for the combined SNR.

Applying the standard conversion formula ENOB = (SNR – 1.76) / 6.02 dB, this calculates to ENOB = 16.81 bits.

Note

TINA-TI does not account for non-linearity. Therefore a quick look at the THD is necessary:

The *Harmonic Distortion Over Frequency* graph, Figure 2-7, from the LMH5485-SP data sheet shows distortion of –118 dBc for 50 kHz and below. Its absolute value of 118 dB is significantly enough higher than the previously-identified combined SNR of 102.94 dB. Distortion from non-linearity can therefore be ignored.

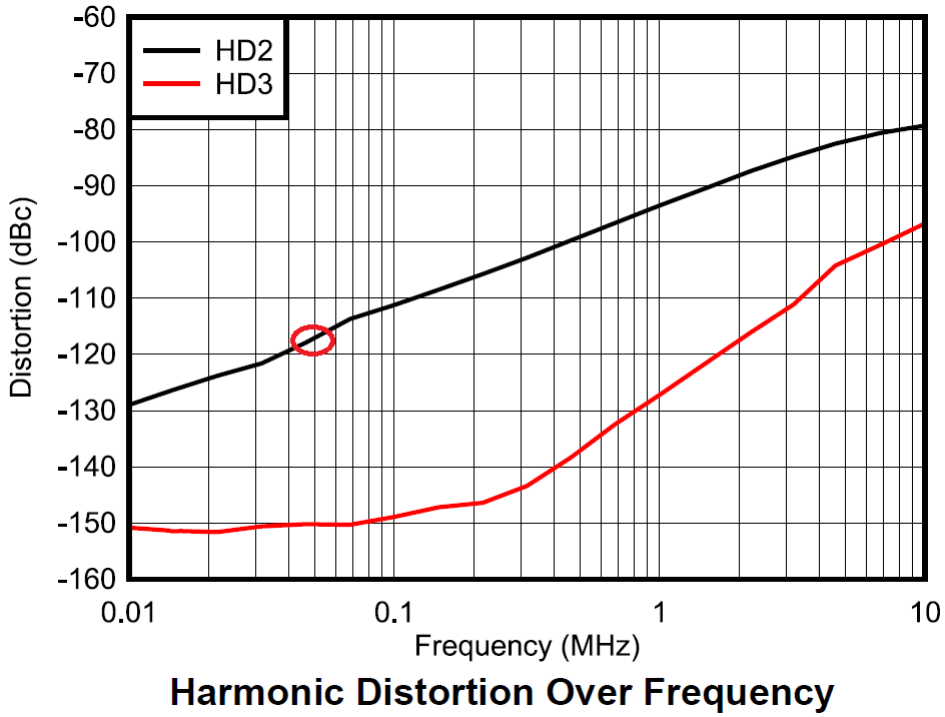


Figure 2-7. LMH5485-SP Data Sheet Shows THD of About –118 dBc for f = 50 kHz in its Harmonic Distortion Over Frequency Chart

2.3 Linearity or Frequency Response

This section looks at the frequency response of the input circuit to verify that the bandwidth is wide enough to preserve the signal of interest across its entire bandwidth but also be narrow enough to act as an anti-aliasing filter.

For this, the signal chain from signal input to ADC input must be analyzed, in other words, the same circuit as shown in Figure 2-1. Figure 2-8 shows the selection of the *AC Transfer Characteristic* option in the *Analysis* menu in the TINA-TI simulator. Use this option to analyze the frequency response for amplitude and phase.

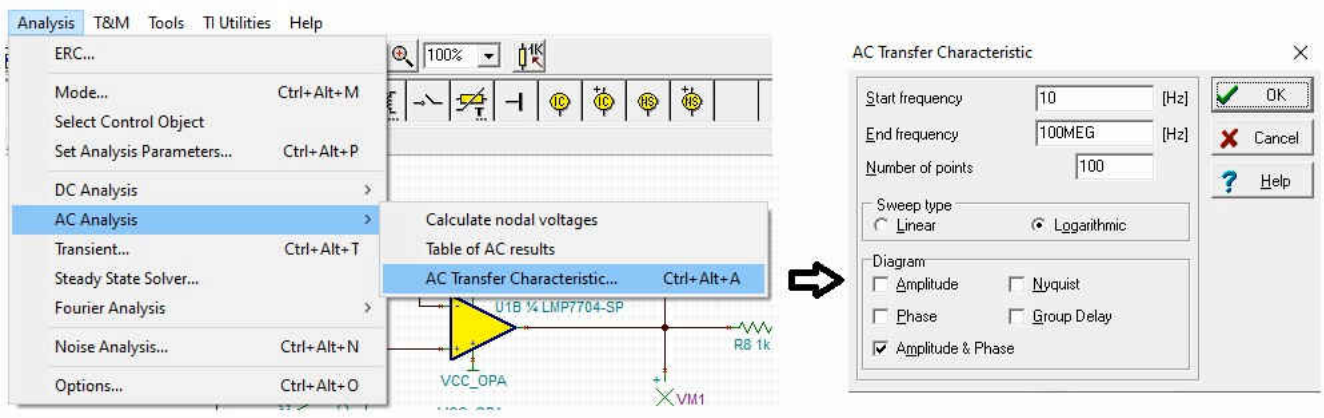


Figure 2-8. Select AC Transfer Characteristic to Analyze the Frequency Response of the Input Circuit

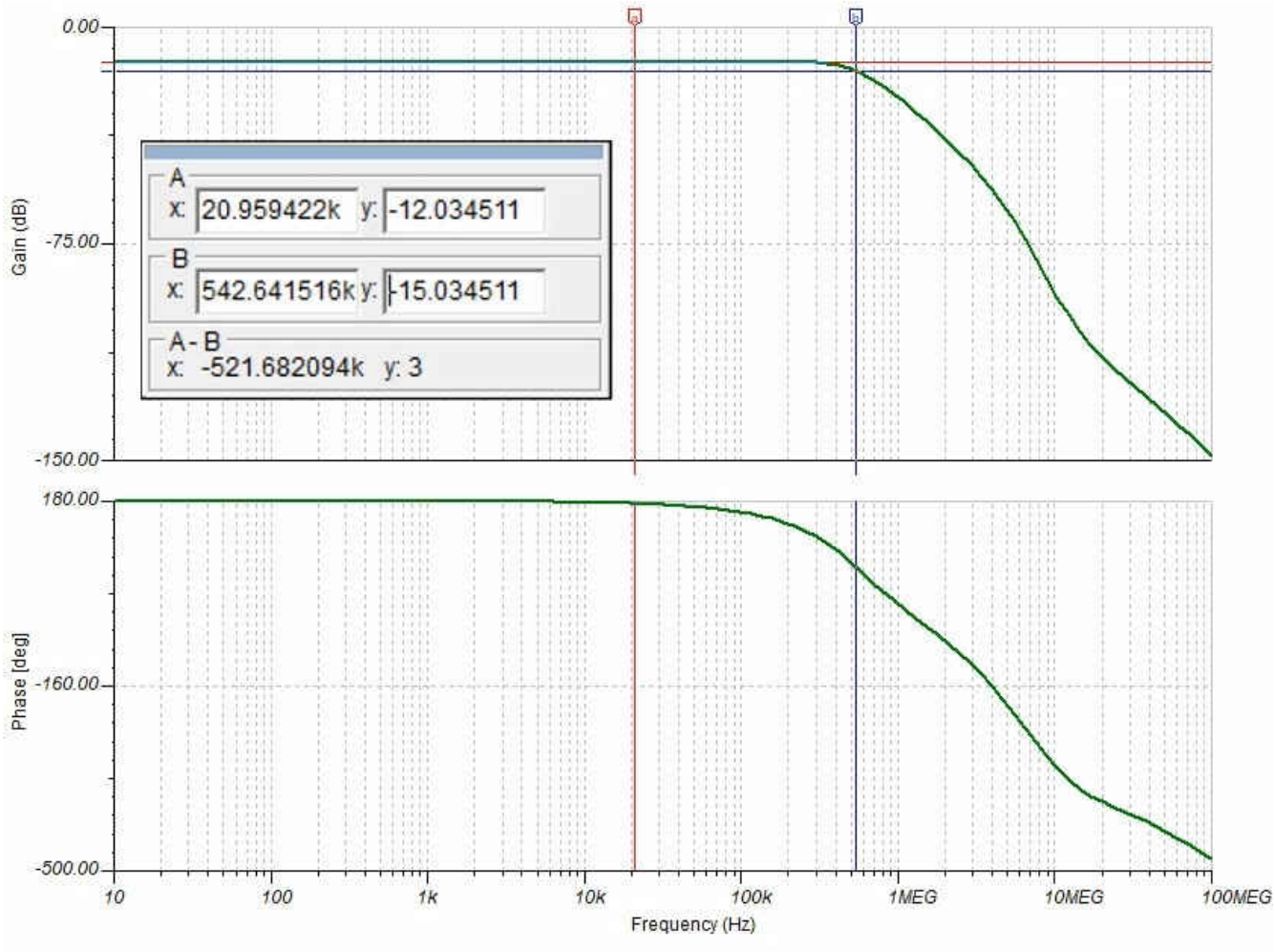


Figure 2-9. AC Transfer Characteristic of Analog Front End – 3 dB Bandwidth of VOUTdiff is 542.96 kHz

For the lower frequencies, the gain is stable at –12.04 dB. The –3-dB bandwidth (–15.04 dB) shows at 542.96 kHz, see Figure 2-9. This is very well above the cutoff frequency of 60 kHz of the digital filter response of the ADS1278. The linearity requirement for the bandwidth of interest is clearly met.

The second concern is on aliasing. ADS1278-SP is a sigma-delta modulator. In this example, the device modulates the signal with 8.192 MHz. Accordingly, Nyquist is at f_{mod} / 2 = 4.096 MHz. The gain shows –57 dB at that frequency which means only 45-dB suppression at the Nyquist frequency. The result from simulation is an indication that further measures for suppression of frequencies at and above 4 MHz might be required.

2.4 Stability

Along with the FDA stage, the AFE design contains a closed-loop system that raises the concern for instability causing ringing or even oscillation. The standard way to understand the likelihood for oscillation is to analyze the Bode plot and verify that there is enough phase margin.

Before the FDA stage can be analyzed, it must be isolated from the rest of the circuit and the feedback path must be opened up to allow for extracting the open loop gain as shown in Figure 2-10. In addition TINA-TI must be enabled to properly converge for any frequency, including DC. All this is accomplished by adding capacitors and inductors with Terra values, practically infinite capacity or inductivity, respectively. The huge capacitor acts like a short for any frequency above a few Hertz and as an open for DC. Likewise, the giant inductor acts as a short for DC and as an open for any frequency higher than a few Hertz. Obviously, this is only practical for the simulation. The higher the values that are selected the closer the simulation will remain to reality, the circuit without such added capacitors and inductors.

The output load must stay included so it continues to interact with the output impedance of the amplifier as it would in the complete AFE implementation. The introduction of the large inductors disconnect the input impedance of the op amp from the circuit. R_Diff and C_Diff are therefore added back in to find the correct open loop gain.

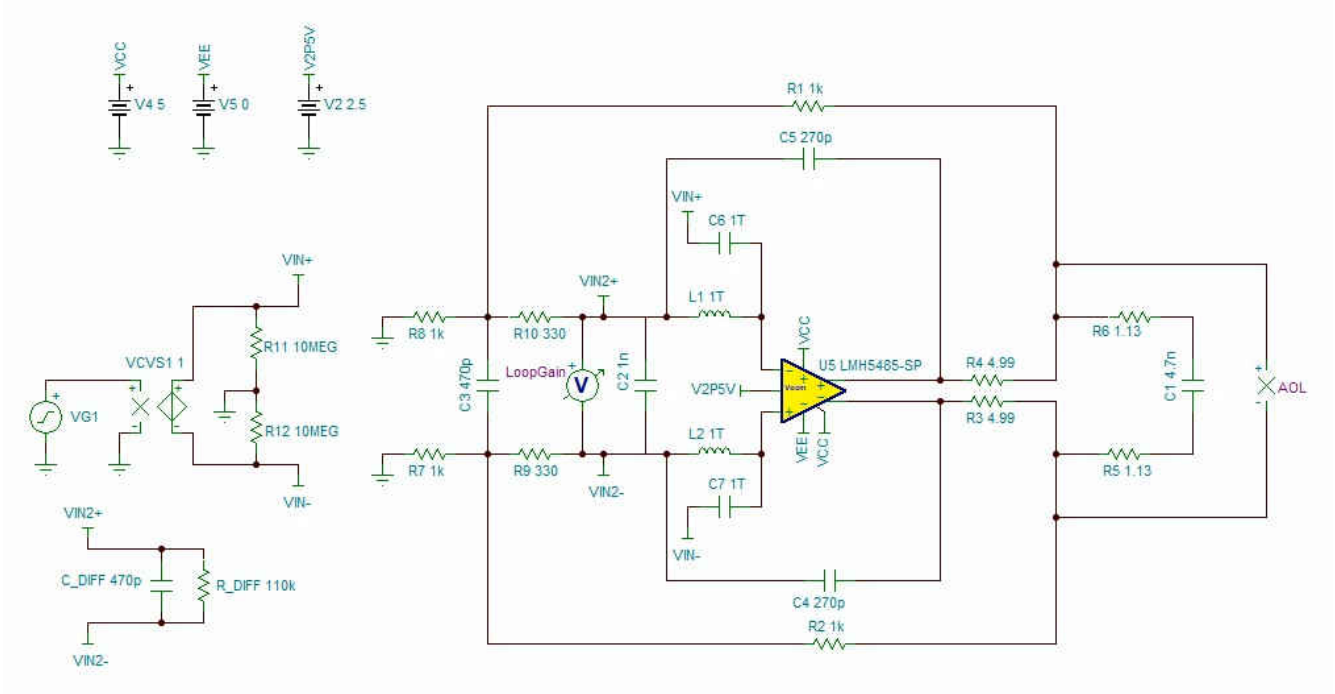


Figure 2-10. Closed-Loop System Extracted and Prepared for Stability Analysis

As in Section 2.3, the AC Transfer Characteristic in TINA-TI simulator is used to analyze the frequency response for amplitude and phase for the FDA stage in open loop configuration, see Figure 2-11.

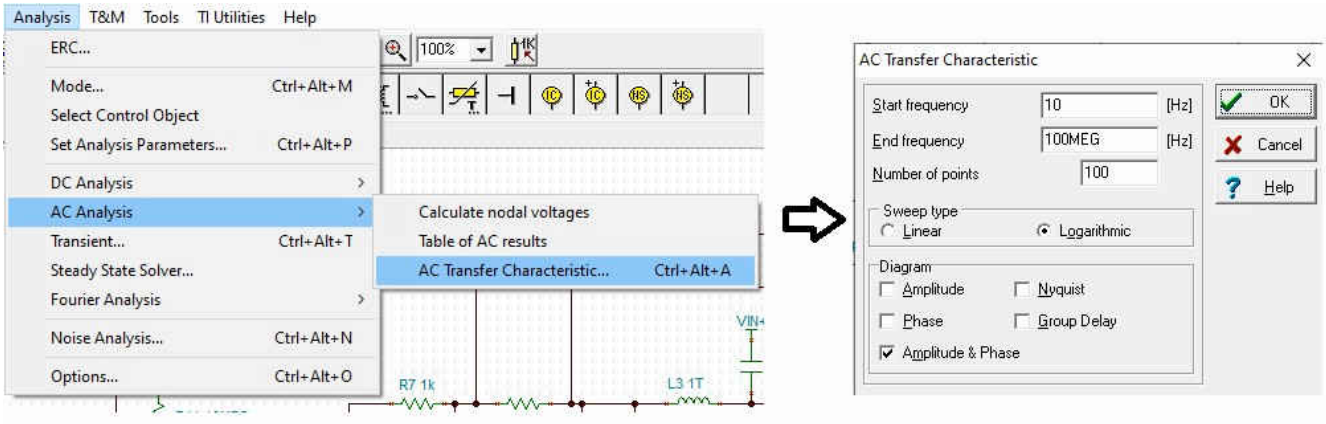


Figure 2-11. Selection of AC Transfer Characteristic to Analyze the Frequency Response for Amplitude and Phase for the FDA Stage in Open Loop Configuration

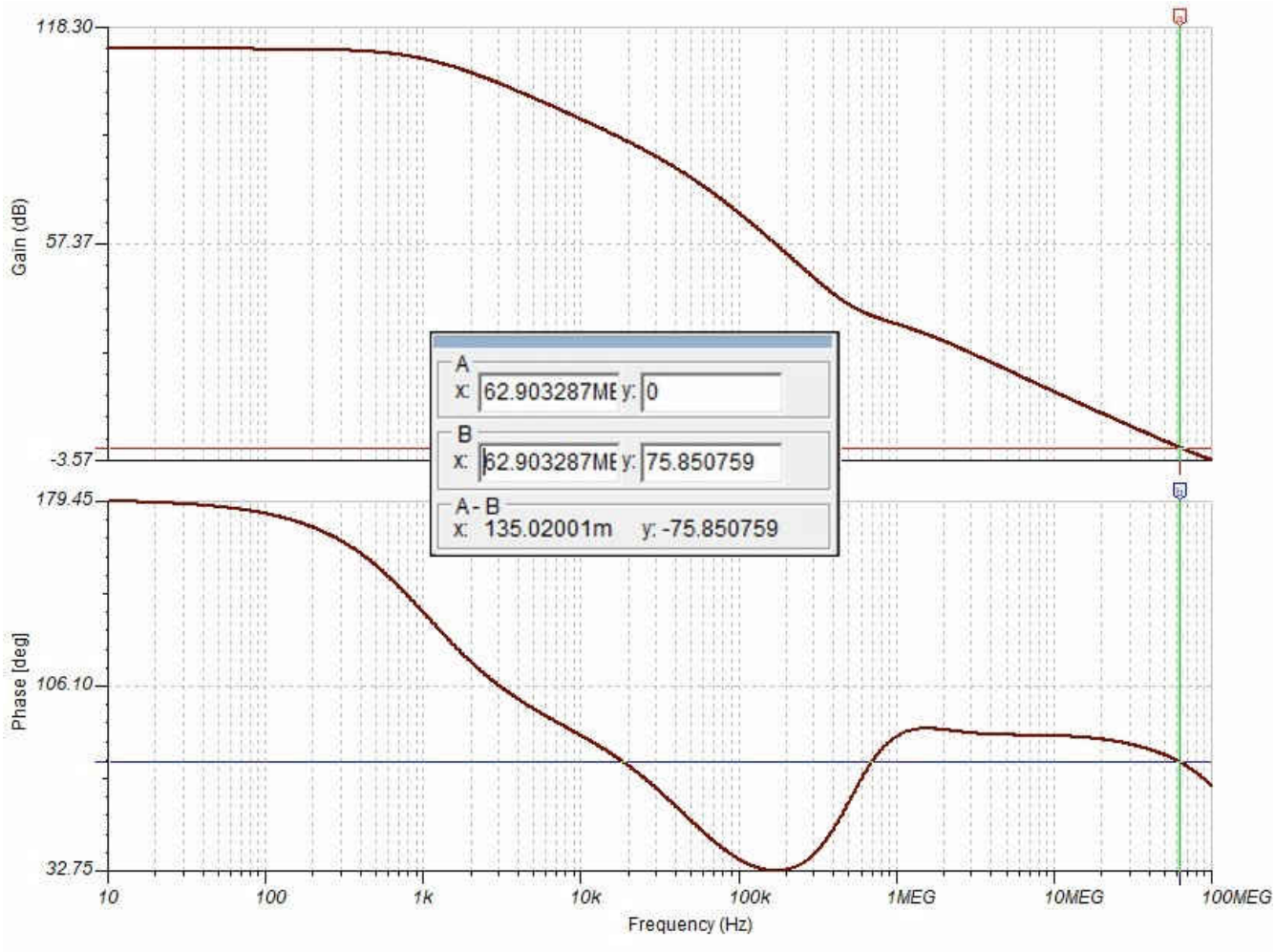


Figure 2-12. Bode Plot for the FDA Stage in Open Loop Configuration

The resulting Bode plot in Figure 2-12 shows sufficient stability with a phase of 75.85° at the crossover frequency of 62.9 MHz. The dip in phase margin at about 150 kHz might allow for some ringing. Remember this issue in case it appears in the actual design.

2.5 Settling Time

The final analysis verifies if the settling time at the ADC input is short enough. For each sampling, the ADC must charge its internal sample and hold capacitor. During the setup time, the charge is transferred over from the external buffer capacitor. After the setup time, the ADC driver must be strong enough to recharge the buffer capacitor on time.

The worst-case condition for the settling time is when the signal input is set to 10 V. This will generate the max Vdiff output of –2.5 V or –2.499541 V, to be precise. Figure 2-13 illustrates using the *DC Analysis* option in the TINA-TI simulator to find the exact voltage that the 10-V input voltage generates at the ADC input.

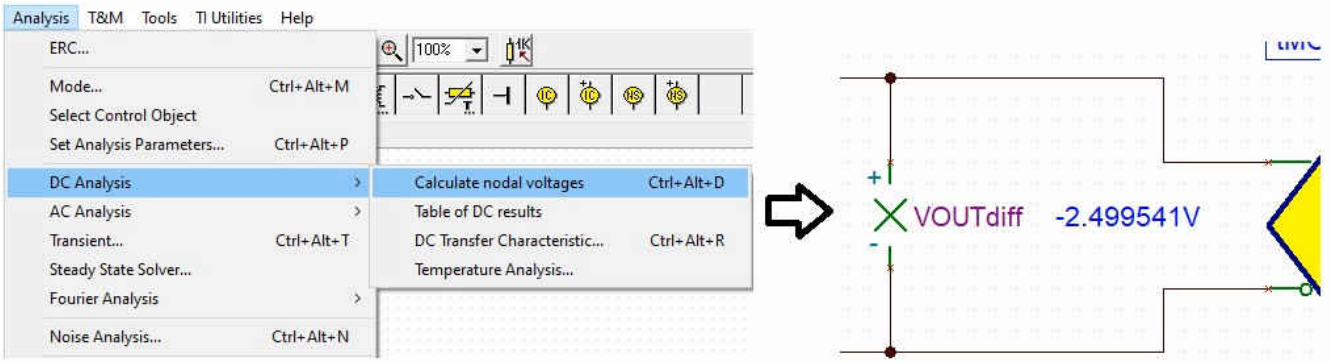


Figure 2-13. Use DC Analysis ➜ Calculate Nodal Voltages Option to Identify the Precise Input Voltage to the ADC

The ADS1278 simulation model provides the output of the sample-and-hold capacitor. If the voltage settles correctly it is exactly at –2.499541 V. Figure 2-14 shows this voltage is applied to this pin in the simulation via an extra voltage source, plus a voltage meter to measure the error from that expected voltage.

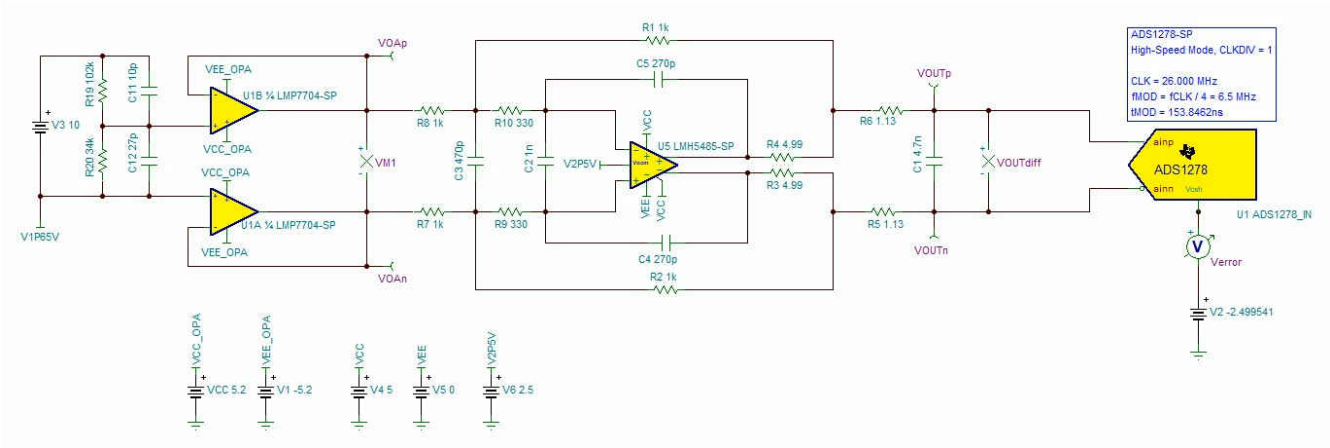


Figure 2-14. Complete AFE System for Settling Time Analysis

Figure 2-15 illustrates how the simulation is activated by selecting the TC transfer option from the analysis window.

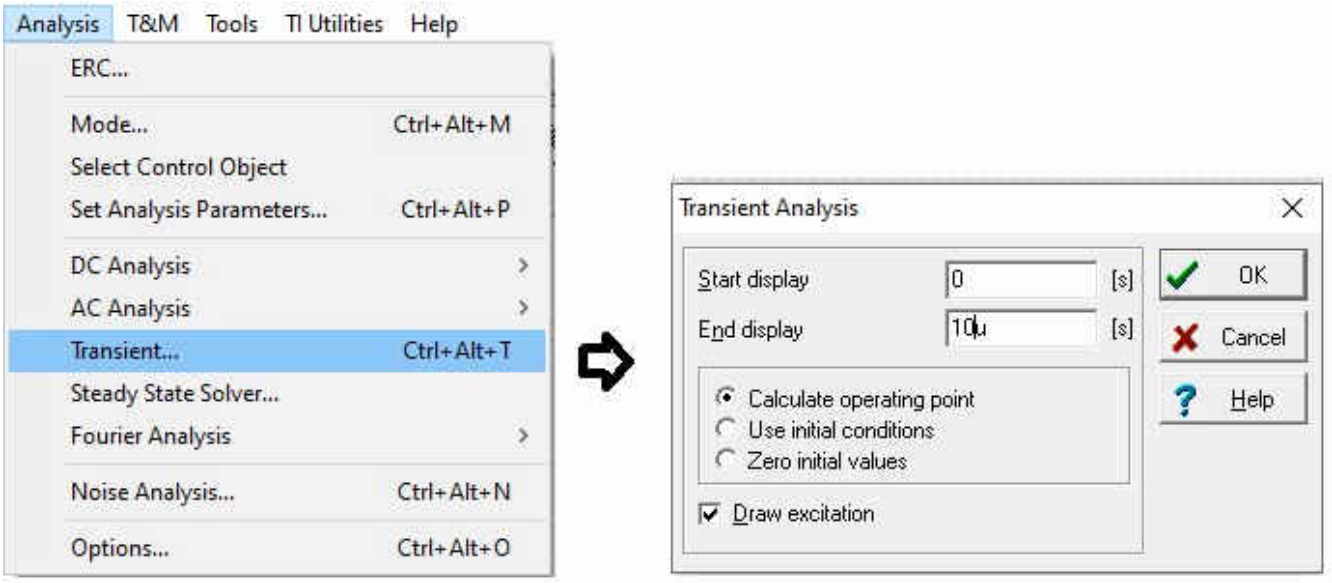


Figure 2-15. Select TC Transfer Option to Analyze the Settling Time

Figure 2-16 shows a zoomed in view of the graph of the error voltage after the settling of –4.153 µV. This error appears as a gain error, and reduces to approximately 0 V at 0-V input. In relation to the full excitation of –2.5 V, these –4.153 µV translate into a gain error of 0.0001663% or –1.663 ppm. This represents roughly a 20-bit resolution, hence the settling error is small enough to meet the original design goal of > 16 ENOB.

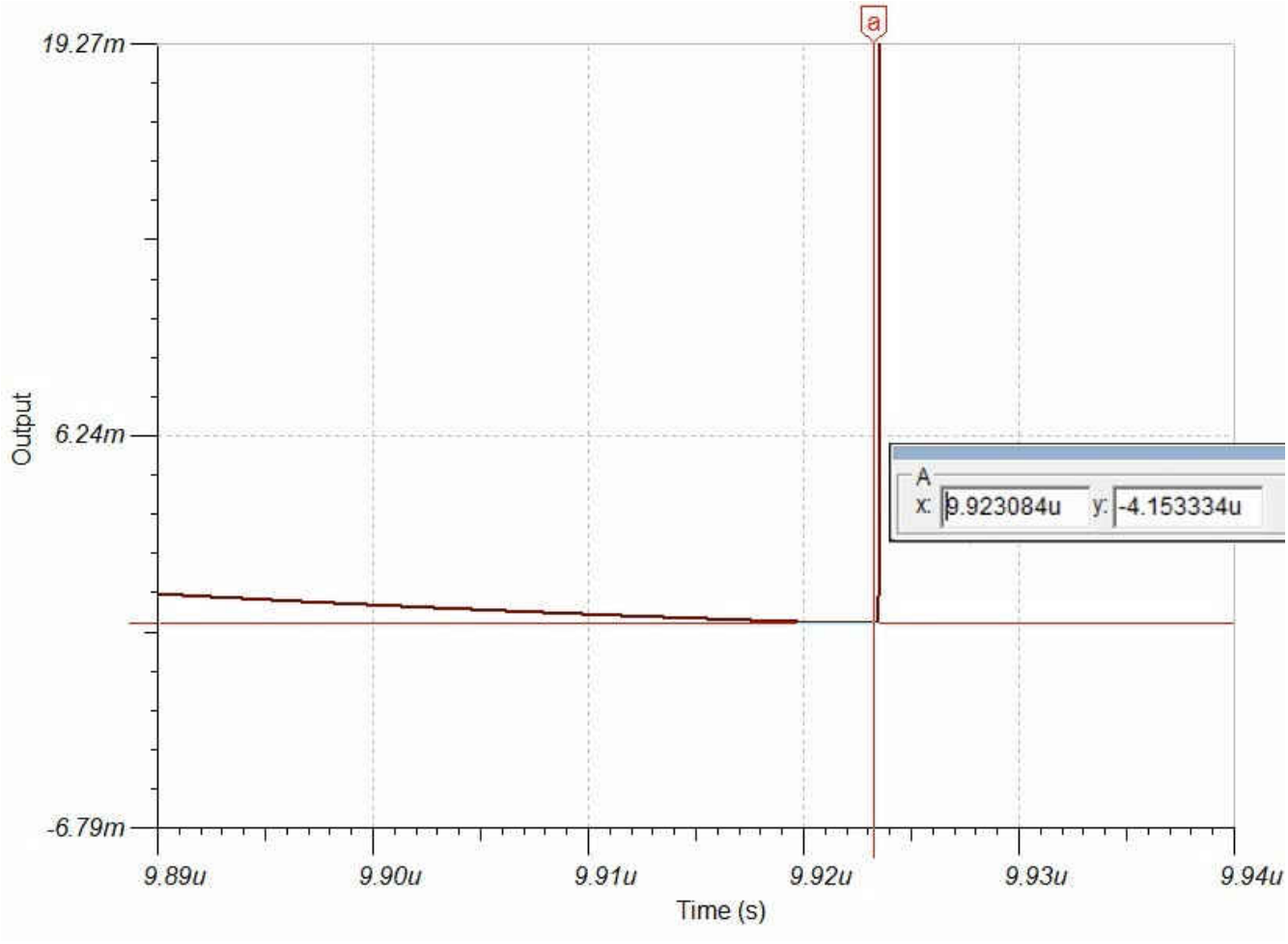


Figure 2-16. Simulation Result of the Sample-and-Hold Capacitor Voltage Error of the ADS1278 at the End of the Settling Window

Note

To obtain high enough resolution, it might be necessary to adjust the analysis parameters. Figure 2-17 shows an example adjustment with the previously-mentioned parameters.

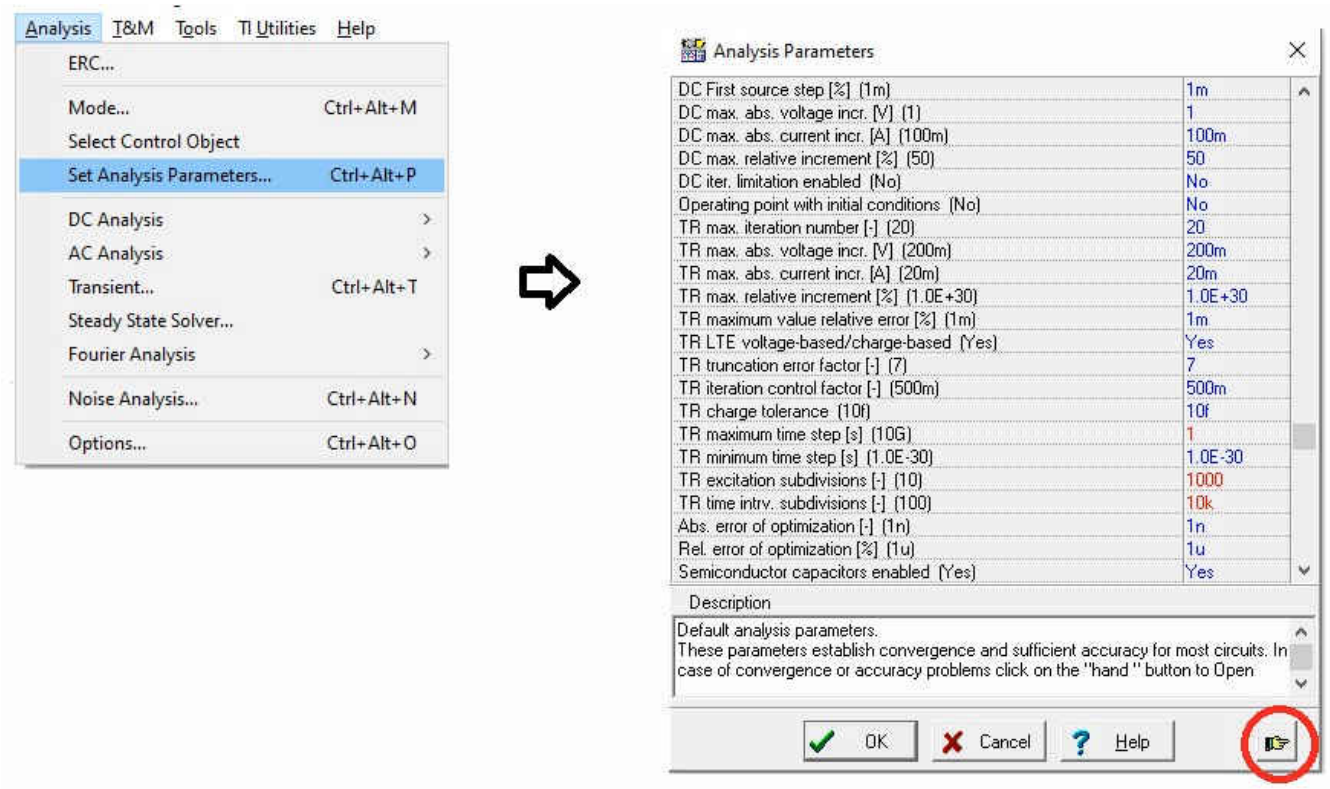


Figure 2-17. Adjusting Analysis Parameters for High Resolution (Numbers in Red), Press On the 'Hand Icon' to Get the Full List

3 Summary

The development of an analog front-end for precision ADCs is a complex design challenge that must meet several aspects such as basic functionality, linearity, stability, SNR, and settling time.

TI's tooling landscape enables designers to easily identify a good starting point for their design and verify each optimization iteration towards their design goals effectively.

There are many more examples, detailed explanations and design aspects discussed in the online video curriculum Precision Labs. There is also the TI E2E™ forum to provide support on any specific design or simulation step. Further, there are a wealth of application reports and reference designs on ti.com.

If needed, be sure to ask for help or support from Texas Instruments. There is a mutual interest between TI and its customers to get any development done as quickly as possible.

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