

# Zero-Drift Amplifiers: Features and Benefits

Errol Leon, Richard Barthel, Tamara Alani



## Introduction

Zero-drift amplifiers employ a unique, self-correcting technology which provides ultra-low input offset voltage ( $V_{OS}$ ) and near-zero input offset voltage drift over time and temperature ( $dV_{OS}/dT$ ) suitable for general and precision applications. TI's zero-drift topology also delivers other advantages including no  $1/f$  noise, low broadband noise, and low distortion – simplifying development complexity and reducing cost. This may be done 1 of 2 ways; chopper or auto-zeroing. This tech note will explain the differences between standard continuous-time and zero-drift amplifiers.

## Applications suitable for zero-drift amplifiers

Zero-drift amplifiers are suitable for a wide variety of general-purpose and precision applications that benefit from stability in the signal path. The excellent offset and drift performance of these amplifiers make it especially useful early in the signal path, where high gain configurations and interfacing with micro-volt signals are common. Common applications that benefit from this technology include precision strain gauge and weight scales, current shunt measurement, thermocouple-, thermopile-, and bridge-sensor interfaces.

## Rail-to-rail zero-drift amplifiers

System performance can be optimized by using standard continuous-time amplifiers plus a system-level auto-calibration mechanism. However, this additional auto-calibration requires complicated hardware and software which results in increased development time, cost and board space. The alternative and more efficient solution is to use a zero-drift amplifier, such as the OPA388.

A traditional rail-to-rail input CMOS architecture has two differential pairs; one PMOS transistor pair (blue) and one NMOS transistor pair (red). Zero-drift amplifiers with rail-to-rail input operation use the same complementary p-channel (blue) and n-channel (red) input configuration shown below in [Figure 1](#).

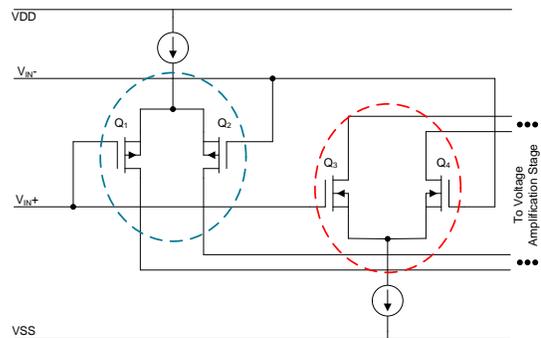


Figure 1. Simplified PMOS / NMOS Differential Pair

The result of this input architecture exhibits some degree of crossover distortion (for more information on crossover distortion, see [Zero-crossover Amplifiers: Features and Benefits](#)). However, the offset of the amplifier is corrected through internal periodic calibration, so the magnitude of the offset transition and the crossover distortion is greatly diminished. [Figure 2](#) shows a comparison of the offset between a standard CMOS rail-to-rail and a zero-drift amplifier.

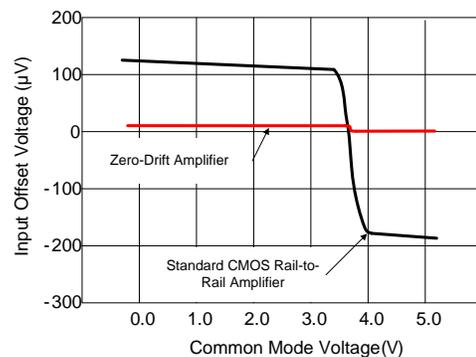
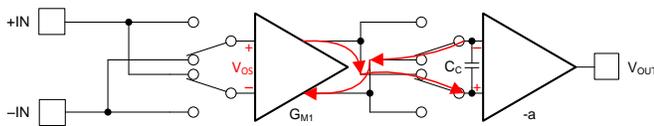


Figure 2. CMOS and Zero-drift Input Offset Voltage Comparison

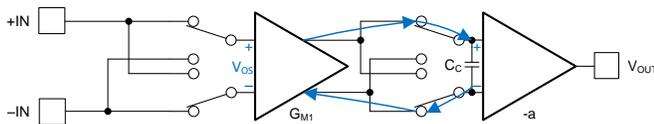
## How zero-drift works

Chopping zero-drift amplifiers' internal structure can have as many stages as continuous-time amplifiers – the main difference is that the input and output of the first stage has a set of switches that inverts the input signal every calibration cycle. [Figure 3](#) shows the first half cycle. In the first half cycle, both sets of switches are configured to flip the input signal twice, but the offset flips once. This keeps the input signal in phase but the offset error polarity is reversed.



**Figure 3. First Half-cycle of Internal Structure**

Figure 4 shows the second half cycle. Here, both sets of switches are configured to pass the signal and offset error through unaltered. Effectively, the input signal is never out of phase, remaining unchanged from end to end. Since the offset error from the first clock phase and second clock phase are opposite in polarity, the error is averaged to zero.



**Figure 4. Second Half-cycle of Internal Structure**

A synchronous notch filter is used at the same frequency of switching to attenuate any residual error. This principle continues to be in effect throughout the amplifier's operation across its input, output and environment. In essence, TI's zero-drift technology delivers ultra-high performance and outstanding precision owing to this self-correcting mechanism.

Table 1 shows a comparison of  $V_{OS}$  and  $dV_{OS}/dT$  of a continuous-time and zero-drift amplifier. Notice that the  $V_{OS}$  and  $dV_{OS}/dT$  are three orders of magnitude smaller on the zero-drift amplifier.

**Table 1. Input Offset Voltage and Drift Comparison**

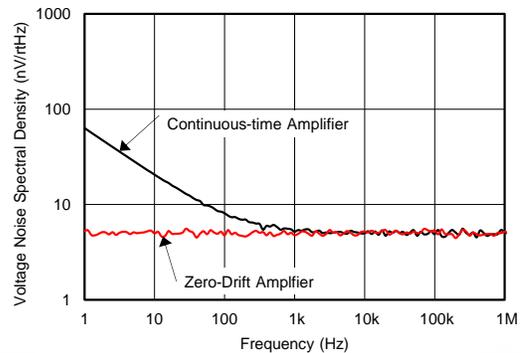
Device		$V_{OS}$ ( $\mu\text{V}$ )	$dV_{OS}/dT$ ( $\mu\text{V}/^\circ\text{C}$ )
OPA388 (Zero-drift)	typ	0.25	0.005
	max	5	0.05
OPA2325 (Continuous-time)	typ	40	2
	max	150	7.5

Auto-zeroing requires a different topology but results in similar functionality. The auto-zeroing technique has less distortion at the output. Chopping results in lower broadband noise.

### Noise in zero-drift amplifiers

In general, zero-drift amplifiers offer the lowest 1/f noise (0.1Hz – 10Hz). 1/f noise (also referred to as flicker or pink noise) is the dominant noise source at low frequencies and can be detrimental in precision DC applications. Zero-drift technology effectively cancels slow varying offset errors (such as temperature drift and low frequency noise) using the periodic self-correcting mechanism.

Figure 5 shows the 1/f and broadband voltage noise spectral density for a zero-drift (red) and continuous-time (black) amplifier. Notice the zero-drift curve has no 1/f voltage noise.



**Figure 5. Voltage Noise Comparison**

### Again, why zero-drift?

Zero-drift amplifiers provide ultra-low input offset voltage, near-zero input offset voltage drift over temperature and time, and no 1/f voltage noise – design factors which are crucial to general purpose and precision applications.

### Additional Resources

Table 2 below highlights some of TI's zero-drift amplifiers. For a full list, see our parametric search tool results by visiting: [ti.com/opamps](http://ti.com/opamps).

**Table 2. TI's Zero-Drift Amplifiers**

Device	Optimized Parameters
OPA388 2.5V<V <sub>s</sub> <5.5V	Zero-crossover, Offset (max): 5 $\mu\text{V}$ , Drift (max): 0.05 $\mu\text{V}/^\circ\text{C}$ , GBW: 10MHz, Noise: 7nV/ $\sqrt{\text{Hz}}$ , RRIO
OPA2333P 1.8V<V <sub>s</sub> <5.5V	2mm x 2mm SON package, Offset (max): 10 $\mu\text{V}$ , Drift (max): 0.05 $\mu\text{V}/^\circ\text{C}$ , $I_{Q(\text{max})}$ : 25 $\mu\text{A}/\text{Ch}$ , RRIO
OPA333 1.8V<V <sub>s</sub> <5.5V	Offset (max): 10 $\mu\text{V}$ , Drift (max): 0.05 $\mu\text{V}/^\circ\text{C}$ , $I_{Q(\text{max})}$ : 25 $\mu\text{A}/\text{Ch}$ , RRIO
OPA188 4V<V <sub>s</sub> <36V	Offset (max): 25 $\mu\text{V}$ , Drift (max): 0.085 $\mu\text{V}/^\circ\text{C}$ , GBW: 2MHz, Noise: 8.8nV/ $\sqrt{\text{Hz}}$ , RRO
OPA317 1.8V<V <sub>s</sub> <5.5V	Offset (max): 20 $\mu\text{V}$ , Drift (max): 0.05 $\mu\text{V}/^\circ\text{C}$ , $I_{Q(\text{max})}$ : 35 $\mu\text{A}/\text{Ch}$ , RRIO
OPA189 4.5V<V <sub>s</sub> <36V	Offset (max): 3 $\mu\text{V}$ , Drift (max): 0.02 $\mu\text{V}/^\circ\text{C}$ , GBW: 14MHz, Noise: 5.2nV/ $\sqrt{\text{Hz}}$ RRIO

**Table 3. Related Documentation**

SBOA181	Zero-crossover Amplifiers: Features and Benefits
---------	--

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale ([www.ti.com/legal/termsofsale.html](http://www.ti.com/legal/termsofsale.html)) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2019, Texas Instruments Incorporated