Optimizing Sensor Measurement: Driving a SAR ADC Input Without a Driver Amplifier

A Successive Approximation Register (SAR) Analog to Digital Converter (ADC) is an excellent choice when it comes to measurement systems that require low latency. Most of the SAR ADCs have an analog input structure which is the combination of a sampling switch, switch resistance and sampling capacitor. In the sampling phase, a sampling switch is closed and the sampling capacitor is charged to the input voltage. To achieve the desired precision and full throughput performance for an ADC, an ADC driver amplifier is frequently used. *But do SAR ADCs always need a driver amplifier?* Not really! Many sensors can be directly connected to the input of a SAR ADC.

Figure 1 shows a typical application diagram for interfacing a sensor directly to a SAR ADC input without the use of a driver amplifier. The Sensor block highlights the Thevenin equivalent of a sensor output. Voltage source V_{TH} is the Thevenin equivalent voltage and source resistance R_{TH} is the Thevenin equivalent impedance. Most sensor data sheets provide the Thevenin model of the sensor from which the value of the series impedance can be easily calculated.

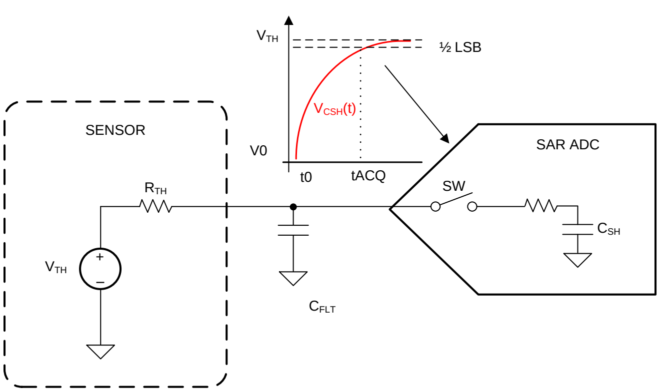

Figure 1. Interfacing SAR ADC Directly With Sensor Output

SAR ADCs can be directly interfaced with sensors when the analog input source is capable of driving the switched capacitor load of a SAR ADC and settling the analog input signal to within ½ of an LSB within the acquisition time of the SAR ADC. This is because ½ of an LSB is the maximum amount of voltage that an ADC can resolve due to its inherent quantization noise. To achieve this, the external RC filter (R_{TH} and C_{FLT}) must settle within the acquisition time (t_{ACQ}) of ADC. The relationship between the ADC acquisition time and RC time constant of the external filter is given by Equation 1.

$$t_{ACQ} > k \times \tau_{FLT} \tag{1}$$

where

- $\tau_{FLT} = R_{TH} \times C_{FLT}$
- k is the single pole time constant for N bit ADC which can be found on page 96 and page 97 of the *Analog Engineer's Pocket Reference*

For more information on SAR ADCs and front end design for SAR ADCs, refer to SAR ADC Precision Labs training video series.

The output impedance of the sensor must be taken into account when interfacing a SAR ADC directly with sensors. The input signal requires more acquisition time to settle to the desired accuracy if the output impedance of the sensor is higher. One way of interfacing high output impedance sensors directly with SAR ADC is to increase the acquisition time to allow the input signal to settle.

In applications such as environmental sensors, gas detectors and smoke or fire detectors where the input is very slow-moving, the sensor can be connected directly to the SAR ADC. The data acquisition circuit can be designed without the input driver because the ADC can run at a lower throughput rate which lengthens the acquisition period allowing the input signal to settle within ½ of an LSB. This direct interface of sensor to the SAR ADC enables lowest power, smallest size and lowest cost solution.

shows the timing diagram for the ADS7056 ADC. This device requires 18 clock falling edges to complete its conversion process and a minimum of 6 clocks for the acquisition of the input signal.

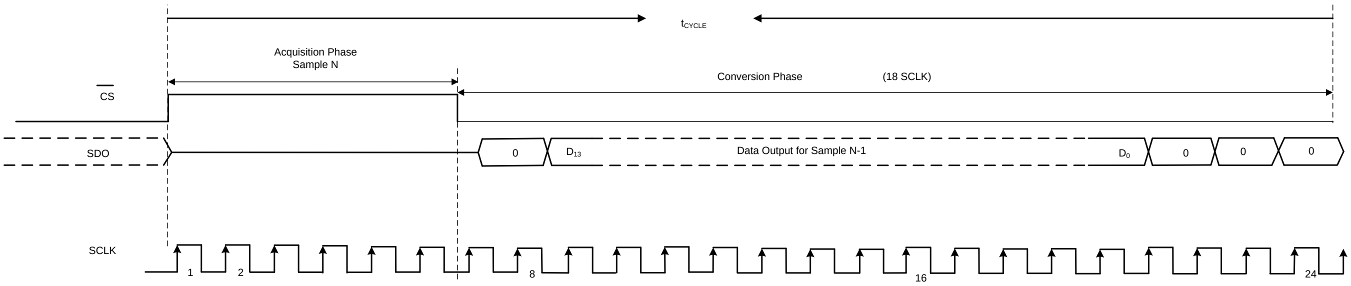

Figure 2. ADS7056 Timing Diagram for 1 Acquisition and Conversion Cycle

The acquisition time of a SAR ADC can be increased by reducing throughput in the following ways:

1. Reducing the SCLK frequency to reduce the throughput
2. Keeping the SCLK fixed at the highest permissible value (that is, 60 MHz for the device) and increasing the CS high time.

Table 1 lists the acquisition time for the above two cases for the ADS7056 SAR ADC operating at 100 kSPS throughput (t_{CYCLE} = 10 µs). We can see that Case 2 provides a longer acquisition time for the input signal to settle.

Table 1. ADS7056 Acquisition Time With Different Clock Speeds

CASE	SCLK	t_{CYCLE}	CONVERSION TIME (18 × t_{SCLK})	ACQUISITION TIME (t_{CYCLE} − t_{CONV})
1	2.4 MHz	10 µs	7.488 µs	2.512 µs
2	60 MHz	10 µs	0.3 µs	9.7 µs

Figure 3 provides the results for the Effective Number of Bits (ENOB) achieved from the ADS7056 for case 2 at different throughput with different input impedances. Note that all the results for Figure 3 were taken without an ADC driver amplifier.

For this example, you can see that optimal performance is achieved for sampling speeds less than 22 ksps for a wide range of sensor impedances. Most of the slow-moving (DC to 100 Hz) environmental sensors mentioned earlier such as smoke, gas, chemical, and temperature can be directly interfaced with low-resolution SAR ADCs operating at lower throughputs.

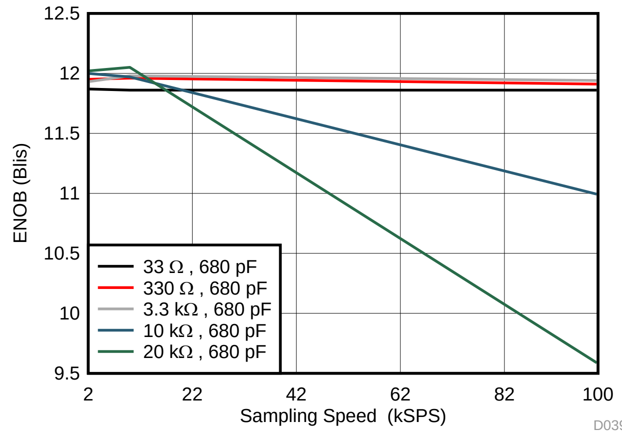

Figure 3. Performance Achieved at Different Throughput Rates of the ADS7056 Under Different Loading Conditions

Table 2 lists performance comparison between an 8-bit, 10-bit, 12-bit and 14-bit ADC with respect to sampling speed and ENOB when a sensor output with an output impedance of 10 kΩ is directly interfaced with the ADC input.

The ADS7042 and ADS7056 families of ultra-low-power, small-size SAR ADCs were especially designed to address system requirements of reducing cost, size and power and are well-suited for low-power sensing applications like the one described here.

Table 2. Sampling Speed and ENOB Performance Comparison Between ADCs

SAMPLING SPEED (ksps)	ADS7040 (8-BIT ADC) ENOB (R_{TH} = 10 kΩ, C_{FLT} = 1.5 nF)	ADS7041 (10-BIT ADC) ENOB (R_{TH} = 10 kΩ C_{FLT} = 1.5 nF)	ADS7042 (12-BIT ADC) ENOB (R_{TH} = 10 kΩ C_{FLT} = 1.5 nF)	ADS7056 (14-BIT ADC) ENOB (R_{TH} = 10 kΩ C_{FLT} = 680 pF)
10	7.93	9.87	10	12.05
100	7.92	9.85	9.97	10.99
500	7.88	9.68	9.95	8

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