Analog Engineer's Circuit

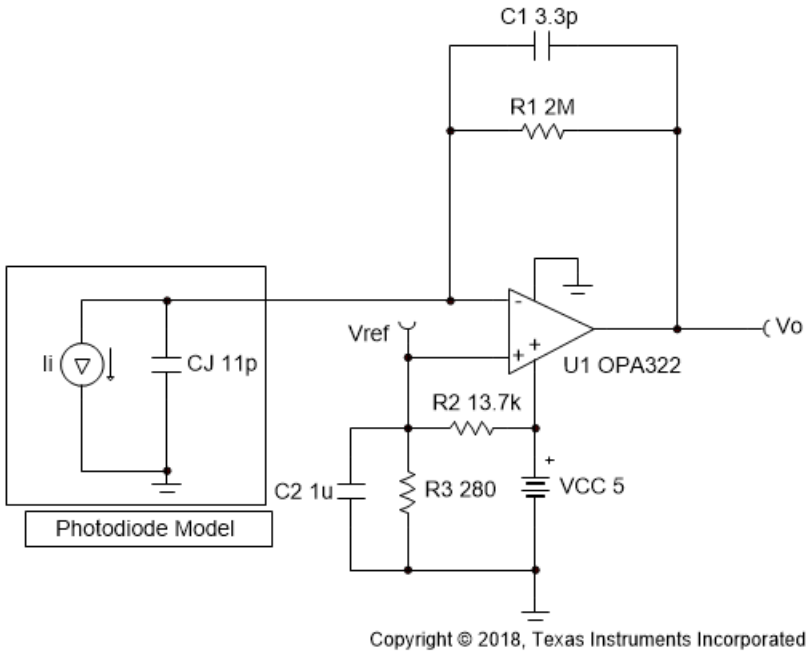
Photodiode Amplifier Circuit

Design Goals

Input		Output		BW	Supply		
I_{iMin}	I_{iMax}	V_{oMin}	V_{oMax}	f_p	V_{cc}	V_{ee}	V_{ref}
0 A	2.4 µA	100 mV	4.9 V	20 kHz	5 V	0 V	0.1 V

Design Description

This circuit consists of an op amp configured as a transimpedance amplifier for amplifying the light-dependent current of a photodiode.



Design Notes

1. A bias voltage (V_{ref}) prevents the output from saturating at the negative power supply rail when the input current is 0 A.
2. Use a JFET or CMOS input op amp with low bias current to reduce DC errors.
3. Set output range based on linear output swing (see A_{ol} specification).

Design Steps

1. Select the gain resistor.

$$R_1 = \frac{V_{oMax} - V_{oMin}}{I_{iMax}} = \frac{4.9V - 0.1V}{2.4\mu A} = 2M\Omega$$

2. Select the feedback capacitor to meet the circuit bandwidth.

$$C_1 \leq \frac{1}{2 \times \pi \times R_1 \times f_p}$$

$$C_1 \leq \frac{1}{2 \times \pi \times 2M\Omega \times 20kHz} \leq 3.97pF \approx 3.3pF \text{ (Standard Value)}$$

3. Calculate the necessary op amp gain bandwidth (GBW) for the circuit to be stable.

$$GBW > \frac{C_i + C_1}{2 \times \pi \times R_1 \times {C_1}^2} > \frac{20pF + 3.3pF}{2 \times \pi \times 2M\Omega \times (3.3pF)^2} > 170kHz$$

where $C_i = C_j + C_d + C_{cm} = 11pF + 5pF + 4pF = 20pF$ given

- C_j: Junction capacitance of photodiode
- C_d: Differential input capacitance of the amplifier
- C_{cm}: Common-mode input capacitance of the inverting input

4. Calculate the bias network for a 0.1 V bias voltage.

$$R_2 = \frac{V_{cc} - V_{ref}}{V_{ref}} \times R_3$$

$$R_2 = \frac{5V - 0.1V}{0.1V} \times R_3$$

$$R_2 = 49 \times R_3$$

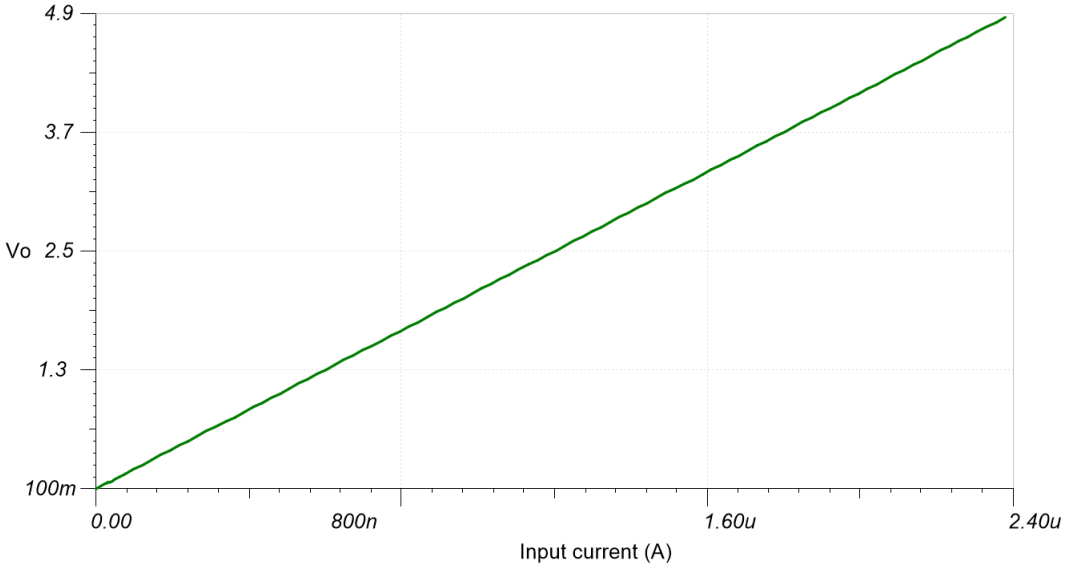
Closest 1% resistor values that yield this relationship are
$R_2 = 13.7k\Omega$ and $R_3 = 280\Omega$

5. Select C_2 to be 1 µF to filter the V_{ref} voltage. The resulting cutoff frequency is:

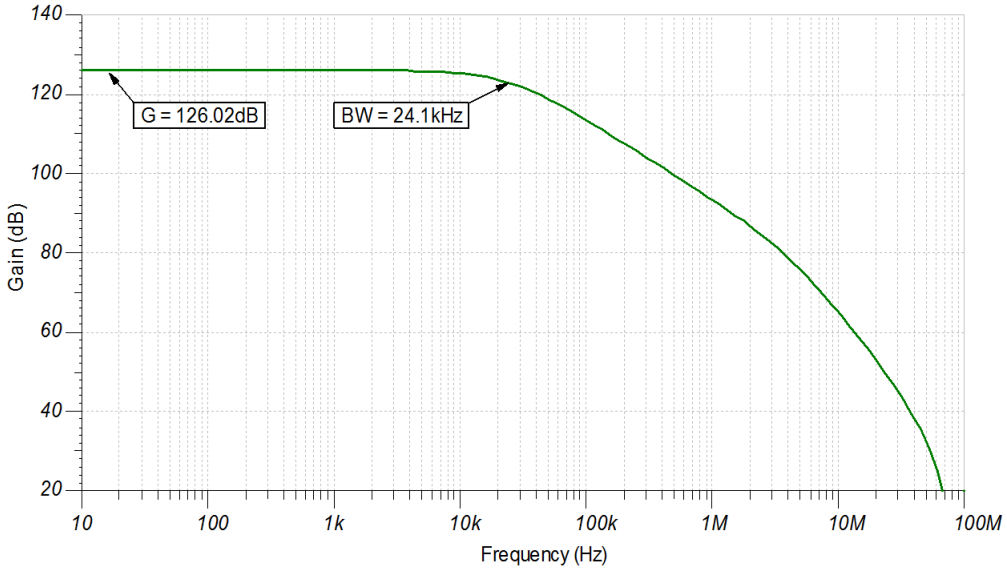
$$f_p = \frac{1}{2 \times \pi \times C_2 \times (R_2 \parallel R_3)} = \frac{1}{2 \times \pi \times 1\ \mu F \times (13.7k \parallel 280)} = 580Hz$$

Design Simulations

DC Simulation Results



AC Simulation Results



Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See the circuit SPICE simulation file SBOC517.

See TIPD176.

Design Featured Op Amp

OPA322	
V_{cc}	1.8 V to 5.5 V
V_{inCM}	Rail–to–rail
V_{out}	Rail–to–rail
V_{os}	0.5 mV
I_q	1.6 mA/Ch
I_b	0.2 pA
UGBW	20 MHz
SR	10 V/µs
#Channels	1, 2, and 4
OPA322	

Design Alternate Op Amp

LMP7721	
V_{cc}	1.8 V to 5.5 V
V_{inCM}	V_{ee} to (V_{cc} –1 V)
V_{out}	Rail–to–rail
V_{os}	26 µV
I_q	1.3 mA/Ch
I_b	3 fA
UGBW	17 MHz
SR	10.43 V/µs
#Channels	1
LMP7721	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from February 1, 2018 to February 4, 2019	Page
• Downscale the title and changed title role to 'Amplifiers'. Added links to circuit cookbook landing page and SPICE simulation file	1

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