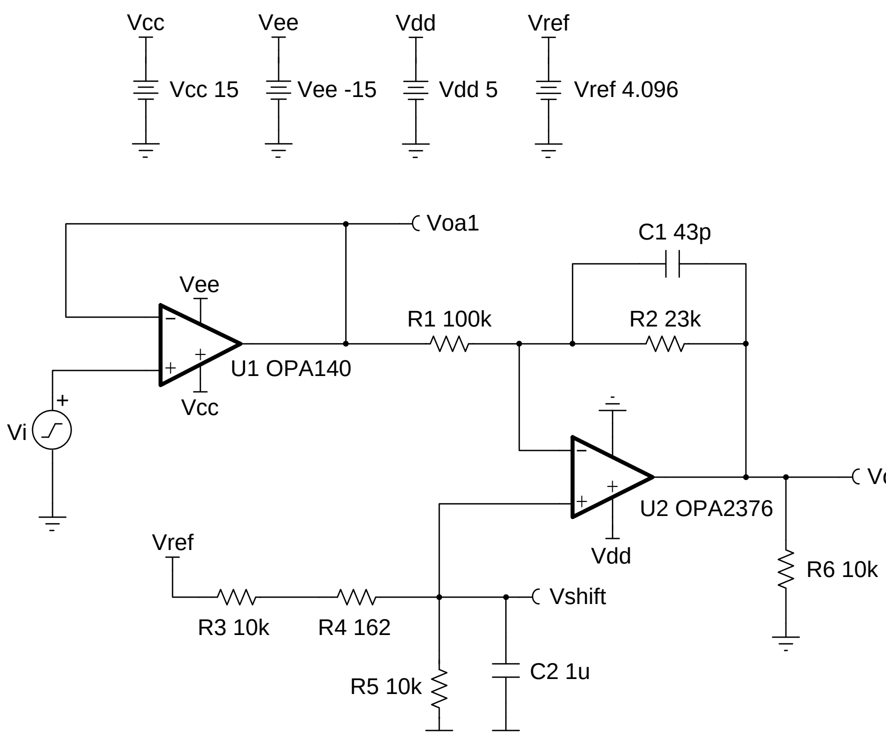
Inverting dual-supply to single-supply amplifier circuit

Design Goals

Input		Output		Supply			
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}	V_{dd}	V_{ref}
–10V	+10V	+0.2V	+4.8V	+15V	–15V	+5V	+4.096V

Design Description

This inverting dual-supply to single-supply amplifier translates a ±10-V signal to a 0-V to 5-V signal for use with an ADC. Levels can easily be adjusted using the given equations. The buffer can be replaced with other ±15-V configurations to accommodate the desired input signal, as long as the output of the first stage is low impedance.



Design Notes

1. Observe common-mode limitations of the input buffer.
2. A high-impedance source will alter the gain characteristics of U_2 if buffer amplifier U1 is not used.
3. R_6 provides a path to ground for the output of U_1 if the ±15-V supplies come up before the 5-V supply. This limits the voltage at the inverting pin of U_2 through the voltage divider created by R_1, R_2, and R_6 and prevents damage to U_2 as well as to any converter that may be connected to its output. To best protect the devices a transient voltage suppressor (TVS) should be used at the power pins of U_2.
4. A capacitor across R_5 will help filter V_{ref} and provide a cleaner V_{shift}.

Design Steps

The transfer function for this circuit follows:

$$V_o = -\frac{R_2}{R_1} \times V_i + \left(1 + \frac{R_2}{R_1}\right) \times V_{shift}$$

1. Set the gain of the amplifier.

$$\frac{\Delta V_o}{\Delta V_i} = \frac{V_{oMax} - V_{oMin}}{V_{iMax} - V_{iMin}} = \frac{4.8\ V - 0.2\ V}{10\ V - (-10\ V)} = 0.23$$

$$\frac{\Delta V_o}{\Delta V_i} = \frac{R_2}{R_1}$$

$$R_2 = 0.23 \times R_1$$

$$\text{Choose } R_1 = 100k\Omega \text{ (standard value)}$$

$$R_2 = 23k\Omega \text{ (for standard values use } 22k\Omega \text{ and } 1k\Omega \text{ in series)}$$

2. Set V_{shift} to translate the signal to single supply.

$$\text{At midscale, } V_{in} = 0V$$

$$\text{Then } V_o = \left(1 + \frac{R_2}{R_1}\right) \times V_{shift}$$

$$V_{shift} = \frac{V_o}{\left(1 + \frac{R_2}{R_1}\right)} = \frac{2.5V}{1.23} = 2.033V$$

3. Select resistors for reference voltage divider to achieve V_{shift}.

$$V_{ref} = 4.096V$$

$$V_{shift} = V_{ref} \times \frac{R_5}{(R_3 + R_4) + R_5}$$

$$\frac{V_{shift}}{V_{ref}} = \frac{2.033V}{4.096V} = \frac{R_5}{(R_3 + R_4) + R_5}$$

$$R_3 + R_4 = 1.0161 \times R_5$$

$$\text{Select a standard value for } R_5$$

$$R_5 = 10k\Omega$$

$$R_3 + R_4 = 10.161k\Omega$$

$$R_3 = 10k\Omega$$

$$R_4 = 162\Omega \text{ (standard 1\% value)}$$

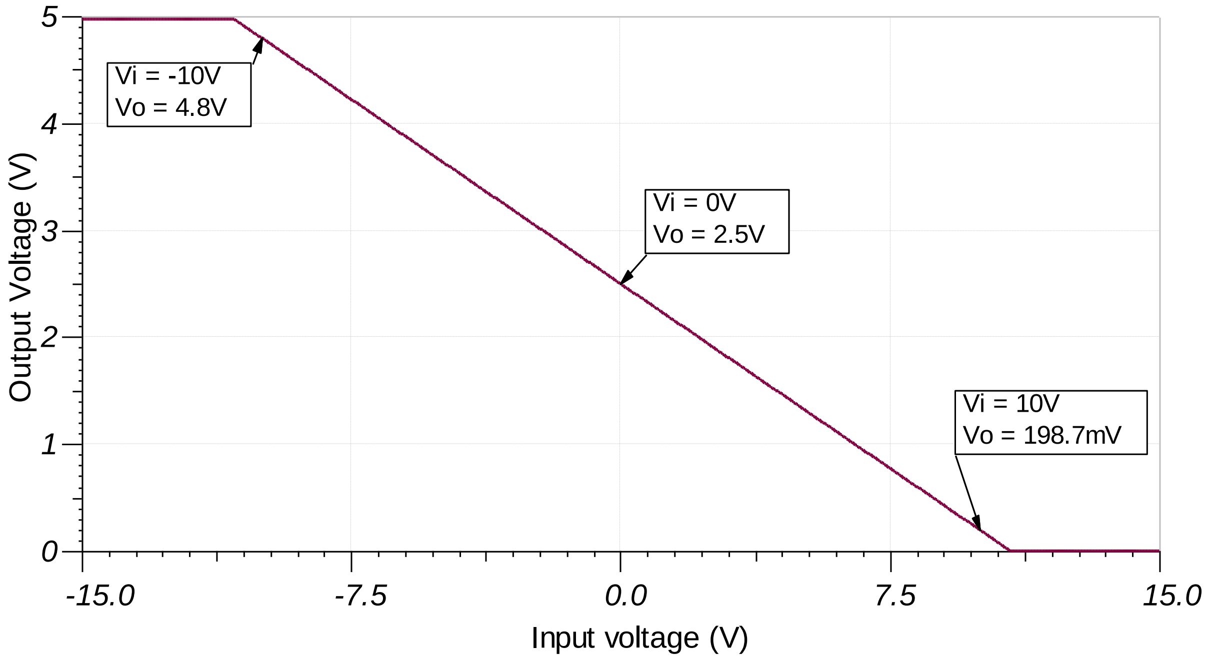
4. Large feedback resistors can interact with the input capacitance and cause instability. Choose C_1 to add a pole to the transfer function to counteract this. The pole must be lower in frequency than the effective bandwidth of the op amp.

$$C_1 = 43pF$$

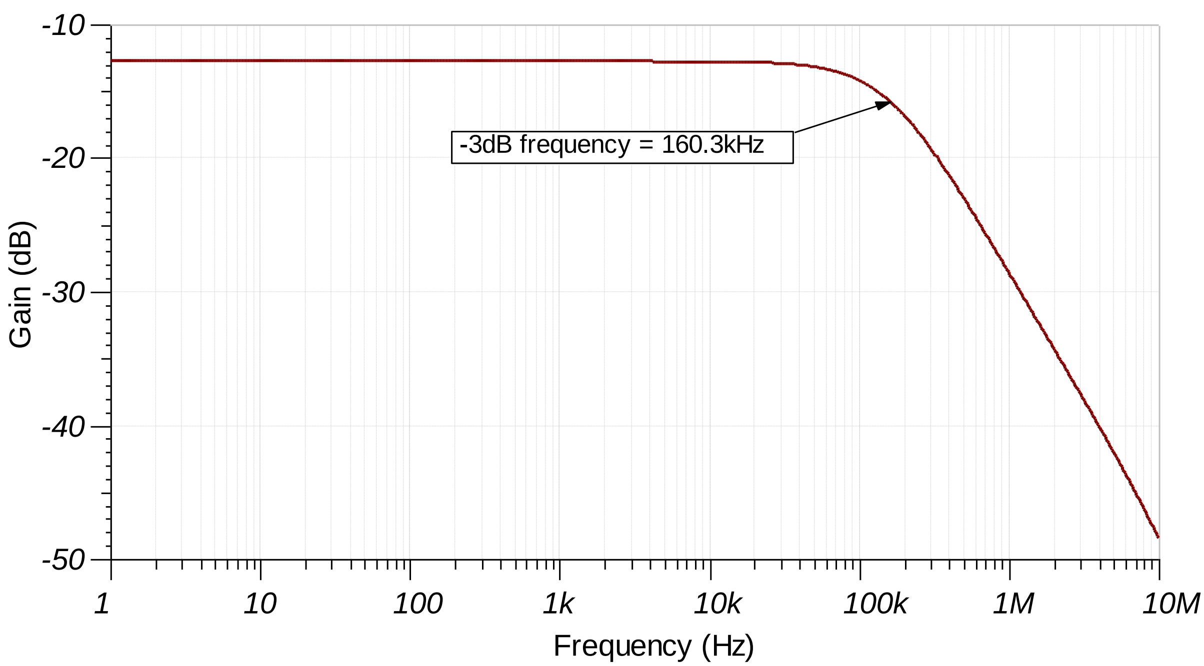
$$f_p = \frac{1}{2\pi \times R_2 \times C_1} = 160.3kHz$$

Design Simulations

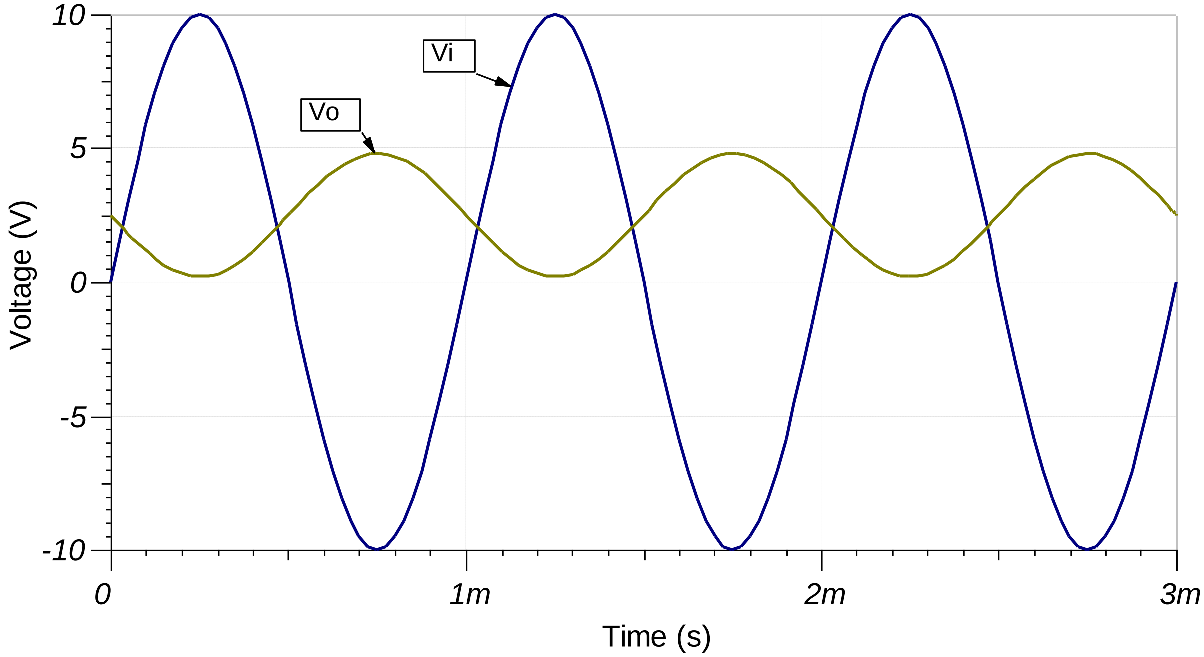
DC Simulation Results



AC Simulation Results



Transient Simulation Results



Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See TINA-TI™ circuit simulation file, SBOMAT9.

See TIPD148, http://www.ti.com/tool/TIPD148.

Design Featured Op Amp

OPA376	
V_{ss}	2.2V to 5.5V
V_{inCM}	Vee to Vcc-1.3V
V_{out}	Rail-to-rail
V_{os}	5µV
I_q	760µA/Ch
I_b	0.2pA
UGBW	5.5MHz
SR	2V/µs
#Channels	1,2,4
http://www.ti.com/product/opa376	

Design Featured Op Amp

OPA140	
V_{ss}	4.5V to 36V
V_{inCM}	Vee-0.1V to Vcc-3.5V
V_{out}	Rail-to-rail
V_{os}	30µV
I_q	1.8mA/Ch
I_b	±0.5pA
UGBW	11MHz
SR	20V/µs
#Channels	1,2,4
http://www.ti.com/product/opa375	

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